

SILICON INGOT

- First transition from non crystalline material to crystalline silicon now in crystal structures. Defects in non crystalline material acts as grain centers degrading performances.
- Orientation or cubic changes properties in silicon at some where with half incomplete bonds
- Si: diamond cubic lattice structure: two nested FCC one offset by $\frac{1}{4}$ in all directions atom covalent bonded to 4 NN
- Bulk properties generally isotropic as no differences in dopant diffusion for (111) (100) crystal. (\approx)

- DEFECTS

↳ POINT DEFECTS

anything other than Si on lattice is point defect (Frenkel pair F+V)
 Native point defect: missing Si vacancy V extra atom I interstitial concentration increasing with T. Concentration tends to be equal no thermodynamic reason

↳ LINE DEFECTS, DISLOCATIONS

Line: edge dislocation, loop dislocation. Extra plane terminates in a dislocation. Neutral present at start created due to high T steps fabrication, or stress in thin film deposition (stress also due to RTA or RTO). Form during cooling process as agglomeration of V or I. Can move due to shear stress along $\{111\}$ planes (Burton vector).

↳ 2D DEFECTS

Stacking faults form along $\{111\}$ planes insertion of normal or extra plane extrinsic if extra plane intrinsic if no plane. Surface stacking faults when reaches the surface

↳ VOLUME DEFECTS

Agglomeration or point defects (precipitates of dopants impurities) due to too high doping concentrations

Production of Silicon: quartzite (sand, SiO₂) \sim MGS \sim EGGS

- From ingot to wafer as: Ingot shaped till a uniform diameter, flats cuts (resistance in cutting wafer), saw into individual wafers, mechanical wiping (wafer wipers), round edges, chemical etching or sonics + chemical mechanical step of surface, CMP

- CZOCITRALSKI CRYSTAL GROWTH

↳ MAXIMUM PULL RATE $V_{\text{max}} = \frac{1}{LN} \sqrt{\frac{20 \varepsilon k_m T^5}{3\Gamma}}$

L = latent heat of fusion
 N = density of Si
 Γ = Stephan-Zeemann constant
 ε = viscosity of silicon
 k_m = thermal conductivity at melting T_m

↳ DOPING INCORPORATED

All impurities segregate between liquid and solid phases. $K_0 = \frac{C_s}{C_L}$ equilibrium segregation coefficient. This means impurities having different solubility in solid and liquid phase. Generally $K < 1$ that means doping increase ~~decrease~~ at end of ingot

additional heat of dV freezes means

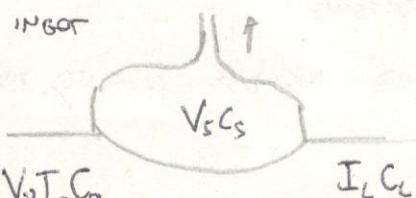
$$dI = -K_0 C_L dV = -K_0 \frac{I_L}{V_0 - V_S} dV$$

$$C_s = C_0 K (1-f)^{k-1}$$

$$\int_{I_0}^{I_L} \frac{dI}{I_0} = -K_0 \int_{V_0}^{V_S} \frac{dV}{V_0 - V_S}$$

$$I_L = I_0 \left(1 - \frac{V_S}{V_0}\right)^k$$

$$K_0 C_S = -\frac{dI_L}{dV_S}$$



WE DON'T CONSIDER A LOT OF NON IDEALITIES (BUT IT'S A GOOD MODEL) LIKE INHOMOGENEITIES IN IMPURITY CONCENTRATION OR CONDUCTION CURRENTS IN MELT.

ELECTRICAL MEASUREMENT

THIS TECHNIQUE IS NOT GOOD SCANNING RESOLUTION WE ASSUME PARAMETERS UNIFORM.

1- HOT POINT PROBE

TWO MODES ONE 25-100°C HOTTER HAVING OHMIC CONTACT WITH WATER A VOLTMETER WILL MEASURE THE POTENTIAL WHOSE POLARITY DETERMINES THE TYPE OF MATERIAL P-n.
HOT PROBE ^{N-TYPE} V THERMAL ENERGY OR E HIGHER THAN COLD PROBE SO WILL GO THROUGH HOT ONE DUE TO T GRADIENT; @ MOVING TO COLD LEADS + FIXED SITE ON NOT ONE DISTURBING THE AV. SAME WITH P TYPE BUT WITH REVERSED POLARITY. VOLTMETRIC ITSELF IMPLIES DROPS TO AVOID CURRENT FLOW AND TO ACHIEVE PICKUP OF e IN COLD PROBE AND OF + IN HOT (FOR N-TYPE). IF VOLTAGE IS LOW IMPEDANCE CURRENT $I_n = q \mu n P_n d t / \Delta x$ Pn THERMOELECTRIC POWER POSITION FOR h INTEGRATING FOR E. VOLTAGE UNKNOWN AS SETBACK VOLTAGE.

2- 4 POINT PROBE

4 POINT PROBE TO AVOID CURRENT SPREADING AND CONTACT RESISTANCE PROBLEMS, EXTERNAL PROBES INJECT CURRENT INTERNAL HIGH IMPEDANCE VOLTMETER TO NOT USE CURRENT FLOW INSIDE FROM THIS $\rho = 2 \pi s V / I$ S DISTANCE BETWEEN PROBES (WAFER DIAMETER AND THICKNESS $\gg s$)

3- HALL EFFECT

STRONG CONDUCTIVITY METHODS SINCE WE CAN DETERMINE TYPE, RESISTIVITY AND CARRIER MOBILITY

- DEFECTS MEASUREMENT WITH A GROW PROCESS (STEREOTEST) AND THEN ELECTRONIC MICROSCOPY

4- EMISSION MICROSCOPY

RESOLUTION OF OPTICAL SYSTEM GIVEN BY FIRST ORDER TO $R_s = \frac{\lambda}{NA}$ NA NUMERICAL APERTURE THAT IN EMISSION MICROSCOPY 0.01 AND $\lambda \approx 2$.

5- SEM SCANNING EMISSION MICROSCOPY

BEAM OF 1-100kV FOCUSED WITH ELECTROSTATIC - MAGNETIC LENS, FROM RESTED IN XY PATTERN BY SOME BLOCKS WILL BACKSCATTER FROM THE SAMPLE OTHER BLOCKS MATERIAL THAT WILL PROBES X-RAYS. SEM COLLECT X-RAYS AND e AND DISPLAYS THE INTENSITY OF THE SIGNAL ON A SCREEN. RESOLUTION $R_s \approx 5 \text{ nm}$ AND LARGEST DIAMETER OF FOCUS

6- TEM TRANSMISSION ELECTRON MICROSCOPY

OPERATES BY PASSING ELECTRONS COMPACTLY THROUGH THE SAMPLE, HIGHER ENERGY USED 100-300kV AND SAMPLE HAVE TO BE THINNER THAN 1μm. IMAGE COMES FROM TRANSMITTED ELECTRONS AFTER THEY PASS THROUGH THE SAMPLE AND IMAGED ON A PHOTOGRAPHIC PLATE. RESOLUTION OF 0.2nm IN AXIAL OR STOKE DIMENSIONS

7- INTEGRATION FROM SLIDES

→ I AND V CAN BE CHANGED

→ I IS A DISLOCATION IF WE CAN IDENTIFY A BIFUR VECTORS

→ WE LET THEM FLOW IN THE BULK AWAY FROM SURFACES IN THIS WAY THEY WILL GATHER IMPURITIES DURING WAFER PROCESSING

→ EPITAXY GROWTH OF SILICON AT GND TO HAVE HIGHEST QUALITY.

SILICON OXIDATION

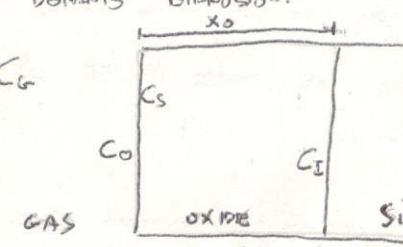
- INTERFACIAL DISTANCE BETWEEN Si AND SiO_2 VARY FROM MECHANICAL OR ELECTRICAL DEFECTS AND IT'S STRATEGY DURING TIME, ONE OR THE BEST INTERFACE WE CAN OBTAIN
- BURN AT RT Si EXPOSED TO OXYGEN AMBIENT FORM A THIN NATIVE OXIDE OR 0.5-1nm UNTIL AFTER A FEW HOURS STOPS AT 1-2nm
- THERMAL OXIDES IN THE RANGE OF 10-30nm ARE USED UNDER Si_3N_4 LAYERS AS SPARE MIGRATION OR PAD OXIDES DURING LOCOS PROCESSES. THICKER OXIDES USED AS MASKS.
- INTERFACIAL $\text{Si}-\text{SiO}_2$ BETTER IF SiO_2 GROWTH NOT DEPOSITED
- OXIDATION PROCESS OCCURS AT $\text{Si}-\text{SiO}_2$ INTERFACE, NEW INTERFACE CONSTANTLY FORMING AND MOVING DOWNWARDS INTO SILICON SUBSTRATE (DEMONSTRATION WITH 2 ISOTOPES OF OXYGEN AND THEN MASS ANALYSIS).
- PROCESS INVOLVES A VOLVING EXPANSION BECAUSE OF ROOM NEEDED FOR OXYGEN. GROWTH IS 46% IN SILICON AND 54% OUTWARD. THIS CAUSES "BOSS" PEAK IN LOCOS PROCESSES.
- NO CRYSTALLINE FORMS OF SiO_2 WHOSE LATTICE SITES MATCHES Si SUBSTRATE SO SiO_2 IS AMORPHOUS. BURN IF AMORPHOUS HAS A SHORT RANGE ORDERED SiO_4 TETRAHEDRAL BASIC FORMS OF SiO_2 . TETRAHEDRAL BOND STRENGTHENED BY SHARING OXYGEN ATOMS (BONDING OXYGEN ATOMS NOT SHARED NON-BONDING OXYGEN ATOMS)
- SiO_2 GROWTH ON SILICON IS IN COMPRESSIVE STRESS AND IN ADDITION THERMAL EXPANSION COMPENSATES ADD COMPRESSIVE STRESS TOO. THICKNESS OF CUBICATIC MUST BE ENOUGH TO SUSTAIN THIS STRESS. CUBICATING OF A WAFER AS A MEASUREMENT METHOD FOR OXIDE THICKNESS.
- FIRST UNDER THE INTERFACE IS PEAKET DEFECT DENSITY IN ORDER OF $10^9 - 10^{11} \text{ cm}^{-2}$ COMPARED TO A Si SURFACE DENSITY OF 10^{15} cm^{-2} . MOST DEFECTS RELATED TO INCOMPATIBLY OXIDIZED Si ATOMS OR Si ATOMS WITH BUNDLING BONDS
- DEFECTS IN SiO_2

- ↳ Q_f FIXED OXIDE CHARGE FOUND EXPERIMENTALLY A SHEET OR POSITIVE CHARGE IN OXIDE VERY CLOSE TO INTERFACE ($\approx 2\text{nm}$) AND IT'S LIKELY ASSOCIATED WITH THE TRANSITION FROM Si-SiO₂. DO NOT CHANGE DURING DEVICE OPERATION
- ↳ Q_{it} INTERFACE TRAPPED CHARGE DUE TO INCOMPATIBLY OXIDIZED Si ATOMS WITH BUNDLING BONDS NEAR THE SURFACE. THIS CHARGE CAN CHANGE CAPTURING e OR h DEPENDING ON THE DEVICE OPERATION.
- ↳ Process WITH HIGH Q_f HAS ALSO HIGH Q_{it} SO PROBABLY COMMON SOURCE, OXYGEN.
- ↳ Q_m MOBILE OXIDE CHARGE NOT SO NEGLECTABLE TODAY. MOBILE IONS K⁺ OR Na⁺ ELIMINATED WITH CLEANER CLEAN ROOMS
- ↳ Q_{et} OXIDE TRAPPED CHARGE LOCATED ANYWHERE IN THE OXIDE, LIKELY BROKEN Si-O BONDS IN TAIL OF THE OXIDE (BROKEN DUE TO PROCESS STEPS OR IONIZING RADIATION) NORMALLY DESTROYED BY HIGH TEMPERATURE ANNEAL. THIS MAY CAPTURE e OR h DURING DEVICE OPERATION RESULTING IN TRAPPED CHARGE. (NOT OF IMPORTANCE NOW DUE TO HIGH ELECTRIC FIELDS PRESENT IN DEVICES TODAY (NOT QUESTIONS))
- All THESE ANNEALED AT THE END OF FABRICATION IN Ar OR N₂ AMBIENT AND THEN ANNEAL IN H₂.

- To OXIDISE BASICALLY A FURNACE UP TO 1000-1200°C AND GAS DISTRIBUTION TO CONVECT H₂O or O₂ MUST FURNACES TODAY VARIOUS TO SPARE SPACE. WAFERS NORMALLY LOADED INTO FURNACES ON "BOATS" OF 10-50 WAFERS CARRIED BY AUTOMATIC LOADING SYSTEMS THAT DO NOT TOUCHES THE FURNACE WALLS. TEMPERATURE CONTROL WITH THERMO COUPLES IN ORDER TO MANTAIN UNIFORM T AROUND WAFERS. TIME CONTROL OF SECONDS AND T UP $\pm 0.5^\circ\text{C}$ AND NEEDED TO PRODUCING CONSISTENT OXIDE THICKNESS. IDEALLY WE WANT VERY SHOT HIGH T SHOTS.
- RTO RAPID THERMAL OXIDATION USES (AM) HEATED CHAMBER THAT CAN HEAT UP TO 1000°C /s HOLD THE WAFER AND THAN COOL IT DOWN TO RT AGAIN IN 1000 SECONDS. USUALLY THIS SYSTEMS ARE SINGLE WAFER. BIG PROBLEM IS KNOWING EXACTLY THIS WAFER TEMPERATURE (NOT POSSIBLE THE USE OF THERMO COUPLES HEAVY DUE TO FAST T CHANGE)
- Some OXIDATION HAS "FAST MODE" THAT IS A MIDDLE POINT ($100^\circ\text{C}/s$) BETWEEN CLASSIC AND RTO

IDEAL GROWTH MODEL

LINER PARABOLIC MODEL USED IN PLANNER OXIDATION. THIS MODEL CANNOT EXPLAIN SHARDED OXIDATIONS OR OXIDATION IN MIXED SITES OR VERY THIN OXIDE GROWTH. ALSO UNEXPLAINED HOW OXIDATION AFFECTS DOPANTS DIFFUSION.



ASSUME OXIDE ALREADY PRESENT x_0 AND ONLY PLANE SURFACE. 3 MAIN FLUXES F_1 TRANSPORT OF OXIDANT IN GAS PHASE TO OXIDE SURFACE $F_1 = h_g (C_o - C_s)$ h_g MASS TRANSFER COEFFICIENT. DEFINING C_o AS THE CONCENTRATION OF GAS JUST OUTSIDE THE SURFACE WE CAN WRITE THE HENRY'S LAW $C_o = h_p P_g$ BUT WE CAN'T KNOW P_g (PARTIAL PRESSURE OF OXIDANT AT SOLID INTERFACE) SO IT'S CONVENIENT TO WRITE C_o IN FUNCTION OF P_g THE TOTAL GAS PRESSURE AS $C^* = h_p P_g$ BEING C^* THE OXIDANT CONCENTRATION THAT WILL BE IN EQUILIBRIUM WITH P_g WE CAN NOW ASSUME $C^* \approx C_o$ $P_g \approx P_s$ (THIS NOT LIMITING TERM SO WE CAN) FROM IDEAL GAS LAW $C_o = P_g / RT$ AND $C_s = P_s / RT$ USING THIS IN THE EXPRESSION OF THE FLUX WE OBTAIN $F_1 = h(C^* - C_o)$ WITH $h = h_o / R T$.

FLUX 2 IS THE DIFFUSION THROUGHOUT OXIDANT TO THE INTERFACE WITH SILICON THAT USING FICKL'S LAW $F_2 = -D \frac{dC}{dx} = D \left(\frac{C_o - C_i}{x_0} \right)$ THIS ASSUMING PROCESS AT STEADY STATE.

FLUX 3 REACTION AT Si-SiO₂ INTERFACE $F_3 = k C_i$ WE HAVE A LOT OF PARAMETERS.

IN STEADY STATE CONDITION $F_1 = F_2 = F_3$ SO WE OBTAIN \downarrow . WE HAVE USED

$$\left. \begin{aligned} C_i &= C^* \left(1 + \frac{V_s}{h} + \frac{V_s x_0}{D} \right) \approx C^* \left(1 + \frac{V_s x_0}{D} \right) \\ C_o &\approx C^* \end{aligned} \right\}$$

THE ASSUMPTION OF $h \gg 1$ MUCH LARGER THAN ALL OTHER PARAMETERS. WE CAN OBSERVE TWO REGIMES

- $V_s x_0 / D \ll 1$ $C_i \approx C^*$ OXIDANT SUPPLIED FASTER THAN IT REACTS. THIS IS REACTION RATE CONTROLLED
- $V_s x_0 / D \gg 1$, $C_i \approx 0$ OXYGEN REACTING FASTER THAN N_a

IF REGIME, DIFFUSION CONTROLS REGIME. WE CAN COMBINE FLUX AND SILICON DEPOSITION TO OBTAIN $\frac{dx_0}{dt} = \frac{F_1}{N_A} = \frac{k_s C^*}{N_A} \left(1 + \frac{V_s x_0}{D} \right)$ NO NUMBER OF OXIDANT MOLECULES INCORPORATED PER UNIT VOLUME OF OXIDE GROWTH. INTEGRATING THIS WE OBTAIN $\frac{x_0^2 - x_i^2}{B} + \frac{x_0 - x_i}{B/A} = t$ WHERE $B = 2DC^*/N_A$, $B/A = C^* V_s / N_A$. COEFFICIENTS B AND B/A EXPERIMENTALLY OBTAINED AND HAVE APPROXIMATELY FORM B/A CONCERN. FOR REACTION WITH SURFACE B THE TRANSPORT. WE CAN GENERATE WRITING $\frac{x_0^2}{B} + \frac{x_0 - x_i}{B/A} = t$ WHERE t IS THE TIME TO CREATE THE ALREADY PRESENT OXIDE. ACTIVATION ENERGY OF $B/A \approx 2eV$ ENERGY TO BREAK Si-Si BONDS.

↳ CRYSTAL ORIENTATION MAY AFFECT THE PARAMETER B/A SINCE NONE Si ATOMS ARE PRESENT HIGHEN THE SPACE FOR REACTION WILL BE IN RACE ($B_{AlIn} = B_{AlLiO_2} \approx 1.68 = B_{AlClO_3}$) (WE HAVE MORE SILICON BONDS). CRYSTAL ORIENTATION DO NOT AFFECT B THAT TAKES INTO ACCOUNT THE DIFFUSION THROUGHOUT THE EXISTING OXIDE. THIS CAN CREATE PROBLEM IN 3D STRUCTURE SINCE NONE SURFACES WILL BE EXPOSED

↳ OVER FIRST 20nm OF OXIDE THIS MODEL DOES NOT WORK WE HAVE TO INCLUDE AN A TERM IN THE MODEL $\frac{dx_0}{dt} = \frac{B}{2x_0 + A} + C \exp(-\frac{x_0}{L})$ $L = 7nm$ THIS MODEL MATCHES THE EFFECTIVE GROWTH RATE

↳ SUBSTRATE DOPING PROFILE WILL CHANGE DURING OXIDATION DEPENDING ON IMPURITIES DIFFUSIVITY AND SEGREGATION COEFFICIENTS (ALSO PLUG BURN)

↳ OXIDATION PROCESS CONSUMES VACANCIES AND INJECT INTERSTITIALS (VOLUME EXPANSION)

- MEASUREMENT METHOD

↳ PHYSICAL MEASUREMENTS.

ETCH THE SiO₂ (IE) AND WITH STYLUS PROFILER OXIDE THICKNESS OR ALSO SIM OR TEM MICROSCOPY BUT THIS PROVIDES ONLY THE THICKNESS OF THE SiO₂ AND NOT OTHER TRANSPORTS

↳ OPTICAL MEASUREMENTS

- MONOCROMATIC WAVELENGTH INTO SILICON AT A CERTAIN ANGLE SOME LIGHT WILL BE ABSORBED BY SURFACE AND REFLECTED BY THE INNER SURFACE SO THAT THE 2 LIGHT REFLECTED IN DIFFERENT PLACES (OPTICAL PATH) WILL

CREATE DISTORTING OR CONSTRUCTIVE INTERFERENCE. FROM THIS ONE CAN DEDUCE THE OXIDE THICKNESS. THIS WORKS FOR THICKNESS OF A FEW FEET OR MM

- Ellipsometry same as before but with polarized light and take each thickness of polarization with can deduce to this works down to 1nm
- Color change (colours reflects over 30nm) estimate within 10-20nm can be made with this change but oxides thinner than 5nm has no colour

↳ EMISSION MEASUREMENTS: MOS CAPACITOR (SEE BUGGON DENOTES COURSE)

- INTEGRATION FROM THE SLIDES

- Nitridation mainly used to form a barrier to the diffusion of B from Si to SiO₂

- ADVANCED OXIDATION TECHNIQUES:

RADICAL OXIDATION: H₂ AND O₂ INTO PTO CHAMBER WATER AND RADICALS LIKE O AND OH ARE FORMED AND THIS WITH LOW PRESSURES GUARANTEES HIGH QUALITY OXIDES

PLASMA OXIDATION: LOW THERMAL BUDGET BUT ULTRA THIN AND QUALITY OXIDES

THIN FILM DEPOSITION

- MAIN ISSUES WHEN TALKING ABOUT THIN FILM AND THIS QUALITY OF DEPOSITED FILM (IN TERMS OF COMPOSITION, CONTAMINATION LEVELS, DEFECT DENSITY AND MECHANICAL AND ELECTRICAL PROPERTIES) STRESS IN THE FILMS (THAT SHOULD BE MINIMUM) MECHANICAL STABILITY DURING SUBSEQUENT PROCESSES AND GOOD ADHESION TO UNDERLYING FILMS.
- WE WANT ALSO UNIFORM THICKNESS ACROSS WAFER FROM WAFER TO WAFER AND AS FILM COSS NON-PUNAL TOPOLOGY.
- STEP COVERAGE: COVERAGE ON THE SIDE OF A STEP OR EVEN QUANTITABLY AS MINIMUM THICKNESS ON SIDE OF A STEP DIVIDED BY THICKNESS ON TOP HORIZONTAL SURFACE IF THIS RATIO = 1 CONFORMAL COVERAGE
- GAP FILLING: ABILITY TO FILL VIAS OR CONTACTS WITH HIGH ASPECT RATIO ($= \frac{h}{l}$). INCOMPLETE FILLING OF A GAP CAN CAUSE HIGH RESISTANCE PATH (IF METAL LINE) STRESS & CAN TRAP CHEMICALS LEADING TO RELIABILITY ISSUES
- TWO MAIN CATEGORIES: CHEMICAL AND PHYSICAL VAPOR DEPOSITION OR CVD PVD.
CVD HISTORICALLY FOR Si AND DIELECTRIC DEPOSITION DUE TO GOOD QUALITY FILMS AND GOOD STEP COVERAGE WHILE PVD FOR METAL LINES.
- THIRD CATEGORY COATING A WAFER WITH A LIQUID FILM THAT FORMS A SOLID WHEN HEATED. THIS SPIN ON GLASSES (SOGs)
- FOURTH CATEGORY BUBBLING DEPOSITION MAINLY USED TO DEPOSIT Cu LINES.

- CVD

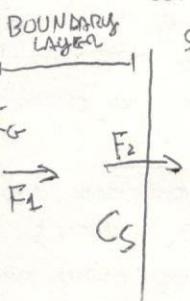
- GAS INTRODUCED INTO DEPOSITION CHAMBER WHERE THEY REACT AND FORM THE DESIRED FILM ON THE WAFER. GAS STREAM REACTIONS CAN CREATE PARTICULATES WHICH CAN DROP DOWN onto THE SURFACE AND CREATE DEFECTS
- SIMPLEST ATMOSPHERIC PRESSURE CVD OR APCVD. WALLS OF THE CHAMBER NOT HEATED TO REDUCE DEPOSITION ON THEM BUT WAFER HEATED WITH RF COATED GRAPHITE SUSPENSIONS HEATED BY RF INDUCTION
- LOW PRESSURE CVD (LPCVD) HOT WALL REACTION WAFER PLACED IN A CHAMBER SIMILAR TO OXIDATION SYSTEMS
- OTHER TYPES USE SOG GASEOUS REACTANTS AND PLASMA. VERY LOW THERMAL BUDGET.

- ATMOSPHERIC PRESSURE CHEMICAL VAPOR DEPOSITION (APCVD)

- + STEP INVOLVED BASICALLY ARE 1) TRANSPORT OF REACTANTS THROUGH CONVECTION TO DEPOSITION REGION 2) TRANSPORT BY DIFFUSION FROM GAS STREAM TO SURFACE 3) ABSORPTION OF REACTANTS ON WAFER SURFACE 4) SURFACE PROCESS 5) DESORPTION OF BY-PRODUCTS FROM THE SURFACE 6) TRANSPORT OF BY-PRODUCTS AWAY FROM THE SURFACE BY CONVECTION.
- + A NON MENTIONED PHASE IS THE ABSTRACTION THAT IS THE MOVE AWAY OF ABSTRACTING SPECIES BEFORE THEY REACT (COLLISION WITH STICKING COEFFICIENT). ALSO SURFACE MIGRATION DON'T MENTIONED.

+ IN OUR ANALYSIS WE WILL NOT CONSIDER GAS-PHASE REACTIONS.

+ THE MOST IMPORTANT STEPS ARE 2) THAT IS MASS TRANSFER OF REACTANTS THROUGH THE BOUNDARY LAYER AND STEPS 3-5 THAT WE WILL USE AS SURFACE REACTIONS.



Si + Flux 1 THAT NAME SUGGESTS THE FLOW OF REACTANTS SPECIES FROM BULK OF THE GAS TO THE SURFACE (THROUGH THE BOUNDARY LAYER)
 $F_1 = h_g (C_G - C_S)$ C_G CONCENTRATION IN GAS FLOW C_S CONCENTRATION AT THE SURFACE OR REACTANTS SPECIES h_g MASS TRANSPORT COEFFICIENT

+ Flux 2 FLOW OF REACTANTS CONSUMED AT THE SURFACE BY REACTION
 $F_2 = k C_S$ k CHEMICAL SURFACE REACTION RATE.

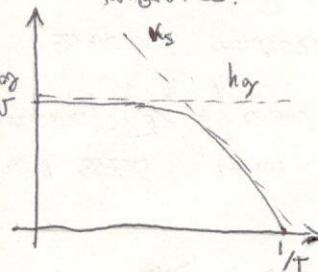
+ ASSUMING STATIONARY STATIC CONDITIONS $F_1 = F_2 = F$ $\Rightarrow C_S = C_G \left(1 + \frac{V_S}{h_g}\right)^{-1}$ AND SO

GROWTH RATE $\gamma = \frac{F}{N} = \frac{v_{\text{sho}}}{v_{\text{sho}}} \cdot \frac{C_N}{N}$ WHERE N NUMBER OF ATOMS INCORPORATED PER S
 UNIT VOLUME IN THE FILM. DIVIDING $\gamma = \frac{C_N}{C_T}$ WE CAN WRITE $\gamma = \frac{v_{\text{sho}}}{v_{\text{sho}}} \cdot \frac{C_T}{N} \gamma$ WHERE
 OF CONCENTRATION OR ALL MOLECULES IN GAS.

f If $v_{\text{sho}} \propto C_T$ $\gamma \propto \frac{C_T}{N} \gamma$ SURFACE REACTION CONTROLLED CASE } TWO REGIMES

f If $v_{\text{sho}} \propto C_T$ $\gamma \propto \frac{C_T}{N} \gamma$ MASS TRANSFER CONTROLLED REGIMES

f GROWTH IN BOTH REGIMES IS LINEAR BECAUSE REACTION ALWAYS OCCURS AT GROWTH INTERFACE.

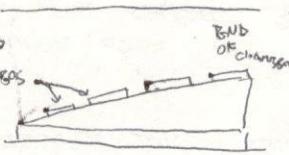


+ THE TWO REGIMES DOMINATES IN DIFFERENT TEMPERATURE RANGES DUE TO THEIR DEPENDENCE WITH T , $v_{\text{sho}} \propto \exp(1/T)$ $\gamma \propto \text{constant}$ (v_{sho} HAS ARRHENIUS FORM)

f IN MASS TRANSFER REGIME THE FLOW OF GAS AND BOUNDARY LAYER CONTROL (SO THE GEOMETRY OF THE REACTOR) AND FLOW RESTRICTIONS ON THE ABSORPTION OF THE WAFER AND THERMAL POSITION

f IN SURFACE REACTION REGIME T IS CRUCIAL BUT THE GEOMETRY OF THE CHAMBER NOT SO WAFERS CAN BE STACKED ONE ON ANOTHER.

+ USING S_s AS THE BOUNDARY LAYER THICKNESS THIS TERM IS NOT CONSTANT THROUGHOUT THE CHAMBER BUT INCREASES AND SINCE $\gamma \propto D_g/S_s$ WHERE D_g IS THE GAS DIFFUSION COEFFICIENT THE WAFER HAS TO BE PLACED THROUGH THE FLOW TO KEEP γ CONSTANT FURTHERMORE THE CONCENTRATION OF REACTANTS SPECIES ALSO DECREASE ALONG THE CHAMBER. FOR THIS TWO REASON WAFER HAVE TO BE PLACED ON A TILTED SURFACE.

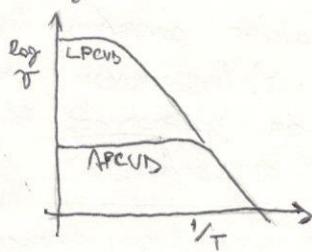


f HIGH TEMPERATURE PROCESS MEANS HIGH QUALITY FILMS THAT ARE BAD RATHER WANT LOW T (AND SO REACTION REGIME) GIVES US GOOD RICHES

- LOW PRESSURE CHEMICAL VAPOR DEPOSITION (LPCVD)

f WE WANT TO AVOID GEOMETRY PROBLEMS OR APCVD KEEPING GOOD QUALITY FILMS AND A NICE GROWTH RATE. (IN THIS WAY WE CAN STACK WAFERS IN BOATS)

f $\gamma \propto \frac{D_g}{S_s} \propto \frac{1}{P}$ SO DECREASING THE PRESSURE WE CAN ACTIVATE HIGHER γ AND SO INCREASE THE REACTION CONTROLLED REGIMES



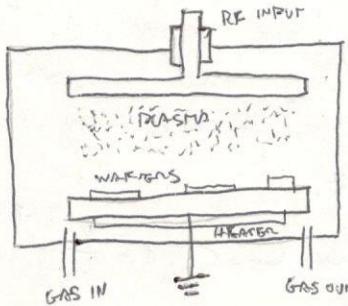
f DEPOSITION NO LONGER DEPENDENT ON GEOMETRY SO WAFERS CAN BE STACKED WITHOUT AFFECTING DEPOSITION UNIFORMITY

f LOWER PRESSURE MEANS ALSO LOWER GAS PHASE COLLISIONS AND REACTIONS AND SO LOWER DEFECTS IN THE FILM

- PLASMA ENHANCED CHEMICAL VAPOUR DEPOSITION (PECVD)

f SOMETIMES THERES ABS RESTRICTIONS TO TEMPERATURE PASSAGE (IF ALREADY NO MORE THAN 450°C CAN BE ACHIEVED)

f PECVD IN ADDITION TO A THERMAL SOURCE TO PROVIDE THE ENERGY NEEDED FOR CHEMICAL REACTIONS TO OCCUR A PLASMA SOURCE IS USED (PLASMA ARE HIGHLY IONIZED GAS)



f BY SUPPLYING ADDITIONAL ENERGY FROM THE PLASMA TO THE REACTANT GAS THE REACTION NEEDED FOR DEPOSITION CAN OCCUR EVEN AT RT

f PLASMA INTERACTION CAUSES REACTANT GASES TO DISOCIATE AND IONIZE IN A VARIETY OF SPECIES SUCH AS RADICALS THAT ARE HIGHLY REACTIVE AND WITH OTHER SPECIES FINDING THE FILM.

f FREE RADICALS REACT WITH NEUTRAL SPECIES THAT HAVE INCOMPATIBLE BONDING

+ In addition to ion and ion beam bombardment from the plasma can occur.

+ PECVD can result in good coverage and filling gaps also at low T.

- HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION (HDPCVD)

- + Very high density plasma and separate RF bias applied to the substrates
- + Combines PECVD techniques with bias sputtering to obtain very good narrow gap filling
- + Mostly used for SiO_2 deposition

- PVD

- More versatile than CVD allowing almost any material deposition
- Very low gas pressure in this system so very few gas phase collisions
- Little re-deposition of atoms usually occurs on surfaces so shadowing effects and gap filling problems are not

- EVAPORATION



f Source material is heated in a vacuum chamber and evaporated atoms condense on the chamber and on wafers. Heater resistance type (but this leads to contamination) or e-beam heater that can achieve heating T without contamination effects (side effect of e-beam is production of X-rays that can damage oxide)

f Low pressures (10^{-5} torr) leads to few gas phase collision and atoms travel in straight lines from surface to wafers.

f We can model our evaporation in two ways as a point source or a small planar source on a small V surface

~ Point source
The flux F_p leaving the source A_k is $F_p = \frac{R_{\text{evap}}}{\pi r^2}$ where R_{evap} is the evaporation rate and $\pi = 2\pi$ for a source emitting only upwards or for a source emitting in all directions.
This flux that strike A_k depends on the normal component of the flux of a source emitting in all directions. This flux that strike A_k depends on the normal component of the flux of a source emitting in all directions. We must multiply for $\cos \theta_i$ being the angle between the source normal and the direction of the source, dividing this flux for the density of the material deposited w/ get the velocity of deposition $V = \frac{F_{\text{evap}} \cos \theta_i}{\rho N k}$.

~ Small surface source
The emitted flux is written for normal direction. Emission from small planar surface known as ideal cosine emission. Extra term $\cos \theta_i$ comes into play so deposition rate becomes $V = \frac{R_{\text{evap}}}{\pi N k} \cos \theta_i$ (ideal cosine emission also describes reflection or materials)

f For small planar surfaces more anisotropic emissions can occurs and can be modeled as $\cos^n \theta_i$ with $n > 1$. This can be due to crucible geometry or ratio matl. depth vs melt surface area.

L The term $R_{\text{evap}} \propto \left(\frac{m}{T}\right)^{1/2} \cdot P_e$ As angle of source m - gram-molecular mass Pe vapour pressure dramatically depending on temperature

f Big drawback not all material easy to evaporate and no in-situ monitoring and poor step covering

f Sticking coefficient near to 1 and poor narrow angles of annular distribution leads to low step coverage and gap filling properties.

- SPUTTER DEPOSITION
- DC SPUTTER DEPOSITION
 - INLET GAS (Ar) FLOWS INTO SPUTTERING CHAMBER AT LOW PRESSURES AND VOLTAGES APPLIED BETWEEN TWO ELECTRODES AND PLASMA IS COLLIMATED.
 - PLASMA CONTAINS NEUTRAL ATOMS AND A MIXTURE OF POSITIVE IONS AND FREE ELECTRONS.
 - TOP ELECTRODE WITH NEGATIVE VOLTAGE IS APPLIED TO THE SOURCE MATERIAL TO BE DEPOSITED (CATHODE OR TARGET). BOTTOM ELECTRODE METAL PLATE IS WITHOUT WARPS SINCE IT IS GROUNDED AND CAUSES A NODE.
 - POSITIVE IONS ACCELERATED THROUGH THE TARGET STRIKE AND DISLOCATE OR SPUTTER THE TARGET METAL ATOMS THAT ARE FREE TO MOVE THROUGH THE PLASMA UNTIL THEY REACH THE WORKPIECE.
- TARGET MUST BE CONDUCTIVE TO DEPOSIT INSULATORS OTHER TECHNIQUES MUST BE USED.
- AN ACCELERATED SPUTTER ATOMS THAT MIGRATE THROUGH THE CHAMBER WHILE THEY CAN STAY ABSORBED, MIGRATE TO ANOTHER SURFACE OR BE REFLECTED. AN ACCELERATED ION CAN ABSORB NEUTRALS DURING SPUTTERING AND INCORPORATED DURING THE FILM.
- SECONDARY ELECTRONS CAN BE EMITTED DURING SPUTTERING BY THE TARGET THAT CAN IONIZE IMPURITIES THAT TRAVEL TO WORKPIECE TO IONIZE AN SUSTAIN THE PLASMA.
- SPUTTERING YIELD RANGE BETWEEN 0.1 AND 0.3 AND DEPENDS ON MATERIAL, ION ENERGY AND ION ANGULAR DISTRIBUTION.
- SPUTTERING TARGETS USUALLY WIDE SO THIS PROVIDES A NARROW ANGULAR DISTRIBUTION THAT LEADS TO GOOD STEP COVERAGE.
- RF SPUTTER DEPOSITION
 - TO SPUTTER NON CONDUCTIVE MATERIAL WE NEED A RF VOLTAGE INSTEAD OF A DC ONE. FREQUENCIES USED: 13.56 MHz TARGET DESIGN TO BE HIGH ENOUGH SO THAT A CONTINUOUS PLASMA DISCHARGE IS MAINTAINED.
 - ELECTRONIC FIELDS ARE NOT THE SAME BUT THE RF CURRENT MUST BE CONTINUOUS SO $\frac{V_1}{V_2} = \left(\frac{A_2}{A_1}\right)^m$ WHERE m IS EXPONENTIALLY 1-2. FINE TUNING THE RATIO BETWEEN THE 2 ANGLES WE CAN TUNE THE AMOUNT OF SCATTERING ON WORKPIECE PLATES.
 - SHIELDS ARE REQUIRED AND GUARANTEES A SELF BIASING STEADY STATE CONDITION AT ELECTRODES.
 - REACTIVE SPUTTER DEPOSITION: REACTING GAS IS ADDED IN PLASMA AND HELD AND CONCERN DEPOSITION (Ti SPUTTER N GAS TiN DEPOSITED).
 - BIAS SPUTTERING: WORKPIECE IS BIASED IN ORDER TO GET A SURFACE CLEANING OR WORKPIECE OR DEPOSITION AND SPUTTERING AT SAME TIME.
 - MAGNETRON SPUTTERING: MAGNET ADDITION TO IMPROVE IONIZATION OF THE PLASMA COLLIMATED SPUTTERING INCLUDING GAP KILLING PERFORMANCE BY ALLOWING NARROW ANGULAR DISTRIBUTION.
 - IONIZED SPUTTERING: IN SOME CASE THE MATERIAL TO BE DEPOSITED IS IONIZED AN RF COIL AROUND THE PLASMA INDUCES COLLISION TO CATCHES IONS. THIS PROVIDES NARROW ANGULAR DISTRIBUTION.

DOPANT DIFFUSION

- PRE-DEPOSITION: DOPING OCCURS PROBABLY BY AN INITIAL PRE-STORE STEP TO INTRODUCE THE PREVIOUS DOSE OR DOPANT IN THE SUBSTRATE
- DOPING-IN: A SUBSEQUENT (TOP) DOPING-IN ANNEAL THEN DISTRIBUTES THE DOPANTS TO DESIRED PARAMETERS.
- SOLID SOLUBILITY: MAXIMUM CONCENTRATION OF A DOPANT THAT CAN BE DISSOLVED IN Si UNDER EQUILIBRIUM CONDITIONS WITHOUT FORMING A SEPARATE PHASE (OFTEN THIS COMPLEX, TYPICALLY PRECIPITATES)
- SIMS MEASUREMENT TECHNIQUES MEASURING ALSO PRECIPITATES AND CAN'T DISTINGUISH BETWEEN ACTIVE dopants (THE IMPORTANT ONE) AND UNACTIVE dopants.
- ELECTRICAL SOLUBILITY MAY BE DIFFERENT THAN SOLID SOLUBILITY (ABOUT 10x)
- INACTIVE dopants ARE FORMED THAT DO NOT CONTRIBUTE FREE CARRIERS
- A SITE CAN BE IMPLANTED IN "E-ACTIVE" POSITIONS UNTIL HIS SOLID SOLUBILITY ($> E_{\text{SOLUB}}$) BUT THERE IS A HUGE FORCE THAT TENDS TO UNACTIVE AS DURING SUBSEQUENT THERMAL ANNEALING (As ATOMS SWAP VACANCY AND REMAIN INACTIVE).

- DIFFUSION FROM MACROSCOPIC VIEW POINT

✓ FICK'S FIRST LAW: FLOW OF MATERIAL PROPORTIONAL TO CONCENTRATION GRADIENT
 $F = -D \frac{\partial C}{\partial X}$ IN A DIAMOND LATTICE AS Si D HAS THE SAME VALUE IN ALL DIRECTIONS

✓ FICK'S SECOND LAW: CONSERVATION LAW FOR MATTER, INCREASE OF CONCENTRATION IN A VOLUME WITH TIME IS THE DIFFERENCE OF FLUX INSIDE AND OUTSIDE THE VOLUME $\frac{\partial C}{\partial t} = \frac{\partial F}{\partial X} = \frac{F_{\text{out}} - F_{\text{in}}}{\Delta X}$

✓ SUBSTITUTING THE FIRST LAW INTO THE SECOND WE OBTAIN $\frac{\partial C}{\partial t} = \frac{\partial}{\partial X} \left(D \frac{\partial C}{\partial X} \right)$ THAT SUPPOSING D CONSTANT (AT $T = \bar{T}$) GIVES $\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial X^2}$ THIS IS CALLED FICK'S SECOND LAW OF DIFFUSION. SIMPLER SOLUTION OF THIS IS IN STEADY STATE CONDITION SO $D \frac{\partial^2 C}{\partial X^2} = 0$ THAT GIVES $C = a + xb$.

- ANALYTIC SOLUTIONS OF DIFFUSION EQUATION

↳ GAUSSIAN SOLUTION IN INFINITE MEDIUM

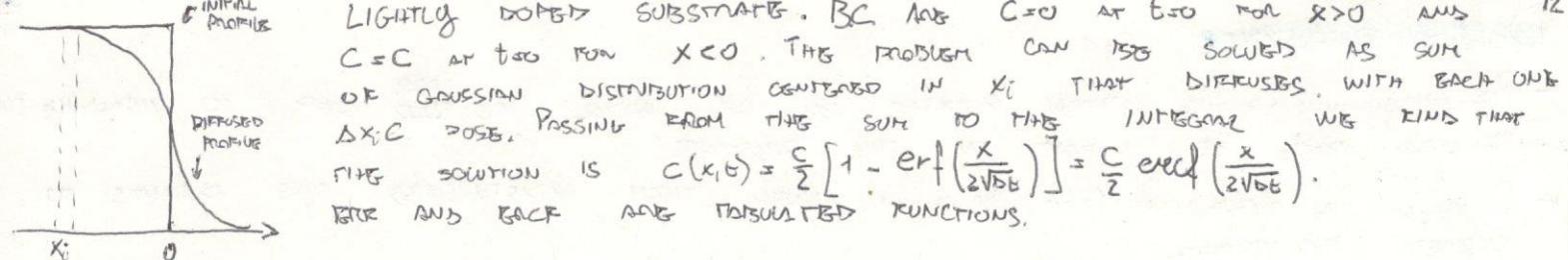
DOSAGE SPIKE IN A LIGHTLY DOPED REGION (LOW T EPITAXIAL GROWTH OF SINGLE CRYSTAL Si ON A Si WAFER AND INTRODUCES DOPANT GAS INTO CHAMBER FOR SHORT AMOUNT OF TIME). BOUNDARY CONDITIONS ARE $C \rightarrow 0$ AS $t \rightarrow \infty$ FOR $x > 0$ AND $C \rightarrow \infty$ AS $t \rightarrow 0$ FOR $x < 0$ AND THE DOSE $Q = \int_{-\infty}^{+\infty} C(x,t) dx$. SOLUTION TO FICK'S LAW FOR THIS B.C. IS A GAUSSIAN FUNCTION PROFILE THAT EVOLVES WITH TIME AND RETAINS THE SAME GAUSSIAN FORM $C(x,t) = \frac{Q}{2\sqrt{\pi D t}} \exp\left(-\frac{x^2}{4Dt}\right)$ RULES OF THUMB TO KNOW HOW MUCH THE DOPANTS IS DISPERSED IS LOOKING AT THE DIFFUSION LENGTH $\sqrt{4Dt}$. ION IMPLANTS MORNING AND IN FIRST ORDER GAUSSIANS.

↳ GAUSSIAN NEAR A SURFACE

DOPANTS DOSE NEAR A SURFACE SPIKE (DOSED BY LOW ENERGY ION IMPLANTATION) ASSUMPTION: NO DOPANT LOSS DOPANT DOSE CONSTANT, EVAPORATION OR SEGREGATION EFFECT EQUAL 0. WE CAN NEGLECT PRECONDITION PROBLEMS BY CONSIDERING A DOSE $2Q$ AND THE SURFACE A MIRROR IMAGE SO THAT WE OBTAIN $C(x,t) = \frac{Q}{\sqrt{4\pi D t}} \exp\left(-\frac{x^2}{4Dt}\right)$ EQUAL TO SOLUTION OF STRONG WITHOUT $\frac{1}{2}$

↳ GAUSSIAN FUNCTION SOLUTION IN INFINITE MEDIUM

DIFFUSION FROM AN INFINITE SOURCE OF DOPANT (HEAVILY DOPED EPITAXIAL LAYER ON



\hookrightarrow Error Function Solution Near a Surface

CONSTANT SURFACE CONCENTRATION ALL TIMES (DIFFUSION FROM GAS AMBIENT WITH CONCENTRATION ALONGS SOURCE SOLUBILITY) WE ARE NEAR A SURFACE. THE MIDPOINT R MUST REMAIN STATIONARY AND THE SOLUTION ON x>0 IS STILL VALID. THE SURFACE CONCENTRATION IS HELD CONSTANT AND THIS CONSIDERATIONS LEADS TO $C(x,t) = C_s \left[\text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \right]$. THE TOTAL DOSE IMPLANTED WILL BE $Q = \frac{2C_s}{\sqrt{\pi}} \sqrt{Dt}$

- PARABOLIC FUNCTION SOLUTION APPLIES WHEN THE TARGET IS AN INFINITE SOURCE OF DOPANTS WHICH IMPLIES THAT AN INCREASING DOSE OF DOPANTS IS INTRODUCED IN THE SUBSTRATE DURING DIFFUSION PROCESS TO MAINTAIN CONSTANT SURFACE CONCENTRATION.

GAUSSIAN SOLUTION APPLIES WHEN THE DOSE IS FIXED AND SO THE SURFACE CONCENTRATION MUST DEPEND AS DOPANT DISSOLVED IN THE BULK

- DIFFUSION COEFFICIENT D HAS AN ARRHENIUS FORM SO A STRONG DEPENDENCE WITH TEMPERATURE. SINCE THERE ARE A LOT OF PROCESSES IN A SINGLE PRODUCTION THE EFFECTIVE PRODUCT DT IS GIVEN BY $D_{eff} = D_{e,T_1} + D_{e,T_2} \dots$ THE TOTAL EFFECTIVE DT IS GIVEN BY THE SUM OF ALL DT PROCESSES AND SINCE D IS EXPONENTIALLY DEPENDENT WITH TEMPERATURE THE HIGHEST TEMPERATURE STEPS IN THE PROCESS GENERALLY DOMINATE AMONG THE OTHERS.

- CORRECTIONS TO FICK'S LAW

\hookrightarrow ELECTRIC FIELD EFFECTS

WITH AN EXTERNAL FORCE ACTING ON DIFFUSING SPECIES WE HAVE TO ADD AN ADDITIONAL TERM TO $F = -D \frac{dC}{dx} + Cv$ AND ALSO TO FICK'S LAW $\frac{dC}{dx} = \frac{2}{\lambda k} \left(\frac{D_e}{kT} \frac{dC}{dx} \right) - v \frac{dC}{dx}$. THIS ADDITIONAL FORCE IS AN ELECTRIC FORCE CAUSED BY THE FACT THAT DIFFUSING SPECIES AND e, h HAVE DIFFERENT MOBILITIES (ACTUALLY $D_{ion} \ll D_{eh}$). EUSCOMONS WILL TEND TO DIFFUSE AHEAD OF DONORS LEAVING BEHIND POSITIVELY CHARGED DONOR CREATING AN ELECTRIC FIELD TO SET UP CAUSING AN ENHANCED DIFFUSION.

THIS CAN BE TAKEN INTO ACCOUNT BY A FACTOR h IN FICK'S LAW $F = -D_h \frac{dC}{dx}$ WHERE $h = 1 + C/\sqrt{C + 4m^2}$ WHICH HAS AN UPPER BOUND OF 2 (THIS WHEN DOPING CONCENTRATION IS MUCH HIGHER THAN INTRINSIC CARBON CONCENTRATION).

\hookrightarrow CONCENTRATION DEPENDENT D EFFECTS

DIFFUSIVITY D VARIES WITH CONCENTRATION WITH HIGHER CONCENTRATION NEGATIVE DIFFUSING RATHER THAN LOW CONCENTRATION CAUSING A MORE BOK-LIKE PROFILE RATHER THAN A GAUSSIAN ONE (OR TRUE). THE DIRECT CONSEQUENCE OF THIS PROBLEM IS THAT $\frac{dC}{dx} = \frac{\partial}{\partial x} \left(D_{eff} \frac{dC}{dx} \right)$ MUST BE COMPUTED NUMERICALLY SINCE $D = D(x)$

\hookrightarrow SEGREGATION EFFECTS

DOPANTS HAVE DIFFERENT SOLUBILITIES IN DIFFERENT MATERIALS AND SO REDISTRIBUTE AT THE INTERFACE UNLESS THE CHEMICAL POTENTIAL IS THE SAME IN BOTH PHASES OR THE INTERFACE. THIS DIFFERS NOT IN DOPANTS SOLUBILITY IN EACH PHASE DUE TO A LOCAL DIFFUSIVE FLUX UNTIL CHEMICAL POTENTIAL EQUALIZES

\hookrightarrow INTERFACIAL DOPING PILEUP EFFECTS

IT HAS BEEN OBSERVED THAT DOPANTS MAY PILEUP IN A VERY NARROW INTERFACIAL LAYER BETWEEN Si AND SiO₂. THIS PILEUP BURST IS SEPARATED FROM ANY SEGREGATION LAYER CAN BE MONOLYTIC AND ALL ATOMS IN THAT LAYER ARE ACTIVE. BECAUSE OF AMOUNT OF INTERFACIAL DOSE LOSS CAN BE SIGNIFICANT FRACTION OF THE DOSE OR DOPANTS THAT ARE USED THIS EFFECT CAN TAKE ON A DOMINANT ROLE IN DETERMINING THE CRITICAL CHARACTERISTIC OF THE DEVICE.

DIFFUSION KNOWS AN ATOMIC SCALE VIEWPOINT

+ POINT DEFECTS AND DOPANT DIFFUSION ARE STRONGLY LINKED

+ EASY TO THINK THAT A VACANCY ADJACENT TO DOPANT PROVIDES MECHANISM FOR THE DOPANT TO HOP TO ADJACENT SITES THIS REFLECTING A SINGLE MIGRATION STEP FOR THE DOPANT ATOM (THIS HAPPENS IN METALS WHICH FULL OF VACANCIES)

+ EASY TO THINK SILICON INTERSTITIAL MIGHT "WALK OUT" A SUBSTITUTIONAL DOPANT ATOM KNOW HIS LATTICE SITE AND BRINGING IT TO QUICKLY DIFFUSE DOWN FORM NEARLY OPEN CHANNELS IN SILICON LATITICE.

+ DOPANT AND A SILICON ATOM COULD SHARE A LATTICE SITE AND BY MOVING IN THIS BOND DIRECTION COULD MIGRATE AS A BOUND PAIR THROUGH THE LATITICE. THE PAIR INTRASTITIAL-DOPANT MIGRATES AS A MOBILE SPECIES THROUGH THE LATITICE BREAKS THE PAIR BREAKS UP LEAVING THE DOPANT IN SUBSTITUTIONAL SITE AND AN INTRASTITIAL. THIS PROCESS IS REFERRED AS INTRASTITIAL ASSISTED DIFFUSION.

L OXIDATION ENHANCED DIFFUSION

OXIDATION INSERT INTRASTITIAL AND CONSUMES VACANCIES SO SPECIES THAT TENDS TO HAVE AN INTRASTITIAL ASSISTED DIFFUSION WILL DIFFUSE FASTER THAN OTHER VACANCY-ASSISTED WILL DIFFUSE LESS.

PENETRATING TO MOVE WITH I OR V DEPENDS ON THE SIZE OF THE DOPANT. ELASTIC INTERACTION BETWEEN A POINT DEFECT AND A DOPANT DEPENDS ON THE MISMATCH OF SIZE SO THAT A LARGE DOPANT MAY PREFER TO MIGRATE WITH VACANCY moving WITH SMALL WITH INTRASTITIAL. B, P INTRASTITIAL Sb VACANCY NITURATION OF THE SURFACE HAS OPPOSITIVE EFFECT OF OXIDATION. THIS CAN BE NORMALIZED WRITING AN EQUILIBRIUM IN THESE CONDITIONS $\frac{f_I}{f_V}$ INTRASTITIAL/VACANCY, TYPE CONCENTRATION AND $C_{V/I}$ VACANCY/INTRASTITIAL CONCENTRATION

$$D_{eff} = D^* \left(f_I \frac{C_I}{C_I^*} + f_V \frac{C_V}{C_V^*} \right)$$

- ATOMIC SCALE DIFFUSION

WE CAN CONSIDER A DOPANT A INTERACTING WITH AN INTRASTITIAL I AS $A + I \rightarrow AI$ WITH AI INTRASTITIAL ASSISTED MOBILE SPECIES. IF WE CONSIDER THAT REACTION TO BE IN EQUILIBRIUM ($C_{AI} = k(C_A C_I)$) WE CAN DERIVE THE FOLLOWING EXPRESSION THAT LEADS TO UNK MACRO-MICRO SCOPIC PARAMETERS

$$\frac{\partial C_A}{\partial t} = \frac{\partial}{\partial x} D_A^* C_A \cdot \frac{C_I}{C_I^*} \left[\frac{\partial}{\partial x} \ln \left(C_A \frac{C_I^*}{C_I} \frac{n}{m} \right) \right]$$

- MEASUREMENT METHODS

Lb SIMS SECONDARY ION MASS SPECTROSCOPY
USED TO MEASURE THE CHEMICAL CONCENTRATION OF DOPANTS (CHEMICALLY REACTIVE!) SPECIAL SIMS TIPS ARE INCORPORATED IN THE Layout DURING PROCESS DEVELOPMENT. THIS ARE SPUNTED BY AN ION BEAM AND SPUNTED ATOMS TYPICALLY COLLECTED FROM A PROBE. SPUNTED ATOMS SO THAT ARE NOT IONIZED AND EXCITED AND MASS ANALYZED AND COUNTED. SINCE ONLY SMALL KINETIC OF SPUNTED ATOMS AND ANOTHER IONIZED ION BEAM IS CHOSEN TO HAVE HIGH ION YIELD.

Lb SPOTTING RESISTANCE

CUT THE SAMPLE AT A SHALLOW ANGLE AND USE A PAIR OF METAL PINCHES TO COUNT THE RESISTANCE DOWN IN THE BULK. IMPORTANT THAT THE TIPS HAVE GOOD ELECTRICAL CONTACT WITH SURFACE AND DO NOT PENETRATE THE BULK. IF TIP IS TOO SHARP MICROSPONTANEOUSLY MAKES BAD CONTACT IF TIPS TOO ROUGH IT PENETRATES DEEP INTO THE SUBSTRATE AND MEASURES THE RESISTANCE OR CREATE UNWANTED ZONES.

THIS MEASURES ONLY THE REACTIVELY ACTIVE DOPANTS DETERMINING WHETHER THIS AND SIMS GIVES US UNACTIVE DOPANTS CONCENTRATION.

Lb SPOT RESISTANCE ALREADY DESCRIBED BEFORE

ION IMPLANTATION

- DORMANT IONS ARE ACCELERATED TO HUNDREDS OR THOUSANDS VOLTS OR KILOGRAY AND SHOTCHED INTO A PERFECT SILICON LATTICE CAUSING A CASCADE OF DAMAGE THAT MAY DISPLACE THOUSANDS OF SILICON ATOMS FOR EACH IMPLANTED ION. SUBSEQUENT ANNEALING REDUCES THE DAMAGE.

ION IMPLANTER (MACHINE)

f SOLID SOURCE OF MATERIAL VAPORIZED OR GAS SOURCE USED TO DELIVER MATERIAL TO ION IMPLANTER (SOLID SOURCE GOOD SINCE AMOD GIVING MATERIAL CAN BE VAPORIZED AND IMPANNED)

f GAS ROOM IS IONIZED BY ENERGETIC ELECTRONS COMING FROM ARC DISCHARGE OR HOT FILAMENT USUALLY ALSO A MAGNETIC CIRCUIT IS ADDED SO THAT ELECTRON HAS GLASS TRAJECTORY TO INCREASE IONIZATION PROBABILITY.

+ EXIT SLOT SHAPES THE ION BEAM WITHOUT ACCELERATED ATOMS ENTERING INTO AN ANALYZER CHAMBER WITH A MAGNETIC FIELD B PERPENDICULAR TO ION MOTION SO THAT

WE CAN WRITE THE MOTION EQUATION OF IONS AS $\frac{m v^2}{R} = q v \cdot B$ SINCE IONS MOVE IN CIRCULAR SHAPE DUE TO B WITH A RADIUS R AND A VELOCITY v AND DUE TO THE CONSTRAINED OF ENERGY CONSIDERING THE IONS ACCELERATED BY A POTENTIAL DIFFERENCE

$$V_{\text{ext}} = \frac{1}{2} m v^2 = q V_{\text{ext}}$$

SO FOR A FIXED MAGNET DESIGN AND A FIXED OF THE RESOLVING APERTURE IN THE MACHINING TUNING THE ANALYZER MAGNET CURRENT WILL CAUSE DIFFERENT MASS ATOM TO BE SEPARATED

f FOR MOST SITUATIONS IONS ARE ACCELERATED TO THEIR FINAL ENERGY OF IMPLANTATION

f ION PATH ELECTROSTATICALLY DEVIATE IN ORDER TO COLLECT ALL NON IONIZED ATOMS THAT CONTINUES UNDEVIATED.

f IMPANT DOSE CALCULATED BY LOCATING THE FOCUS IN A FARADAY CUP WITH COLLECTING CURRENT AND INTEGRATES OVER TIME (NORMALIZED DOSE GIVEN BY $Q = \frac{1}{A} \int \frac{I}{q} dt$ I COLLECTS BEAM CURRENT AND A IMPLANTED AREA).

f WAFERS CAN BE MECHANICALLY MOVED ON ION BEAM PATHS THROUGH ELECTROSTATIC DEFLECTION PLATES.

- TEMPERATURE RISE IN SILICON CAUSED BY ION IMPLANT. ENERGY DEPOSITED IS $E_{\text{dep}} = \sqrt{IIdt} = VId$ IMPANT T IS ABOUT 120°C WHILE THE PHOTORESIST CAVES.

- INCREASES THE DOSE MEANS LONGER IMPLANT TIME OR HIGHER BEAM CURRENT.

- ION IMPLANTATION IS A RANDOM PROCESS BECAUSE IONS FOLLOW RANDOM TRAJECTORY. IF DIFFERENT IONS IMPLANTED AT SAME ENERGY HEAVY IONS STOP AT SHALLOW LENGTH

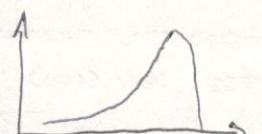
- DISTRIBUTION OF ION IMPLANTATION CAN BE DESCRIBED AS A GAUSSIAN $C(x) = C_p \exp\left(-\frac{(x-R_p)^2}{2\Delta R_p^2}\right)$ WHERE R_p IS THE PROJECTED RANGE (AND IT'S DEPENDENT ON IMPLANTATION ENERGY BIGGER IS BETTER HIGHER R_p) AND ΔR_p IS THE SPREAD OF IONS, STANDARD DEVIATION, (BIGGER WITH BIGGER DOSE) AND C_p DENOTE CONCENTRATION OF GAUSSIAN. WE CAN DEDUCE THE TOTAL DOSE IMPLANTED AS $Q = \int_{-\infty}^{+\infty} C(x) dx = \sqrt{\pi} \Delta R_p C_p$ AND SO $C_p = \frac{Q}{\sqrt{\pi} \Delta R_p}$

- DEFINING THE THICKNESS OF THE MASK AS X_m TO HAVE THE CORRECT DOSE Q OVER THE MASK ON A CORRECT MASK PROPERTY WE CAN CALCULATE THE TOTAL DOSE THAT PASSES THROUGH THE MASK AS $C_p = \frac{Q}{Z} \exp\left(\frac{X_m - R_p}{\sqrt{2} \Delta R_p}\right)$

- IF APPLIED A GAUSSIAN IMPLANT WE HAVE A T ANNEALING THE GAUSSIAN DISTRIBUTION WILL DISSESS AS IN THE ROLLING FORMULA $C(k, t) = \frac{C}{\sqrt{2\pi(\Delta R_p^2 + 2\Delta t)}} \exp\left(-\frac{(k-R_p)^2}{2(\Delta R_p^2 + 2\Delta t)}\right)$ WITH ALL PROBLEMS RELATED TO DIFFUSION ALREADY DISCUSSED

- ION IMPLANT IS SIMILAR TO GAUSSIAN ONLY NEAR THE PEAK TO HAVE A BETTER DESCRIPTION OF THIS SHAPE WE NEED HIGHER ORDER MOMENTS R_p IS FIRST ORDER ΔR_p SECOND ORDER LINE SMOOTHNESS THAT

MOMENTS R_p IS FIRST ORDER ΔR_p SECOND ORDER LINE SMOOTHNESS THAT IS III ORDER OR KURTOSIS FOURTH ORDER (SKW ASYMMETRY, KURTOSIS TAILNESS)



CHANNELING EFFECT

Crystalline structure of silicon plays important role. Ions can kind open channels in the silicon lattice and travel a long way inside the crystal beyond their stops. Effect or channeling on implant is to cause tails that continues much further than expected. To avoid this effect 3 solutions: tilt the sample, add grain small silicon dioxide (that is amorphous) or implant some amorphous silicon on top.

- STOPPING MECHANISM.

+ IONS SCATTER DETERMINISTICALLY FROM TARGET ATOMS THROUGH ANGLES DETERMINED FROM CLASSICAL TWO-BODY COLLISION THEORY SLOWING DOWN BY AN ADDITIONAL DRAG FORCE FROM ELECTROSTATIC INTERACTIONS PLUS AT WHICH IONS LOSE ENERGY DUE TO BOTH FROM NUCLEAR SCATTERING AND ELECTRONIC STOPPING POWER GIVING $\frac{dE}{dx} = -N [S_n(E) + S_e(E)]$ N SILICON DENSITY S STOPPING POWERS, I_k IS THE KNOWN RANGE OF IONS CAN BE DETERMINED AS $R_s = \int^R dx = \frac{1}{N} \int^R \frac{dE}{S_n(E) + S_e(E)}$

+ NUCLEAR STOPPING

Can be modeled as a Coulomb scattering with a potential modified to account for nuclear shielding effect $V(r) = \frac{q_1 q_2}{4\pi \epsilon_0 r} \phi(r)$ q_1, q_2 ATOMIC NUMBERS ANALOGUE FOR HEAD ON COLLISION MAXIMUM ENERGY TRANSFERRED IS $T_f = \frac{4 M_1 M_2}{(M_1 + M_2)^2} E$ WHERE E IS THE IMPACT ENERGY SO $S_n(E)$ DEPENDS ON ION ENERGY. SMALL AT HIGH E BECAUSE PARTICLES HAVE LESS INTERACTION TIME WITH SCATTERING NUCLEUS

+ NON LOCAL ELECTRON STOPPING

Major component of electronic stopping due to drag that moving ions experience in a dielectric medium.

Polarization of dielectric medium occurs around the atom to minimize the overall electric field. As the ion is set in motion polarization field must adjust by realignment of electrons with it at sufficient ion velocity causing the polarization field to lag behind charged ion leading to a drag force moving the ion. It's analogous with particles moving part in a viscous medium where viscosity is caused by sea or boundary. Drag is proportional to ion velocity and acts as dissipative energy loss.

+ LOCAL ELECTRONIC STOPPING

Collision with electrons and subsequent motion transfer reducing ion energy. This can also alter the ion trajectory although this effect is minor compared to nuclear stopping deviation. Also this depends on ion velocity. Charge we can write $S_e(E) = k/E$

- DAMAGE PRODUCTION

To cause enough pair need 15eV GeV ion that can be thousand. Some recombination occurs within the cascade due to segmentary diffusion hops in 10^{-9} time scale after damage has been produced.

Some defects generated can be recombined with defect from other cascades so the damage accumulation on the existing local defect density. The amount of damage accumulated depends on N of defects generated in an isolated cascade on the fraction that recombines within cascade and overlapping cascades N local existing defect density and N_d the threshold defect density where N/N_d is considered annealed $\Delta n_{\text{tot}} / n_{\text{tot}} = 1 - \frac{N}{N_d}$. Note $N/N_d \Delta n = 0$ if amorphous no defect since no crystal.

DAMAGE PRODUCTION IS MAXIMUM WHEN NUCLEAR ENERGY LOSSES HIGHEST

- SOLID PHASE EPITAXY (SPE)

If Si: amorphized during implantation crystalline structure can be reconstructed through SPE. Use of the undamaged substrate as seed. It's a quick process for (100) even easier if substrate is doped (easy annihilation of defects and activation). Activation $P_s = 20$

- DAMAGE ANNALING

Two steps. First step annealing around 400°C where vacancy clusters break up and annihilate with interstitial; final result is remove all dumbbell pairs leaving only interstitial type defects. These defects result in an excess (dopant) atom added so +1 monol. Interstitial of "f" condense in rod shaped defects upon further annealing at $T > 400^{\circ}\text{C}$. This occurs on $\{311\}$ planes. This can be compounded upon further annealing by evaporation of S-I monolayers of the defect. Larger defect easy to form dislocation loops that are difficult to remove.

Dislocation in depletion region or pn junction can cause damage currents particularly if they become decorated with metal impurities.

- To activate atoms annealing is roundabout. High implant damage difficult to activate (I competes with B for sites and B-I inactive couple can be created) within low ion implant also low $T \approx 600^{\circ}\text{C}$ and on

- TRANSIENT-ENHANCED DIFFUSION (TED)

Burst of diffusion many thousand times faster than what is normally observed for similar anneals where no implant damage is present. It's dominant effect that determines junction depth in shallow p-n-junction. Basic model assumes that all damage annihilates rapidly leaving only \pm interstitial pair dopant atom with dopant atom occupies a substitutional site. $\{311\}$ clusters forms rapidly and remains stable for long during TED by emitting I and shrinking TED duration inversely proportional with T .

- EFFECT ON DEVICES

PLSD reverse short channel effect gradient of interstitial profile toward gate oxide cause change dopant to piled up under the gate increasing V_{TH} for short gate lengths.

18

1947 1948 1949 1950 1951 1952 1953 1954 1955 1956 1957 1958 1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975 1976 1977 1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 20100 20101 20102 20103 20104 20105 20106 20107 20108 20109 20110 20111 20112 20113 20114 20115 20116 20117 20118 20119 20120 20121 20122 20123 20124 20125 20126 20127 20128 20129 20130 20131 20132 20133 20134 20135 20136 20137 20138 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202020202020206 202020202020207 202020202020208 202020202020209 2020202020202010 2020202020202011 2020202020202012 2020202020202013 2020202020202014 2020202020202015 2020202020202016 2020202020202017 2020202020202018 2020202020202019 2020202020202020 2020202020202021 2020202020202022 2020202020202023 2020202020202024 2020202020202025 2020202020202026 2020202020202027 2020202020202028 2020202020202029 20202020202020200 20202020202020201 20202020202020202 20202020202020203 20202020202020204 20202020202020205 20202020202020206 20202020202020207 20202020202020208 20202020202020209 202020202020202010 202020202020202011 202020202020202012 202020202020202013 202020202020202014 202020202020202015 202020202020202016 202020202020202017 202020202020202018 202020202020202019 202020202020202020 202020202020202021 202020202020202022 202020202020202023 202020202020202024 202020202020202025 202020202020202026 202020202020202027 202020202020202028 202020202020202029 2020202020202020200 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ETCHING

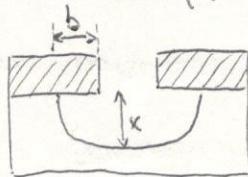
- Etch selectivity is the ratio of etch rates of different materials in an etch process.
- Etch directionality is a measure of the relative etch rates in different directions. Isotropic etching occurs when etch rates are the same in all directions both vertical and horizontal typically. Anisotropic etch is when we have more vertical etch than horizontal (commonly anisotropic no etch in horizontal directions). More physical etch being anisotropic and less selective.
- Etch process should be uniform, safe to use and should cause minimal damage to structures on the chip.

- WET ETCHING

Immersing wafer into baths of liquids chemicals exposed rich could be etched away. Wet etchants work by chemically reacting with the film to be water soluble byproduct or gases.

Etch selectivity defined as $S = \frac{V_1}{V_2}$ where V etch rate of material 1 or 2. Being the material we want to etch will define $S > 1$. Selectivity for the material to be etched w.r.t. the mask important gives us the mask thickness so that it's not completely removed.

Most chemical etch isotropic with exception to those which are sensitive to crystallographic orientation ($\langle 111 \rangle$ direction). The length 'b' in figure it's called etch bias.



Some overetch is always done to ensure that etch goes completion everywhere this ensures that within some structures may be overetched no parts remain unetched. Due to this practice it's found mental the selectivity to the substrate.

- PLASMA ETCHING

Wet etch replaced with plasma etch for 2 reason 1) more vigorous etch due to formation of reactive chemical species 2) possible directional etching

Typical RF-powered plasma etch uses like PECVD, both chemical and ionic species have a role in etch. The electrode (without wafer) is usually shaped to have higher fields to maintain current continuity (higher RF current density)

f) CHEMICAL ETCHING

Done typically by free radicals (electronically neutral species that have incomplete bonding so highly reactive) that react with the material to be etched. The byproducts should be volatile species that leaves the surface exposing more material to be reacted. This component etch isotropically due to 2 main causes: 1) Uniform angular distribution ($\cos^0 \theta = 1$) 2) Low sticking coefficient. The process is very selective.

f) PHYSICAL ETCHING

Positive ions accelerated towards each electrode. Staying on wafer surface results in physical component of etching. Flux of atoms ion toward the wafer is much more bidirectional because of the directionality of E . It is usually assumed that all ions move \perp to wafer surface, meaning it very large in cosine distribution.

⚠️! One ion reaches the surface it does not stick to the surface because (or if with low E so nothing happens) so sticking coefficient ≈ 1 .

Ions etch material by physical sputtering. Some chemical reaction can occur if ionized species are reactive.

f) ION-ENHANCED ETCH

CHEMICAL AND PHYSICAL SPECIES WORK IN A SINERGETIC MANNER. MORE THAN A SIMPLE SUPERPOSITION OF EFFECTS. IF CHEMICAL SPECIES INCREASED INCREASE VERTICAL ETCH AND NOT HORIZONTAL. CHEMICAL COMPONENTS AND PHYSICAL ONE IN THE PLASMA WORK TOGETHER TO GET THE MATERIAL WITH BOTH COMPONENTS REQUIRED AT ANY POINT TO WORK.

GOOD SELECTIVITY AND GOOD ANISOTROPY

Why? - CHEMICALLY INERT RESIDUE IS OFTEN FORMED AND DEPOSITED ON THE SURFACE THIS LAYER INHIBITS CHEMICAL ETCHING BY PHYSICALLY BLOCKING THEM AND BY REACTING WITH THEM MAKING THE REACTIONS POOR. THIS PASSIVATION LAYER IS REMOVED (ONLY ON BOTTOM WALL) BY ION BOMBARDMENT LEADING TO VERY ANISOTROPIC ETCH. ION BOMBARDMENT USING SIDEWALLS INHIBITOR TO PROTECT AGAINST LATERAL ETCHING.
Typically PROFILES LOOK IN FIGURE ↗

- PLASMA ETCH SYSTEMS

- BARREL ETCHERS

NAME FOR IT'S SHAPE. NO IONIC BOMBARDMENT EXCITING DOWNGEY CHEMICAL SO VERY SELECTIVE AND VERY LITTLE DAMAGE FROM THE SURFACE. HIGH THROUGHPUT DUE TO CLOSELY STACKED WAFERS.

ETCH UNIFORMITY NOT GOOD BECAUSE OF LONG DIFFUSION PATH FROM OUTSIDE TO INNER PART OF WAFER.

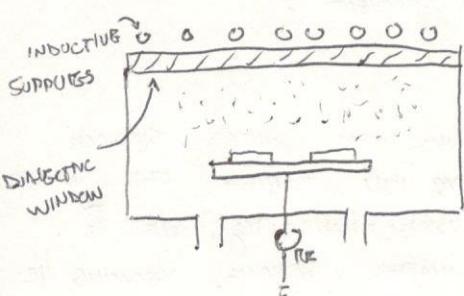
LIMITED TO NONCONICAL SPHERES OR PHOTOABST RETRACTION SIMILAR TO DOWNSIDE PLASMA ETCHERS WHERE PLASMA IS

CONTAINED IN ONE CHAMBER AND NEGATIVE SPHERES DIFFUSE IN ANOTHER CHAMBER WHILE WAFERS ARE ALSO CALLED AFTER GLOW RETCHERS USED FOR NON-MASKED PROCESS USING NITRODE REMOVAL AFTER LOCOS PROCESS.

- PARALLEL PLATE ETCHERS

VERY SIMILAR TO PECVD SYSTEMS EXCEPT THAT ETCH GASES ARE USED INSTEAD OF DEPOSITION GASES. MUCH BETTER ETCH UNIFORMITY THAN BARREL ETCHERS AND ALLOWS FOR ION BOMBARDMENT TOO. 2 OPERATION REGION : PLASMA MODE SYMMETRICAL ELECTRODES LEADS TO POOR ION BOMBARDMENT DUE TO SMALL SIGNAL VOLTAGE DROP AT WAFER SURFACE, HIGH REACTIVE ION BOMBARDMENT ASymMETRIC PLATES GUARANTEES ION-IMBALANCED BOMBARDMENT

- HIGH DENSITY PLASMA SYSTEMS



PLASMA DENSITY AND ION ENERGY DECREASED BY AN IGNITION OR PLASMA USING ECR (ELECTRON CYCLOTRON RESONANCE) OR ICP (INDUCTIVELY COUPLED PLASMA) SYSTEM. WE CAN ACHIEVE HIGH ION DENSITY AND LOW ION BOMBARDMENT.

ION BOMBARDMENT DAMAGE CAN BE kept LOW WHILE MAINTAINING HIGH ETCH RATES AND GOOD ANISOTROPIC ETCH

- SPUTTER ETCHING ONLY SPUTTERING COMPONENT USED (NOT USE IN INDUSTRY)

WITH CHEMICALLY INERT ATOMS AS ARGON WITH HIGH ENERGIES
- ION MILLING : CONFINED PLASMA USED TO GENERATE IONS TITAN GIDS TO ACCUMULATE IONS THE TEAM CAN ALSO BE FOCUSED (USE FOR MASK ABALING AND TEM STAMPING PROTECTION)

- END POINT DETECTION : USING OPTICAL EMISSION SPECTROSCOPY A SPECIFIC WAVE-

- LENGTH RELATING TO A REACTANT OR REACTION PRODUCT CAN BE FOCUSED (THIS AVERAGE OVER A LARGE SURFACE IT'S NOT A PUNCTUAL MEASUREMENT)
- PLASMA ETC+ ISSUES
 - + LOADING EFFECT ETC+ RATE DEPENDS ON LOCAL PLASMA DENSITY THAT COULD BE NON UNIFORM
 - + μ-LOADING EFFECT STRUCTURES WITH DIFFERENT MASK OPENING OR ASPECT RATIOS ARE ETCHED WITH DIFFERENT ETCH RATES (SMALL ETC+ FOR HIGH ASPECT RATIOS). CAN BE DUE TO: DEPOSITION OR TRAPPING OF REACTANTS SPECIES, DISTORTION OF ION PATH DUE TO CHARGING, SHADOWING EFFECTS
 - + OTHER ISSUES MAY BE MICRO TRAPPING DUE TO ION PHYSICAL DEFLECTION (F_z) RESIST & SPOTTING AND ION TRAJECTORY DISTORTION DUE TO RESIST CHARGING, WE CAN ALSO INCUR IN RADITION DAMAGES

ETCHING MODELS

- + LINEAR ETC+ MODEL CHEMICAL AND IONIC COMPONENTS ACTS INDEPENDENTLY AND COMBINE IN A LINEAR FASHION. SO WE GET ETC+ RATE = $(S_c V_f F_c + V_i F_i) / N$ N IS THE DENSITY OF THE FILM TO BE ETCHED F_i ION FLUX S_c STICKING COEFFICIENT F_c CHEMICAL FLUX V_f , V_i REACTIVE RATE CONSTANT FOR THE TWO FACTORS. IN PRACTICE V_f USED AS FITTING PARAMETER FOR THE PURELY CHEMICAL ETCHING AND V_i IS ION INDUCED ETC+ YIELD.

- ION ENHANCED MODEL WE NEED A MODEL WHERE THE REACTANT COMPONENT IS FUNDAMENTAL, IF ONE IS MISSING THE ETC+ RATE HAVE TO GO TO 0 AND IF ONE IS MUCH MORE THAN THE OTHER ETC+ VELOCITY HAS TO SATURATE TO A UNIT VALUE (ACCORDING TO LANGMUIR ABSORPTION THEORY) THE NUMBER OF REACTIVE NEUTRAL SPECIES THAT ABSORB ON THE SURFACE TO REACT WITH SURFACE MATERIAL IS $C = S_c (1 - \theta) F_c$ θ IS THE FRACTION OF SITES COVERED BY BY PRODUCTS AND F_c FLUX OF SPECIES ON SURFACE.

- | REACTIVE NEUTRALS CONTAINED IN BYPRODUCTS REMOVED PER TIME PER AREA BY ION BOMBARDMENT AND | $I = V_i F_i$ |
|---|---------------|
| ASSUMING STEADY STATE CONDITION WE DRAVE $\theta = 1 / [1 + \frac{V_i F_i}{S_c F_c}]$ | |
| THE ETC+ RATE IS THE FLUX OF REMOVED SPECIES DIVIDED BY THE DENSITY OF THE FILM TO BE ETCHED SO | |
| ETC+ RATE = $\frac{1}{N} \cdot 1 / \left[\frac{1}{V_i F_i} + \frac{1}{S_c F_c} \right]$. | |
| WE SEE 2 EVENTS BEING IN SERIES AND NOT IN PARALLEL. THE PROCESS IS LIMITED BY SLOWEST OF THE 2 PROCESSES | |

- OTHER AND POINT DEFLECTION FOR THIN-FILM CAN BE INTERFEROMETRY.
- ETC+ RATE DEPENDENCE AND QUITE COMPLICATED BUT IN GENERAL:
 - ① DEPENDS ON GAS SPECIES
 - ② INCREASING POWER INCREASES THE ETC+ RATE
 - ③ INCREASING PRESSURE DECREASES THE DENSITY BUT INCREASES CHEMICAL FLUX, DEPENDENCE ON PRESSURE NOT EASILY PREDICTABLE
 - ④ LOW RATE CAN BE INCREASED TO SUPPLY MORE REACTANT SPECIES BUT HIGH FLOW RATE CAN DECREASE TOO MUCH THE RESIDENCE TIME, FLOW RATE HAS MINOR IMPACT.
- ETC+ PROFILE CAN BE CONTROLLED BY:
 - INCREASING ION BOMBARDMENT (SO POWER)
 - USING DIFFERENT REACTANT GASES TO CONTROL BYPRODUCTS REACTIONS.



Back-end Technology

- Back-end refers to the interconnect layers, contacts, vias, and dielectric layers that bring active devices into specific circuit configurations.
- It can be divided into: local interconnects (silicided gate transistors and silicided active regions like source and drain regions), contacts (connect silicide/local interconnects to first level of metal), intermediate or global interconnect (metal lines wiring active elements into circuits), dielectrics (insulating different metal levels and lines), vias (same as contacts but connects metal lines together).

Silicides

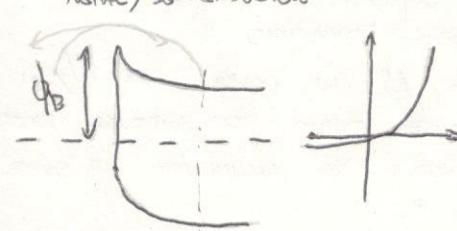
- Used as local interconnections in 2 ways: on top of polysilicon layer they form "polycide", on top of source and drain regions and as independent local interconnect.
- In polycide silicidation degrades the sheet resistance of the polysilicon gate and local interconnect while maintaining the good properties of the polysilicon/Si_x interface, in source drain region degrades sheet resistance of the diffused layers.
- Silicides used because they provide low electrical resistivity status at high T (good since no implanted GaAs) good process compatibility with silicon easy to etch and provides good contacts with other materials and having low electromigration probabilities.
- Two ways of forming silicides:
 - + Direct deposition from a composite target, cosputtering from two targets / co-sputtering from 2 targets or CVD also deposited with metal
 - / Reaction method: a.) deposit metal upon amorphous Si & then annealing process so that Si and metal react to form silicide and unreacted metaletched away
b.) No Si deposited but metal only deposited and then anneal so that it will react only when it's on silicon target etch away the unreacted part (it's a self-aligned process) self aligned silicide on silicide
- For both methods annealing process needed
- Very popular silicide is TiSi_x that has a high resistivity phase "C19" that forms at moderate temperature. We have to convert it to "C54" phase with an anneal at 800°C with low resistivity characteristics.
- Narrow width salicidation and compatibility with shallow junctions are main issues in salicidation process

Contacts

- Metal/semiconductor can in general be rectifying or ohmic. Because ideally it's a strong function of metal work function and so in theory it could be possible to choose a metal which produces small ϕ_B ; in practice impossible due to other constraints on metal (low resistivity) and the surface states induced pinning or from metal at the surface. So generally high ϕ_B for n-doped Si and low for p-type.
- If we use a low doped Si the barrier creates a depletion region that we don't want in our contact. Instead we use a high doped Si the depletion zone becomes narrow to up near the Fermi-Nordheim tunneling current to negligible levels so that our junction begins as a small resistance. Actually $\rho \propto \sqrt{N_D}$. In case of low doping thermionic current is type dominant term.

Measured ρ can be higher due to not clean interface, fewer dopants in Si at surface than desired due to segregation effects.

General requirements for MS-S/contacts are low resistance and good thermal



STABILITY

- Early circuits used only Al as contact material making contact with Si and heavily doped regions. Al makes good contact reducing native oxide and carbon impurities with an annual at 600°C. This in the ambient to "cage" also SiO₂. But solubility of Si in Al at 500°C is 1% meaning that Al in contact with Si wants to absorb the Si up to its solubility limit. This silicon does not diffuse by Al precipitates voids that are quickly filled by Al resulting in 0.2-0.3 μm of native oxide uniformly so creating spikes in Si or also 1 μm solutions to this problem is 1) use Al with already some silicon in it so that solubility requirement is already full-filled (but at less than T too much Si in Al and creates precipitates) 2) barrier layers to prevent or slow down any interaction with Si; passivating barrier layer has to be inert to both Si and Al and be good diffusion barrier as well (TiN is one example). TiN has good structure (L < 10 nm) this makes impingement to Si and most other species; chemically stable and inert with most species. Other layers usually first layer of Ti and then TiN to form also this silicide under all contacts now ruggedized with W plugs. With Al planarity remains an issue done by "damascene" process since first we deposit a usual dielectric that we then etch a hole in it and fill the surface with adhesion layer (TiN) then W deposition all over (CVD W gives much more conformality and filling of the contact w.r.t Al.) and finally CMP process to manage all.

- INTERCONNECTS AND VIAS

- Primary requirements are low resistivity, good adhesion to underlying films, stability during processing and operations and the ability to be etched and deposited in easy ways but noting T is low (600°C) and thermal expansion coefficient $\times 10$ than Si.
- Two phenomena happens in Al that are problems:
 - + hillock growth occurs when Al film is subjected to high compressive stresses. This stress easily causes by thermal expansion coefficient mismatch. Due to its polycrystalline structure and can melting point of Al and subjected to coating hillocks and voids resulting this stress position of Al and subjected to coating hillocks and voids. Can creates shorts between lines or open circuits. Hillocks can break or crack upper SiO₂ layers increasing probability of shorts. Solution is to add portion of Cu that in excess (over its solubility) segregates an precipitates on the Al grain boundaries without diffusion of Al is enhanced reducing this phenomena and avoiding hillocks or voids formation.
 - + electromigration: when electrical current flows through Al in order of mA/cm^2 electrons transfer enough momentum to Al atoms to cause them to diffuse (fastest along grain boundaries) and this can cause a build-up of aluminum in some regions and voids in others and so same problems or.
Because of Al diffuses mostly on grain boundaries electromigration is very dependent on grain structure, size and crystallographic orientation of grains. Adding Cu to Al slow down this process. Also multi-layer stacks and used Ti (helps controlling grain structure) + TiN (barrier during via processing) + Al+TiN (that can also limit metal line in case of void or cracks formation)

- DIELECTRICS

- First usage of dielectric separates active areas from first line of metal high intermetal dielectrics (IMDs) dielectrics that separates global interconnections
- Good electrical isolation low dielectric constant (so C_p low) high breakdown fields and low leakage as electrical characteristics. In addition good adhesion to Si

- NETAL AND SILICIDES, LOW INTRINSIC STRESS, GOOD THERMAL STABILITY, LOW DOPING DENSITY AND THEREFORE SHOULD BE PREFERRED TO HYDROGEN FOR THE FINAL Ti_x ANNEAL.
- SiO₂ OR PSG PHOSPHOSILICATE GLASS THAT IS SiO₂ DOPED WITH P USED (SiON).
 - ONE FOR BETTER PROPERTIES). USUALLY A THINNER LAYER USED BI-LAYERLY RATHER SiO₂ THAN PSG. PSG AS FIRST LAYER. (PSG HAS BETTER NUCLEATION AND SMOOTH COATINGS).
 - PECVD USED FOR OXIDE DEPOSITION SINCE IT USES ENERGY FROM PLASMA ENHANCES DEPOSITION NUCLEATION AND PROVIDES DENSE FILMS AND BETTER COATINGS AND RILUNG AT LOW T.
 - PLANARIZATION NEEDED TO DEPOSIT AL LINES. REFLUX OF PSG OR MENG COMMONLY CMP PROCESS.

- SCALING PROCESS

TIME OF A SIGNAL PROPAGATING INTO A LINE CAN BE DESCRIBED FROM DISTURBED MODEL (TIME FROM 10% TO 90%) AS $0.89 R_{\text{Cu}} L$. RESISTANCE OF A LINE IS R_{Cu} AND TIME CAPACITANCE AS $C = K_{\text{OK}} E_0 \frac{W}{L} + K_{\text{OX}} E_0 \frac{L}{W}$ WHERE K_{OK} AND K_{OX} ARE THICKNESS AND DIELECTRIC CONSTANT OF SiO₂ LS DISTANCE BETWEEN 2 LINES SO THE TOTAL DELAY WILL BE $\tau = 0.89 R_{\text{Cu}} E_0 \rho L^2 \left(\frac{1}{K_{\text{OK}}} + \frac{1}{K_{\text{OX}}} \right)$ R_{Cu} ADDED TO ACCOUNT FOR RADIATING FIELDS OR INTEGRATED CIRCUITS ABOVE OR BELOW MULTILAYER STRUCTURES DURING FWHM AS THE MINIMUM DIMENSION OF A LINE IN A TECHNOLOGY WE CAN SAY THAT K_{OK} & L ARE ALL EQUAL TO FWHM AND L REMAINS QUASI-CONSTANT SINCE DURING THE AREA OF THE CHIP (ACCUMULATING $L^2 = A$ THAT SLIGHTLY INCREASES) SO THE TIME $\tau \approx 0.89 K_{\text{OK}} E_0 \rho / F_{\text{FWHM}}^2$ WE NEED TO KEEP MATERIAL PROPERTIES AS GOOD AS POSSIBLE TO KEEP τ UNDER CONTROL.

- COPPER PROCESS

COPPER CANNOT BE DRY ETCHED BECAUSE BYPRODUCTS ARE NOT VOLATILE AND REQUIRES A DAMASCENE APPROACH

- SILICIDE GATES ON S/D REGIONS

SiO₂ REMOVED FROM SOURCES THAN Ti DEPOSITED BY SPUTTER ON WHOLE WAFER. FIRST ANNEAL STEP IN NITROGEN AMBIENT SO THAT WHEN Si IS EXPOSED WILL FORM TiSi₂ AND AT THE SURFACE TiN OVER SiO₂ ONLY TiN FORMS THIS LIMIT THE INTEGRAL GROWTH OF THE SILICIDE. SECOND ANNEAL AT HIGH T TO PASS FROM "C9" TO "C8" PHASE

- CONTACT FORMATION (DAMASCENE PROCESS)

OPEN UP HOLES IN FIRST METALLIC OR DIAMONICS TO FORM METAL CONTACT ANISOTROPIC PLASMA Etch USUALLY DONG (IMPORTANT THAT ALL DIAMONICS OR BYPRODUCT REMAIN TO OBTAIN GOOD CONTACT). BIGGING HOLE RILUNG AN ADHESION BARRIER IS FORMED WITH Ti (DEPOSITED IF SPUNTED NOT ALREADY PRESENT) ON BOTTOM OF HOLES. THEN TiN DEPOSITED AS A BARRIER LAYER TO PREVENT DIFFUSION AND SPILLING EFFECTS (TiN DONG BY SPUNTING OR CVD). ANNEALING IN N₂ OR O₂ AMBIENT TO IMPROVE TiN BARRIER PROPERTIES THEN AS FINAL STEP W IS DEPOSITED

- GLOBAL INTERCONNECTS

USUALLY MADE WITH Al WITH 0.5-1% Cu ALSO Si IS ADDED EVEN IF SPILLING IS NO LONGER A PROBLEM. Al LAYERS USUALLY CVD WITH TiN Ti OR TiN LAYERS. SURFACES MUST BE CLEAN TO ENSURE GOOD CONTACT PROPERTIES

- # LITHOGRAPHY
- A LIGHT SENSITIVE PHOTONIC IS SPUN ONTO THE WAFER FORMING A THIN LAYER AT THE SURFACE. RESIST FABRICATION SELECTIVELY EXPOSED BY ILLUMINATING LIGHT THROUGH A MASK AND PABN DEVELOPING COMPOUNDS THE PATTERN TRANSFERRED TO THE WAFER.
- GENERALLY CRITICAL DIMENSION (CD) CONTROL IS REQUIRED TO BE +/- 10% OF THE SMALLEST FEATURE SIZE.
- ABOUT 1/3 OF OVERALL COST OF A WAFER IS DUE TO LIO.
- PATTERNS THAT COMBINE THE VARIOUS LAYERS IN AN INTEGRATED CIRCUIT ARE DESIGNED WITH CADS. ONCE THE DESIGN IS COMPUTED THE INFORMATION FOR EACH MASK LAYER IS TRANSFERRED TO A MASK MAKING MACHINE (E-BEAM OR LASER PATTERN GENERATOR).
- MASK IS FUSED SILICA PLATE COATED WITH THIN LAYER OF CHROMIUM AND A LAYER OF PHOTONIC. LASER OR E-BEAM EXPOSURE RESIST WAFER IS THEN DEVELOPED AND USED AS RETICLE MASK TO REMOVE EXCESS CHROMIUM. OSGA
- Usually mask magnified x1 to x5 dimension lateral magnification will be provided by lens system. No defects on mask or yield rapidly to a mask circuit and repair (done with additional Cr or with e-beam) fundamental. Mask protected by contamination or dust particles with a thin transparent Mg membrane on the chromium side or the mask on a metal frame. Particle designed to fall out of focus and so not transferred in wafer.
- PATTERN INFORMATION TRANSFERRED ON WAFER WITH PROJECTION EXPOSURE SYSTEM. LIGHT FROM HIGH INTENSITY SOURCE COLIMATED AND PASS THROUGH THE MASK. Only few chips printed during one exposure.
- + WAFER PHYSICALLY MOVED TO NEXT EXPOSURE FIELD AND PROCESS REPEATED AS STEP AND REPEAT TOOLS OR STEPPER
 - + IMAGE SET OR LIGHTS BY LIGHT SOURCE SYSTEM AND MASK AND WAFER SIMULTANEOUSLY SCANNED TOGETHER SO THAT IMAGE IS SCANNED ALONG THE WAFER AS SCANNER
- JOB OF EXPOSURE TOOL BEST AREAL IMAGE AS POSSIBLE IN TERMS OF RESOLUTION, EXPOSURE FIELD, DEPTH OF FOCUS, UNIFORMITY ...
- JOB OF PHOTONIC TO TRANSFER AREAL IMAGE IN BEST 3D NEARLY IN TERMS OF GEOMETRIC ACCURACY, EXPOSURE SPEED, RESIST RESISTANCE TO SUBSEQUENT PROCESSSES.
- ## - LIGHT SOURCES
- HIGH RESOLUTION LIO USES SHORT WAVELENGTH PHOTONS. WAVELENGTH STRONGLY CONCENTRED TO DIFFRACTION EVENTS THAT LIMITS OUR TECHNOLOGY NOWADAYS
- ARC LAMPS AS DOMINANT LIGHT SOURCE USUALLY CONTAINING Hg VAPOUR INSIDE SEALED GLASS ENVELOP. Arc is struck between electrodes applying enough voltage to ionize the gas that one of ionized behaves like a plasma.
- LIGHT EMISSION BY TWO PROCESSES: 1) FREE ELECTRONS HAVE HIGH ENERGY AND EMIT BLACK BODY RADIATION BUT WITH WAVELENGTH DEEP IN ULTRA VIOLET SO THIS RADIATION IS ABSORBED BEFORE EXIT THE LAMP BY WALLS 2) Hg IONIZATION EXCITE DUE TO COLLISION AND HOP ON DEFECTS AND EMISSION ENERGY USES SHOOTING PHOTONS AT DESIRED WAVELENGTHS IN UV RANGE.
- Most STEPPERS USE SINGLE WAVELENGTH BY FILTERING UNWANTED ONE (OPTICAL SYSTEM EASY TO DESIGN WITH SINGLE WL.) TWO COMMONLY USED g-LINE 436 nm AND 365 nm i-LINE
- ## - EXPOSING SYSTEMS
- ~~CONT~~
- CONTACT DUVING MASK PLACED FLAT SIDE DOWN IN DIRECT CONTACT WITH WAFER; OR SPINNING WAFER THROUGH MASK. ALIGNMENT DONE prior to EXPOSURE WITH MICROSCOPE AND MASK A LITTLE SEPARATED FROM WAFER.

DIFFRACTION EFFECTS MINIMIZED AND MACHING INEXPENSIVE BUT HAS CONTACT
RESULT IN DAMAGE OF BOTH MASK AND RESIST LEADING TO HIGH DEFECT DENSITY

- PROXIMITY PRINTING

SOLVES THE ISSUE OF DEFECTS WITH GAP 5-25μm BUT THIS SEPARATION DEGRADATES RESOLUTION DUE TO DIFFRACTION EFFECTS. RESOLUTION LIMIT $\approx \sqrt{\lambda}$ OF GAP λ WAVELENGTH. BOTH CONTACT AND PROXIMITY REQUIRES XL MASK NOT EASY TO MANUFACTURE.

- PROJECTION PRINTING

HIGH RESOLUTION WITHOUT PROBLEMS OF CONTACT PRINTING. MASK SEPARATED FROM WAFER AND OPTICAL SYSTEM USED TO IMAGE THE MASK ON WAFER. RESOLUTION LIMITED BY DIFFRACTION LIMIT, OPTICAL ZOOM IN X4 X5 ONLY SMALL PORTION ON WAFER IS PRINTED. FOCUSING LENS COVERS ONLY PART OF DIFFRACTION PATTERN SO INFORMATION IS LOST.

- RESIST PROCESS 1) ACTUAL IMAGE FORMATION ON TOP OF RESIST LAYER 2) LATENT IMAGE FORMATION INSIDE RESIST AND AT EXPOSED AREAS 3) RESIST DEVELOP EXPOSED AREAS TO RADIATION BECOMES SOLUBLE TO DEVELOPER.

- PHOTONICIST

- PHOTORESIST MATERIALS DESIGNED TO RESPOND TO INCIDENT PHOTONS BY CHANGING THEIR PROPERTIES WHEN EXPOSED TO LIGHT. MATERIAL THAT CONTAINS AND MAINTAINS A LATENT IMAGE OF THE IMPRINTING PHOTONS UNTIL THE RESIST IS DEVELOPED.

- ALMOST ALL RESIST HYDROCARBON BASED MATERIALS, WHICH THIS MATERIAL ABSORBS LIGHT ENERGY FROM PHOTONS BREAKS CHEMICAL BONDS AND THE MATERIAL RESTRUCTURES IN A MORE STABLE FORM.

POSITIVE RESISTS: LIGHT-EXPOSED REGIONS BECOME MORE SOLUBLE IN DEVELOPER (BUTTERY)

NEGATIVE RESISTS: LIGHT-EXPOSED REGIONS BECOME HARDER AND INSOLUBLE (BAD RESOLUTION)

- SENSITIVITY MEASURES HOW MUCH LIGHT IS REQUIRED TO EXPOSE THE RESIST. HIGH SENSITIVITY INCREASES THE THROUGHPUT OF LITHO PROCESS. SUPER SENSITIVITY ALSO CAN LEAD TO UNSTABILITY OF THE MATERIAL AND THERMAL AND DUE TO SHOT NOISE OR LIGHT

- RESOLUTION IMPORTANT ISSUE SINCE NOWADAYS WE ARE LIMITED BY ACTUAL IMAGE AND DIFFRACTION PROBLEMS

- "RESIST FUNCTION" DESCRIBES THE NEED FOR PHOTONICIST TO WITHSTAND BAKING OR ION IMPLANTATION. NEEDED A GOOD ROBUSTNESS TO THIS PROCESSES.

- G AND I-LINK PHOTONICIST USUALLY DONB BY 3 COMPONENTS: INACTIVE RESIN USUALLY HYDROCARBON RESIN THE BASIC OF THE MATERIAL, A PHOTOACIDIC COMPOUND (PAC) ALSO HYDROCARBON AND SOLVENT TO ADJUST VISCOSITY.

DUV RESISTS REPLACE PAC WITH PHOTO-ACID GENERATOR (PAG) WHICH ACTS AS CHEMICAL AMPLIFIER.

MOST OF SOLVENT REMOVES DURING SPINNING AND PREBAKING ONCE ACTIVATING EXCITANTS

- G/I-LINK RESISTS

MOST COMMON AND DON MATERIALS. PACS AND DIAZOQUINONES THE ROLE OF PACS IS TO INHIBIT DISSOLUTION OF THE MATERIAL IN THE SOLVENT WITHIN EXPOSED TO LIGHT PACS CHEMICALLY CHANGES AND STABILIZES ITSELF REMOVING A CARBON ATOM WITH AN OXYGEN ATOM COVALENT BONDED WITH IT.

- DUV RESISTS DENG ULTRA VIOLET

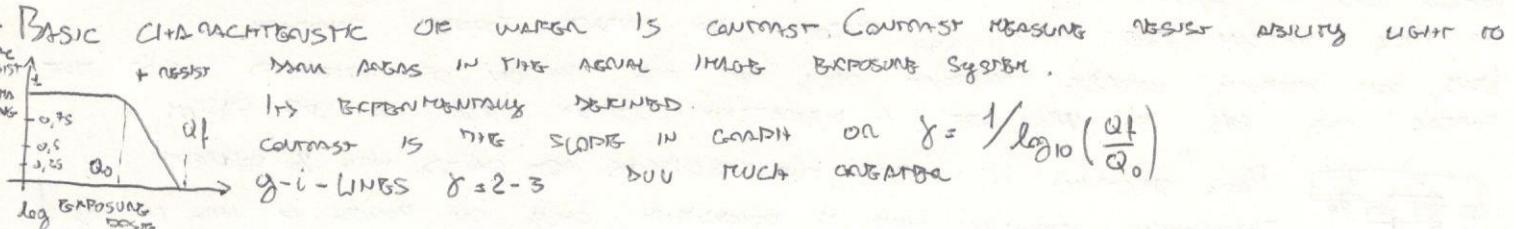
DQN HAS 2 PROBLEMS 1) FOR WAVELENGTHS BELOW I-LINK RESIST STRONGLY ABSORBS INCIDENT PHOTONS MAKING DIFFICULT THE REACTION TO HAPPEN INSIDE THE RESIST 2) LOW SENSITIVITY DUV BASED ON CONDUCTING DIFFERENT CIRCUITRY BASED ON CHEMICAL AMPLIFICATION RESIST (CAR). SENSITIVITY INCREASE BY FACTOR 3. INCIDING PHOTONS REACTS WITH PHOTO-ACID-GENERATOR PAG CREATING AN ACID MOLECULE THIS ACIDS ACTS AS CATALYSTS DURING SUBSEQUENT RESIST POST BAKE TO CHANGE RESIST PROPERTIES. REACTION IN POST BAKE.

KEY POINT REACTION AND CATALYTIC ACID MOLECULE NEGATIVELY AND MAY PARTICIPATE WITH HUNDREDS OF REACTIONS.

POST-EXPOSURE BAKE (PEB) HEAT PROVIDES ENERGY NEEDED FOR REACTION AND MOBILITY TO ADD TO FIND NEW MOLECULES TO REACT WITH DURING PEB.

OPTIMAL SENSITIVITY AND RESOLUTION.

TIME DELAY BETWEEN EXPOSURE AND POSTBAKING CAN CREATE AMMING CONTAMINATION THAT



- PROCESS STEPS

- WAFER CLEANING AND HEATING TO DRY OFF ANY WATER VAPOR ON SURFACE
- ADHESION PROMOTER APPLICATION HMDS MOST COMMON SUBSTANCE FOR THIS PURPOSE
- SPINNING OR RESIST IMMEDIATELY AFTER HMDS APPLICATION. UNIFORM WAFERS WITH HIGH RESIST ACQUISITIONS AND SO HIGH SPIN. SPINNING PRODUCES "EDGE BEAD" THAT IS THICK RESIST ON GOGG OR WAFER THAT HAS TO BE REMOVED BEFORE PROCEEDING
- LITHOGRAPHY CONSISTING SOLVENT INCUBATING RESIST ADHESION AND REGULAR EQUILIBRIUM STATES PRESENT IN PHOTONIST
- EXPOSURE CREATES LARGEST IMAGE (REQUIRED TIME DEPENDENT ON THICKNESS AND LIGHT INTENSITY)
- POST EXPOSURE BAKING IN ORDER TO MINIMIZE STANDING WAVES EFFECTS
- DEVELOP (TIME DEPENDENT ON T REGULATED CONCENTRATION)
- POST-BAKING DONE AT HIGH T IN ORDER BAKES TO HARDEN FINE PHOTONIST

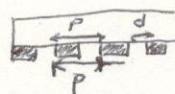
- THERMAL REFLUX IN ORDER TO REDUCE FEATURE DIMENSIONS PHOTONIST CAN BE PROCESSED WITH CONTINUED THERMAL PROCESS THAT SHRINKS DIMENSIONS
- NOTCHING: DUE TO SUBSTRATE NON-MIRRORS OBSCURE REFLECTIONS CAN IMPACT NON EXPOSED REGIONS
- STANDING WAVES: SUBSTRATE REFLECTIVITY THIN FILM INTERFERENCE IS PRESENT WITHIN THE RESIST THICKNESS CAUSING A "SCALLOPED" EDGES RESIST ANTI-NOTCHING LAYER AS SOLUTION
- REGISTRATION: PRINCIPAL ALIGNMENT USEFUL TO LEVEL CRUCIAL FOR DEVICE TUNING. SPECIAL STRUCTURES (ALIGNMENT MARKS) ARE GENERATED. DEDICATED FEATURING BOX AND USED TO EVALUATE MUTUAL ALIGNMENT BETWEEN 2 MASK AND ALIGNMENT SYSTEM USE MARKS TO CALIBRATE ITSELF

- RESOLUTION ENHANCEMENT TECHNIQUES (IN PROJECTION LIO)

- IF THE DIMENSIONS OF AN OPTICAL SYSTEM ARE ALL LESS THAN THE WAVELENGTH OF THE LIGHT WE CAN ASSUME THAT LIGHT CAN BE TREATED LIKE PARTICLES TRAVELING IN STRAIGHT LINES. IN OUR CASE THIS ASSUMPTION FAIL AND WE HAVE TO TAKE INTO ACCOUNT THE WAVE NATURE OF LIGHT
- DIFFRACTION HAPPENS BECAUSE LIGHT DO NOT TRAVEL IN STRAIGHT LINES, SHIELLED APERTURE MEANS WIDGER SPREAD OF THE LIGHT BECAUSE THERE ARE USES WAVES ALONG TO PASS THROUGH THE APERTURE AND THIS WIDE SPATIAL PROPAGATION RESULTS BEYOND THE APERTURE
- BECAUSE OF ITS FINITE DIMENSIONS FOCUSING LENS COLLECT ONLY A PART OF TOTAL DIFFRACTION PATTERN ASSOCIATED WITH LIGHT PASSING THROUGH THE APERTURE.
- IN PROJECTION SYSTEMS UNDERRING DIFFRACTION ON THE RIGID DIFFRACTION HAPPROPS.
- NUMERICAL APERTURE NA: DEFINING IT AS THE INDEX OF REFRACTION OF THE MATERIAL BETWEEN OBJECT AND LENS (USUALLY $n=1$) AND OF THE MAXIMUM HALF ANGLE OF THE DIRECTED LIGHT THAT CAN ENTER THE LENS (MAY BE LIMITED BY PHYSICAL SIZE OF LENS) WE DEFINING NUMERICAL APERTURE AS $NA = n \sin \alpha$ THAT DETERMINES THE NUMBER OF BIREFRACTION ORDERS THAT CAN BE OBTAINED AND THUS THE QUALITY OF THE IMAGE RECONSTRUCTED. INCREASING NA HIGH PATTERN RIDGEY CAN BE OBTAINED.

OBJECTIVE LENS (FOR COHERENT IMAGING) FUNCTION IS TO RECONSTRUCT THE DIFFRACTION PATTERN AND TO FOCUS IT ON THE WAFER, SINCE MASK SPECTRUM IS THE PUPIL TRANSFORM OF THE PATTERN LENS NEEDS TO PERFORM AN INVERSE FOURIER TRANSFORM.

LENS CAN PERFORM INVERSE TRANSFORM ONLY IN THE PUPIL OF DIFFRACTED LIGHT THAT BENDS THE LIGHT SO WE GET A DIFFRACTION LIMITED SYSTEM SO LPIE SYSTEM



MASK SPECTRUM IS DISCRETE THE FREQUENCIES ARE SPACED WITH $\frac{1}{p}$ SEPARATION

THEORETICAL RESOLUTION LIMIT IS DEPENDENT ONLY ON PUPIL P AND NOT BY d UNDER THIS SAME λ WITH FEATURE PITCH GETS SMALLER ($p \propto \lambda$) THE DIFFRACTION ANGLE BECOMES LARGER FOLLOWING THE FORMULA $\sin \phi = h \lambda / p$ WITH ϕ ANGLE OF DIFFRACTED RAY AND h INTEGRAL NUMBER

- WHEN MASK IS ILLUMINATED FROM LIGHT TRAVELLING IN VARIOUS DIRECTION WE HAVE A PARTIAL COHERENT IMAGE. THE IMAGE CAN BE CALCULATED BY ADDING IMAGES ARISING FROM ALL INCIDENT LIGHT SOURCES. WE DEFINING $\sigma = \frac{\sin \phi}{\pi d}$ PARTIAL COHERENCE \rightarrow ANGLE WRT \perp OF MASK AT WHICH LIGHT ARRIVES

- FOR A COHERENT ILLUMINATION WE GET A RESOLUTION OF ($\sigma=0$) $R_c = \frac{\lambda}{NA^2}$

FOR PARTIALLY COHERENT ILLUMINATION $R_c = \frac{1}{2} \frac{\lambda}{NA(1+\sigma)}$

- MODULATION TRANSFER FUNCTION (MTF) USED TO DETERMINE THEORETICAL RESOLUTION OR MTF OF OPTICAL IMAGING. FOR $\sigma=0$ SYSTEM CAN CAPTURE FREQUENCY UP TO NA/λ FOR $\sigma \leq 1$ SYSTEM ABLE TO RESOLVE UP TO $(1+\sigma)NA/\lambda$

- IMAGE CONTRAST IS INDEX OF AVERAGE INTENSITY AT WAFER LEVEL $C = \frac{I_{MAX} - I_{MIN}}{I_{MAX} + I_{MIN}}$

- DEPTH OF FOCUS IS MAXIMUM AMOUNT OF CHANGE (IN \perp DIRECTION) THAT CAN BE TOLERATED BEFORE PRINTED PATTERN SIZE FALES OUTSIDE OF SPECIFICATIONS THAT WITH THE EXPOSURE CRITERIA CAN BE EXPRESSED AS $DOF = \frac{\lambda}{2NA^2}$

- $\left\{ \begin{array}{l} R_c = \frac{\lambda}{NA} \\ DOF = \frac{\lambda}{2NA^2} \end{array} \right.$ THIS CONSIDERING NEAR SYSTEMS AND RESIST RESPONSE. K_1 MEASURES LITH AGGRESSIVENESS DEPENDS ON RESIST LENS AND EXPOSING TOOLS K_2 DEPENDENT ON FEATURES SHAPE CONFIGURATIONS...

- RESOLUTION ENHANCEMENT TECHNIQUES (RET)

- OFF-AXIS ILLUMINATION (OAI)

FILTERING SPATIAL FREQUENCIES ($\frac{1}{p}$) USEFUL TO RECONSTRUCT IMAGE AT WAFER LEVEL AND ASSURE MAXIMUM CONTRAST BECAUSE DC BACKGROUND LIGHT IS MINIMIZED. ILLUMINATION SHAPE MUST BE CUSTOMIZED DEPENDING ON CAVITY RESONANCES TO BE PRINTED

- ATTENUATED PHASE-SHIFT MASKS (ATT-PSM)

DESTRUCTIVE INTERFERING BETWEEN LIGHT TRAVELLING IN THE QUARTZ AND IN THE SHIFTER, MATERIAL IS USED TO ENHANCE AVERAGE IMAGE CONTRAST WRT COHERENT MASKS NO CHROME BUT SEMI-TRANSPARENT LAYER THAT PHASE-SHIFT

- OPTICAL PROXIMITY CORRECTIONS (OPC)

OPCS MAKE SUCH RESOLUTION CHANGES IN THE SHAPE OF THE PATTERN ON THE MASK TO COMPENSATE EFFECTS OF CURRENT WAVELENGTHS AND FEATURE SIZE THAT LOCATES AROUND CORNERS AND SPACER LINES

- ALTERNATIVE LITH TOOLS

- IMMERSION LITHOGRAPHY HAS THE ADVANTAGE OF $n > 1$ SINCE IN WATER $n=1.33$. FURTHERMORE FOR A GIVEN DIRECTION OVER THE ANGLE OF THE LIGHT INSIDE THE FLUID WILL BE USES WRT AIR. SMALL ANGLE MEANS SMALL OPTICAL PATH DIFFERENCE AND SO BETTER DEPTH OR FOCUS

- ELECTRON BEAM DIRECT WRITING

PROS: ALREADY KNOWN TECHNOLOGY $\lambda \approx 0.1 \text{ nm}$ SO LOW DIFFRACTION EFFECTS AND NO NEEDS OF MASK

CONS: HIGH PROXIMITY EFFECT (ELECTRONS HAVING A LOW PERCENT STOPPING EXPOSING UNWANTED AREA)

BRINGING LOW THROUGHPUT AND COULOMB REPULSION BEAM USE EFFECTIVE IC
- EXPOSURE UV (EUV)
SIMILARITY WITH OPTICAL LITO: R AND DOK SCANS WITH NA AND λ USE OF REDUCTION OPTICS
SUPPORT OAI PSM AND OPC EMPLOY STEP AND SCAN SYSTEMS
DIFFERENCES VISUAL SHORT λ ABSORBED BY ALL MATERIALS, VACUUM OPERATION USES NEGLIGIBLE
PARTICLES WITH PARTIAL ABSORBERS AND REQUIRES REFLECTING OPTICS. CHALLENGES IN TOOLS
RESIST AND MASK PROPERTIES

- NANO IMPRINTING LITO (CONTACT PRINTING)
IDENTICAL TO PRODUCTION OR PSM BUT WITH 1:1 DIMENSIONS SO NANOCONTROL AND POSITIONING
IS CRUCIAL

- THE EFFECTS OF REDUCING DIMENSIONS ON THE LENS NAMES A LPR SO WE ARE LOSING HIGH F
COMPONENTS OF THE DIFFRACTION PATTERN. LOST INFRAS RESULTS IN ABERRATION IMAGES WITH
ROUNDERS COMING SHORTENING OF LENGTHS AND NARROW LINEAR FEATURES.
THIS EFFECTS CAN BE PREDICTABLE AND CAN BE COMPENSATED BY ADDING FEATURES
DIMENSIONS AND SHAPES TO THE MASK (OPTICAL PROXIMITY CORRECTION OPC)

- EJECTION BEAM LITO
E-BEAM USED FOR MANY YEARS IN MANUFACTURING. OPTIMAL RESOLUTION OBTAINED SINCE e HAVE
WAVELENGTH PROPERTIES HAVING λ LESS THAN 0.1 nm SO DIFFRACTION PROBLEMS ARE NON-LIMITING
Major DRAWBACK SMALL THROUGHPUT SINCE EXPOSURE NANO μ PIXEL TO PIXEL IN A SERIAL
PROCESS. THIS COMES FROM A NUMBER OF PROBLEMS: 1) e-BEAM CURRENT IS LIMITED BY
WEAVING MINIMUM NUMBER OF EJECTIONS TO WELL EXPOSE A PIXEL AND SO UPPER BOUND
TO VELOCITY 2) HIGH-BEAM INTENSITY, RESOLUTION CAN BE DEGRADED BY COULOMB REPULSION OF
CHARGED e IN BEAM 3) e WITH 10-20 keV ENERGY SCATTER WITH NUCLEI AND PANEL FOR
AT LEAST $1\mu m$ AND THIS CAN CAUSE EXPOSURE OF UNWANTED AREAS

- X-RAY LITO
WAVELENGTHS ORDER OF THM SO DIFFRACTION EFFECTS ARE NEGLIGIBLE BUT FOCUSING X-RAY
IT'S BIG ISSUE SO GENERALLY FOCUSING PRINTING SYSTEMS BASIC CONFIGURATION
X-RAY SOURCE AND OPERATED IN VACUUM AMBIENT.
VISUALLY GOOD RESOLUTION AND THROUGHPUT COMPAREABLE WITH OPTICAL SYSTEMS
ISSUES WITH MASK AND X-RAY SOURCE.
NO MATERIAL TRANSMIT X-RAYS BASICALLY SO CLEAR AREAS DON'T BEG LOW MASS MATERIALS
(Si₃Na) AND DARK AREAS LIVING Au OR W THAT STOPS X-RAYS. MASK LOT REQUIREMENTS AND
NECESSITIES CONSEQUENTLY MANUFACTURING CONTROL FOR STRESS ISSUES.

CMOS PROCESS FLOW

- INDIVIDUAL DEVICES DO NOT INTERACT WITH EACH OTHER EXCEPT THROUGH THEIR CIRCUIT INTERCONNECTIONS. WE NEED TO HAVE CERTAIN THAT INDIVIDUAL DEVICES ON CHIP ARE ELECTRICALLY ISOLATED FROM EACH OTHER. DONE BY LOCOS

- LOCOS

LOCALLY OXIDIZING SILICON SUBSTRATE PROCESS. LOCAL OXIDATION OF SILICON. THE REASON BEHIND THIS THICK SiO_2 LAYERS ARE CAUSED ACTIVE REGION WHERE WE WILL BUILD OUR MOS DEVICE. THIS IS AN INITIAL STEP.

WAFER IS COATED THAN THIN LAYER OF SiO_2 GROWTH AND DEPOSITION OF Si_3N_4 . Si_3N_4 CREATES LARGE COMPRESSIVE STRESS ON SUBSTRATE SO THE MAJOR REASON OF SiO_2 GROWTH FIRST IS TO RELIEVE THIS STRESS THAT CAN LEAD TO DAMAGE OF WAFER (SiO_2 CREATES STRESS IN OPPOSITE WAY BALANCING THE THICKNESS OF THE 2 WE CAN HAVE STRESS NUL). DEPOSITION OF PHOTORESIST AND EXPOSURE TO PATTERN LOCOS ZONES.

Si_3N_4 IS NOW DRY ETCHED USING PHOTORESIST AS MASK. RESIST STRIPPED OFF AND THEN AGAIN IN OXIDIZING AMBIENT IN ORDER TO USE Si_3N_4 TO STOP OXIDATION IN ACTIVE REGIONS AND TO OXIDIZE THIS UNWANTED PART (GROWTH OF SiO_2 INSIDE Si). AFTER THIS Si_3N_4 CAN BE STRIPPED OFF.

- POLY-BURIED LOCOS

NOW $\text{SiO}_2/\text{Si}_3\text{N}_4$ BOT THICK LAYERS SiO_2 - POLY SILICON - Si_3N_4 . PROCESS IS THE SAME POLY SILICON USED TO RELIEVE THE STRESS DUE TO Si_3N_4 . THIS OXIDATION EXTEND FOR SOME DISTANCE UNDER Si_3N_4 (BIRD'S BEAK) IN THE UN-WANTED ZONE AND THIS CAN CAUSE PROBLEMS AND NON-MANUFACTURABILITY.

- STI SHALLOW TRENCH ISOLATION

ELIMINATES BIRD'S BEAK PROBLEMS.

SiO_2 AND Si_3N_4 DEPOSITED (SOLVED RELATED ISSUES NO BIG PROBLEM NOW SINCE WE DON'T HAVE LONG HIGH-T OXIDATION BUT OBTAINNESS OF 2 LAYERS COMPENSATES STRESS). PHOTORESIST APPLIED EXPOSED AND DEVELOPED. NITRODE AND OXIDE LAYER ETCHED USING PHOTORESIST AS MASK. THEN TRENCHES ETCH THAT ARE 0.5 μm DEEP. WE CAN USE AGAIN PHOTORESIST AS MASK ON THE $\text{SiO}_2/\text{Si}_3\text{N}_4$ AND OXIDE. WE CAN USE AGAIN PHOTORESIST AS MASK ON THE $\text{SiO}_2/\text{Si}_3\text{N}_4$ AND OXIDE. IMPORTANT THAT TRENCHES WALLS ARE VERTICAL SO THERE IS LITTLE UNDERCUTTING LAYERS. UNDERRADICAL REGIONS. AFTER TRENCH DONE THERMAL GROWTH OF A NARROW OXIDE (THIN LAYER) TO HAVE GOOD Si/SiO₂ INTERFACE AND ROUND THE CORNERS THEN DEPOSITION OF OVER OR THICK LAYER OF SiO_2 BY CVD. NO VOIDS OR GAP IN TRENCHES IS FUNDAMENTAL. AFTER THIS CMP TO PLANARIZE ALL AND REMOVAL OF Si_3N_4 LAYER.

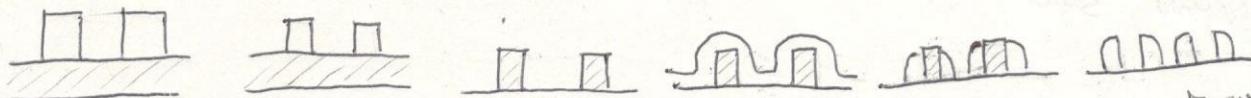
MEMORY PROCESS FLOW

- Objectives to be built on wafer are 3 : + floating gate transistors (memory cells) + low voltage transistors LV ROM P-MOS + high voltage transistors HV ROM P-MOS

- DOUBLE PATTERNING

- Possibility option to overcome resolution limits or LIO

POSITIVE DOUBLE PATTERNING: Photomask developed on a secondary layer with minimum size defined by thermal processes. Then pitch to transfer on mask on secondary layer. Deposition of a support material all over and then anisotropic etch to form spacers around second layers. Removal of this second layer and use of this spacers as mask for next process



NEGATIVE DOUBLE PATTERNING: until spacer formation then deposition of secondary layer all over plane. After then strip of spacers and

THE SAME OF POSITIVE APPROACH TO KILL GAPS AND DOLISH TO USE OR REMAINING AS MASK



- NEGATIVE APPROACH HAS BETTER DIMENSIONAL CONTROL ON SPACES (LINES AND SPACES) PAR WITH FIRST LIO PROCESS PAR WITH FILLING AND PUNARIZATION)

- Main drawback is there are necessary additional masks to cut the lines termination (that in positive approach occurs in a shot 2 by 2) or to print non pitch structures

- DOUBLE EXPOSURE: A mask with double pitch wrt the wanted one is exposed 2 times with the second exposure transposed of $\frac{1}{2}$ pitch wrt the first. Main drawback is that the LIO quality depends on the overlay of the 2 exposures

- Floating gate patterning (without self-aligned techniques) overlay is done to set floating gate on top of the right zone.

or

Si₃N₄ and Poly-CMP

L Poly - CMP

TOUGHEN

Si₃N₄ SiO₂ Si OXIDE CORROSION

GAPFILLING

WET SiO₂

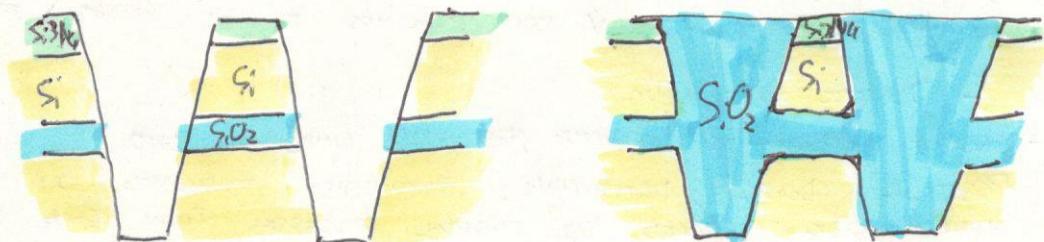
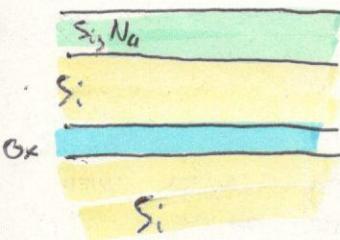
LIO

Si₃N₄ REMOVAL

~

Si₃N₄ SiO₂ Si

DEPOSITION



ROUNDING PROBLEMS DVS&B

- STRESS MEASUREMENT WITH MICRO Raman SPECTROSCOPY : STRESS ALTERS THE SILICON RAMAN SHIFT