Computer Architecture

Fall, 2020

Week 11

2020.11.23

組別：_____ 簽名：_____

[group1] (對抗賽)

1. Shown in the following Figure is a single-cycle implement of the MIPS processor, answer the following questions.

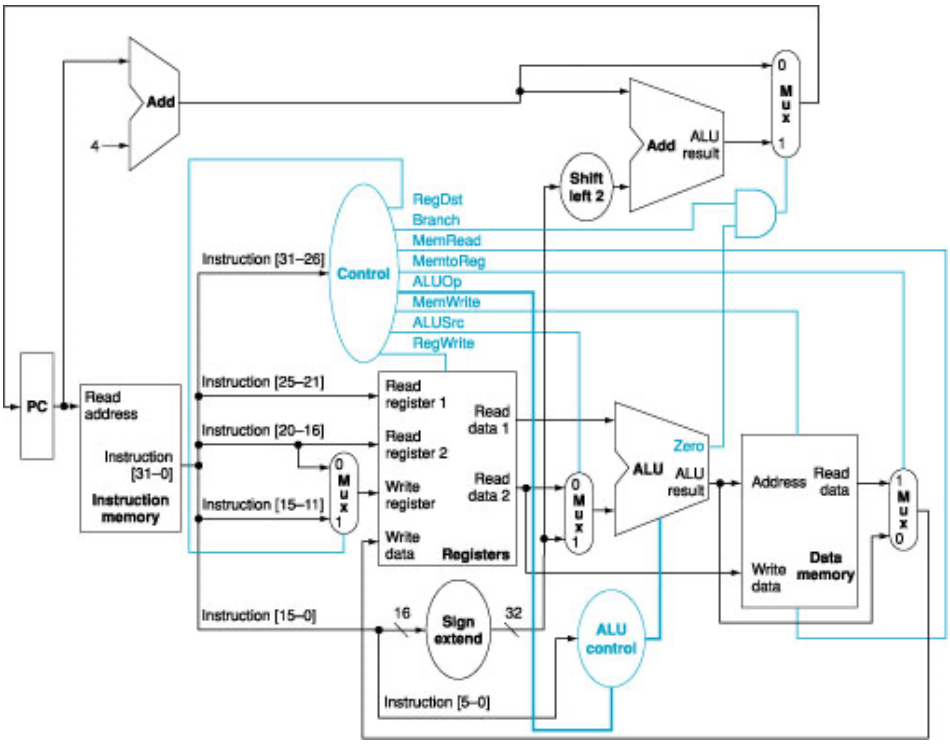
(1) What does “single-cycle” mean for this MIPS implement?

(2) What is the purpose of sending the value of PC register to an adder?

(3) What is the purpose of using multiple levels of decoding to generate the actual ALU control bits?

(4) What is the purpose of performing “Shift left 2” on the output bits of “Sign extend”?

(5) What is the purpose of sending the Zero signal of the ALU to AND gate?



Answer:

(1) In a single-cycle machine, an instruction is executed in one clock cycle.

(2) To increment the PC to obtain the address of the next sequential instruction (4 bytes later).

(3) Using multiple levels of control can reduce the size of the main control unit and may also potentially increase the speed of the control unit.

(4) To increases the effective range of the offset field of the branch instruction by a factor of 4.

(5) Zero output of the ALU, which is used for equality comparison, will need to AND together the control signal, branch, to determine a branch instruction is taken or not.

[group4] (對抗賽)

2. Please sort the steps of the Processor Design.

A. Assemble datapath
B. Assemble the control logic
C. Select set of datapath and establish clocking methodology
D. Determine control points
E. Analyze instruction

Answer:
ECADB

[group12] (對抗賽)

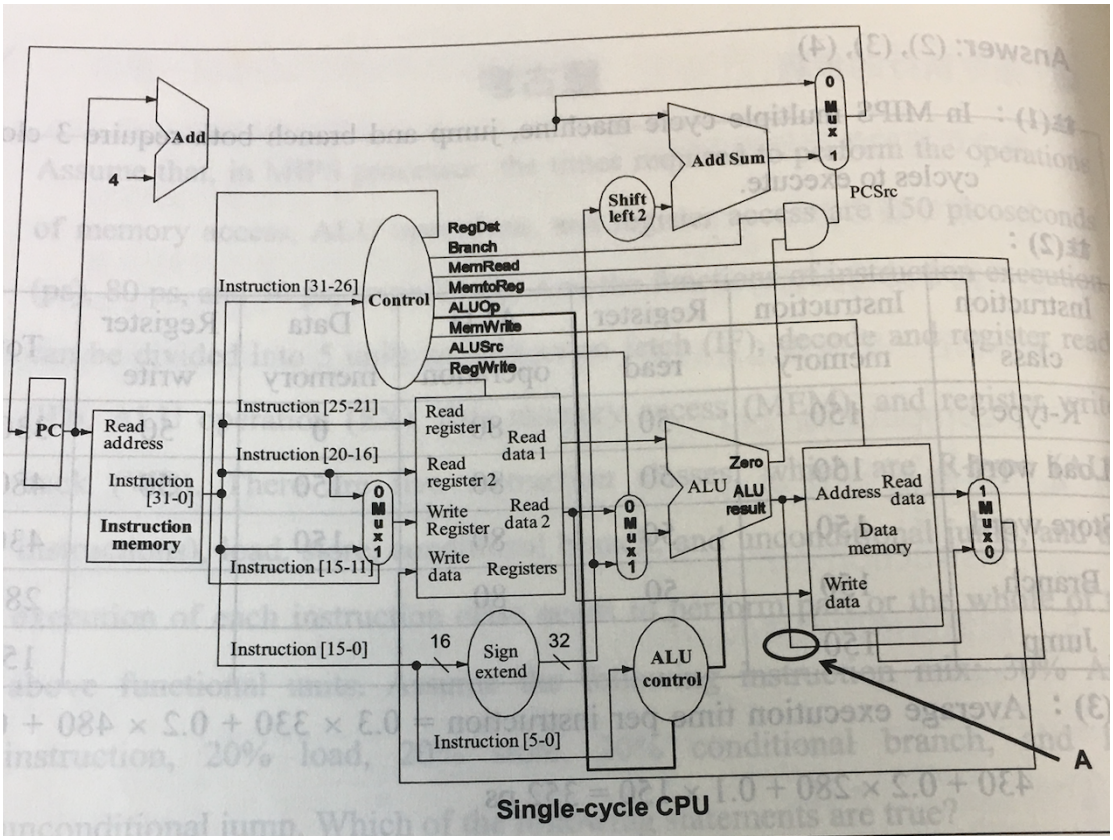
3. The single-cycle datapath conceptually described in this section *must* have separate instruction and data memories because：(pick the correct statement)

(a) The format of data and instructions is different in MIPS and hence different memories are needed.
(b) Having separate memories is less expensive.
(c) The processor operates in one cycle and cannot use a single-ported memory for two different accesses within that cycle.

Answer:
(c)

[group11]

4.



What instruction(s) below may fail to run correctly if the datapath labeled A in the single-cycle CPU figure has been cut?

(a) add (b) sw (c) lw (d) slt

Answer:

a, d

[group3] (對抗賽)

5. How can MIPS makes control easier？

(1) Immediates access from memory.

(2) Instructions same size.

(3) Operations always on registers / immediates.

(4) Source registers can store in different places according to users favor.

Answer:

2、3

[group13] (對抗賽)

6. Which of the following statements are true?

(a) The main job of the controller is to set the correct value at the correct control point.
(b) Whatever the type of instruction is, the opcode is always 6 bits in bits 31-26.
(c) ALU operation can be determined by the opcode directly.
(d) ALU Control (Local) needs 6 bits' function field and 2 bits' ALU op as input to produce 4 bits' ALUctr.
(e) In beq operation, ALUop will be 00.
(f) In the truth table for RegWrite, RegWrite = 1 will happen when opcode = 00 0000 or 10 1011. Therefore, RegWrite = R-type + lw.
(g) The drawback of single-cycle design is the cycle time for load is much longer than needed for all other instructions.

Answer:
A, B, D, G
(C) ALU operation needs a functional field and opcode to determine.
(E) In beq operation, ALU should be 01.
(F) RegWrite = 1 is when opcode = 00 0000 or 10 0011, not 10 1011.

[group2] (對抗賽)

7. Which of the following statements about single-cycle CPU are false, and why?

(a) The period of clock signal we used in single-cycle CPU can shorter than the longest propagation delay of the circuit.
(b) In a single-cycle CPU for MIPS instruction set, the next PC may depend on the result of ALU.
(c) In a single-cycle CPU for MIPS instruction set, control signal simply depends on opcode of the instruction.
(d) We use multiplexers to combine multiple data paths to a single one.

Answer:
(a) False, the period of clock signal we used in single-cycle CPU must be longer than the longest propagation delay of the circuit.
(b) True.
(c) False, it depends on opcode and function field of the instruction.
(d) True

[group6] (對抗賽)

8. Which of the following statement is/are true? explain if it's false.

(a) If (RegWrite AND Write-data-Port in register file) == 0, then no register would be modified.

ALUOP0 ALUOP1	ALU Src	Reg Dst	Mem Read	Mem Write	Branch	Mem toReg	Reg Write	Jump

(b) The control signals above can support all instructions to execute.

(c) Set the control signal "MemRead" always to be 1 would obtain the wrong result.

(d) beq instruction has the shortest delay.

Answer:

(a) When some register write to be 0, the statement still holds.

(b) bne is not supported.

(c) Even "MemRead" is always 1, "MemtoReg" will guarantee the result is true.

(d) Instruction jump has the shortest delay.