Computer Architecture

Fall, 2020

Week 16

2020.12.28

組別：_____ 簽名：_____

[group7] (對抗賽)

1. The CPU in a computer system uses two levels of caches L1 and L2 . Level L1 is accessed in one clock cycle and supplies the data in case of an L1 hit . For an L1 miss , occurring 4 % of the time , L2 is consulted . An L2 hit incurs a penalty of 10 clock cycles while an L2 miss implies a 100-cycle penalty

I. Assuming pipelined implementation with a CPI (cycle per instruction) of 1 when there is no cache miss , what is the effective CPI if L2's local mis rate is 25 % ?

II. Changing the mapping scheme of L2 from direct to two-way associative can improve its local miss rate to 20 % while its hit penalty is increased to 12 clock cycles due to the more complex access scheme . What is the effective CPI after this change ? Is this change a good idea ?

Ans :

I. The effective CPI = 1 +0.04 x 10+ 0.04 x 0.25 x 100 = 2.4

II. The effective CPI after change = 1 +0.04 x 12 +0.04 x 0.2 x 100 = 2.28 The change is a good idea .

[group12] (對抗賽)

2. Assuming a cache of 4K blocks, a four-word block size, and a 32-bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative, and fully associative.

Ans:

4-word (16 byte) per block, total (32-4) = 28 bits for tag and index

a. Direct mapped:

Number of sets = 4K, $log_2(4K) = 12$, number of tag bits = $(28 - 12) \times 4K = 64Kbits$

b. 2-way associative:

Number of sets = $4K/2 = 2K$, number of tag bits =$(28 - 11) \times 2 \times 2K = 34 \times 2K = 68Kbits$

c. 4-way associative:

Number of sets = $4K/4 = 1K$, number of tag bits =$(28 - 10) \times 4 \times 1K = 72 \times 1K = 72Kbits$

d. Fully associative:

Only one set, number of tag bits = $28 \times 4K = 112Kbits$

[group6] (對抗賽)

3. Tell the true or false above statements, and if the statements are false, why?
   A. In multilevel cache, L-1 block size larger than L-2 block size.
   B. Virtual memory is managed by CPU hardware
   C. Miss rate depends on memory access patterns.
   D. If you use virtual memory, you can run a program that the size is bigger than your actual main memory size.
   E. Process states include new, ready, running, waiting and terminated.

Ans:

F a. In multilevel cache, L-1 block size smaller than L-2 block size.

F b. Virtual memory is managed by CPU hardware and OS(Operation System)

T c. Miss rate depends on memory access patterns.

T d. If you use virtual memory, you can run a program that the size is bigger than your actual main memory size.

T e. Process states include new, ready, running, waiting *and terminated.*

[group5] (對抗賽)

4. True or False
   a. Miss rate with LRU policy is lower than miss rate with Random policy.
   b. Direct mapped cache has lower miss rate than 2-way-associative cache.
   c. It doesn't make sense to apply LRU policy on direct mapped cache.
   d. Different processes in OS might share same physical page frame.

A：

a. False, random might be better in some cases.

b. False, higher

c. True

d. True, this is what share memory does.

[group2] (對抗賽)

5. Assume that:

Instruction miss rate 3%

Data miss rate 5%

CPI without any memory stalls is 2

Miss penalty 40 cycles

25% of instructions are load & stores

Please determine how much faster a machine would run with a perfect cache that never missed.

Ans:

Instruction miss cycles = 3% * 40 = 1.2

Data miss cycles = 25% * 5% * 40 = 0.5

Total memory stall cycles = 1.2 + 0.5 = 1.7

Actual CPI = 2 + 1.7 = 3.7

CPU time with stalls / CPU time with perfect cache = 3.7 / 2 = 1.85

[group10] (對抗賽)

6. The following statements are true or false?

(a) OS transfer frames from disk to memory.

(b) When a process completes I/O or an event, it moves from waiting state to ready state.

(c) When a process is admitted, it moves to running state.

(d) Each program has its private physical address space holding its frequently used data.

(e) Virtual memory let program use spaces more than physical memory.

Answer:

(a) False. OS transfer pages from disk to memory.

(b) True

(c) False. It moves to ready state.

(d) False. Each program has its private virtual address space holding its frequently used data.

(e) True

[group9]

7. It's a 4-block caches, 2-way set associative, please implement table below:

   Block access sequence: 0, 9, 5, 1, 5, 7

   Use LRU method to choose the victim when the set is full.

Block Address	Cache index	Hit/Miss	Cache content after access			
			Set0		Set1	
0						
9						
5						
1						
5						
7						

Block Address	Cache index	Hit/Miss	Cache content after access			
			Set0		Set1	
0	0	Miss	mem[0]			
9	1	Miss	mem[0]		mem[9]	
5	1	Miss	mem[0]		mem[9]	mem[5]
1	1	miss	mem[0]		mem[1]	mem[5]
5	1	hit	mem[0]		mem[1]	mem[5]
7	1	miss	mem[0]		mem[7]	mem[5]

[group3] (對抗賽)

8. To improve cache performance with multi level cache,

   primary cache focus on (a)

   L-2 cache focus on (b) to avoid (c)

A:

(a) minimal hit time

(b) low miss rate

(c) avoid main memory access