Computer Architecture

Fall, 2020

Week 15

2020.12.21

組別：_____ 簽名：_____

[group1] (對抗賽)

1. 關於 write-through 和 write-back 的敘述，下列何者正確？

(a) 當 write hit 時，write-through 會將 cache 和 memory 的資料同時更新

(b) 當 write-back 的 dirty bit 為 1 時，代表 cache 裡沒有資料

(c) 在 cache 和 memory，Write-back 的資料是非同步的

(d) 當 write miss 時，對於 write-through 通常都是 fetch the block

Ans：**(c)**

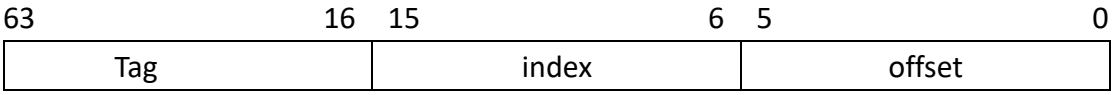
(a) 先存到 write buffer 再慢慢存回 memory / 理論上 write-through 會同時更新 cache 和 memory，但會因為 write buffer 出現些微 delay。

(b) cache 有被寫過資料

(d) write-back

[group14]

2. Consider a direct-mapped cache design with a 64-bit byte-address of the following format



What is the cache size in kibibytes (i.e. ,KiB) for the data storage?

Note that: 2**10 bytes=1KiB

Ans:

(2^10) * (2^6) = 2^6 KiB

[group6] (對抗賽)

3. Which following state is False

(a) DRAM access an arbitrary element of a sequence in equal time

(b) By memory Hierarchy, DRAM should be closer to the processor than SRAM

(c) We use cache controller to management Blocks between Cache and Memory

(d) Loop is a type of Spatial locality

(e) Caches are in the processor chip while the main memory are off the chip

Ans:

(b) SRAM is faster, so it should be closer to the processor

(d) Loop is a type of Temporal locality

[group8] (對抗賽)

4. We design a cache which size is 16KB, containing 4 words for a block. Note that one word is 4 bytes. If memory address are 32bits,

(a) How many blocks we have?

(b) How many bits we use in word offset depends on byte size? How many bits we use in block offset depends on word size?

(c) How many bits in cache index?

(d) How many bits in cache tag?

Ans:

(a) How many blocks Each cache have? 1024

16KB = 2^14 bytes = 2^12 words

2^12/2^2 = 2^10

(b) How many bits we use in Byte offset? in block offset? 2 bits ,2bits

One word = 4 byte ➔2^2

4 words for a block ➔2^2

(c) How many bits in cache index? 10 bits

1024^10

(d) How many bits in cache tag? 18 bits

32-10-2-2=18

[group11] (對抗賽)

5. Which statements are false?

(a) Block is the basic unit of information transfer

(b) Loop is an example of spatial locality

(c) Hierarchy between cache and memory is managed by hardware

(d) DRAM is slow, cheap, and dense while SRAM is fast, expensive, and not very dense

(e) Miss penalty is the time to deliver the block to the processor

Ans:

(B) temporal locality

(E) Miss penalty is the time to deliver the block to the processor + time to replace a block in the upper level

[group3] (對抗賽)

6. Which of the following statements are true? If the statement is false, please explain why.

(a) Random access means that access time is the same for all locations.

(b) DRAM is usually faster but more expensive than SRAM.

(c) There are two types of locality. One of them is spatial locality, for example: loop.

(d) Hit time = RAM access time + time to determine hit/miss

(e) Larger blocks always reduce the miss rate.

(f) On data-write hit, when we do write-back, data in cache and memory may be inconsistent.

Ans：(a) (d) (f) are true.

(b) SRAM is usually faster but more expensive than DRAM.

(c) loop is an example of temporal locality, not spatial locality.

(e) Larger blocks will not always reduce the miss rate.

[group12] (對抗賽)

7. According to following table (total 8 blocks, 1 word/block, direct mapped cache)

Index	Valid	Tag	Data
000	1	10	Mem[10000]
001	0		
010	1	10	Mem[10010]
011	1	11	Mem[11011]
100	0		
101	0		
110	0		
111	0		

1.

Complete the following table

Word address	Binary address	Hit/miss	Cache block
27	11011	Hit	011
7			
13			
26			

Ans:

Word address	Binary address	Hit/miss	Cache block
27	11011	Hit	011
7	00111	miss	111
13	01101	miss	101
26	11010	miss	010

[group4] (對抗賽)

8. In a certain system the main memory access time is 100 ns. The time to access the upper caches is 10 times faster than the time to access main memory. If the hit ratio in cache is 0.92, please compute the average time for the processor to read a data.

1*10 + (1-0.92)*100