Computer Architecture

Fall, 2021

Week 17

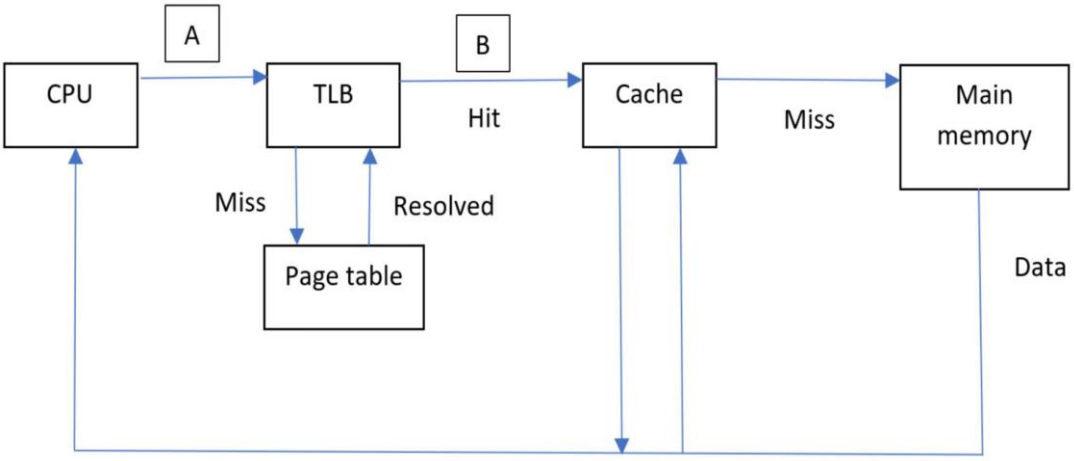
2021.1.4

Group:

組員簽名：_____

[group 14] (對抗賽)

1. Consider the following figure



(A) What is the name of the TLB's input (Symbol A in the figure)?

(B) What is the name of the TLB's output (Symbol B in the figure)?

(C) What is the name of this type of cache (with B as its input)?

(D) "We could have a hit in the cache, and get a TLB miss and a page table miss." Is the statement true (Yes or No)? Explain your answer.

(E) Consider the processor operating at 1 GHz. The processor stalls during a cache miss and has the following properties: (i) a cache access time of 2 clock cycles for a hit, (ii) a miss penalty of 100 clock cycles, and (iii) a miss rate of 0.03 misses per reference. Please compute the average memory access time.

Ans:

(A) Virtual address

(B) Physical address

(C) Physically addressed cache

(D) No page table miss → data are not in memory → data are not in cache

(E) Average memory access time = (2 + 0.03 x 100) x 1 ns = 5 ns

[group 9] (對抗賽)

2. Please fill the block below

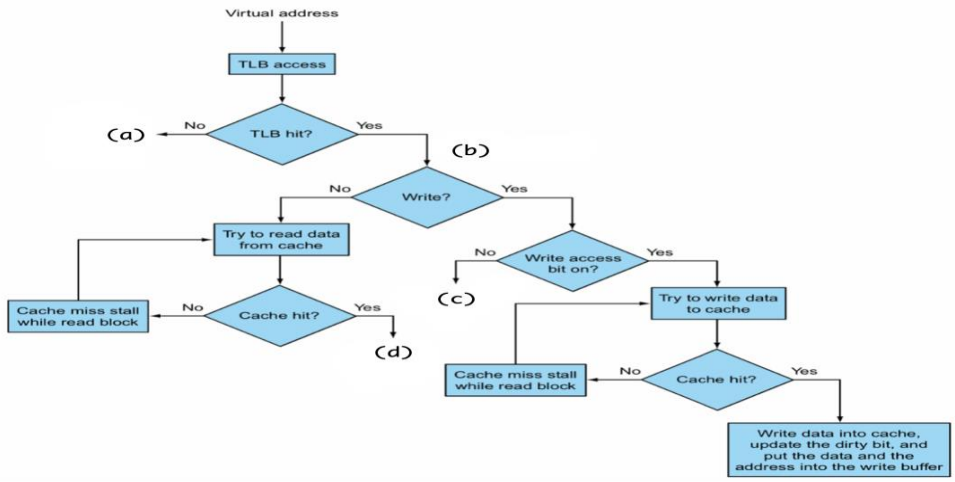
Cache	TLB	Page table	Possible?
Hit	Miss	Miss	
Miss	Hit	Miss	
Miss	Miss	Hit	
Hit	Hit	Miss	
Miss	Hit	Hit	
Hit	Miss	Hit	

Ans:

Cache	TLB	Page table	Possible?
Hit	Miss	Miss	Impossible
Miss	Hit	Miss	Impossible
Miss	Miss	Hit	Possible
Hit	Hit	Miss	Impossible
Miss	Hit	Hit	Possible
Hit	Miss	Hit	Possible

[group 6] (對抗賽)

3. Fill in the following blanks by: **TLB miss exception**, **Physical address**, **Write protection exception**, and **Deliver data to the CPU**.



Ans:

(a) TLB miss exception

(b)Physical address

(c)Write protection exception

(d)Deliver data to the CPU

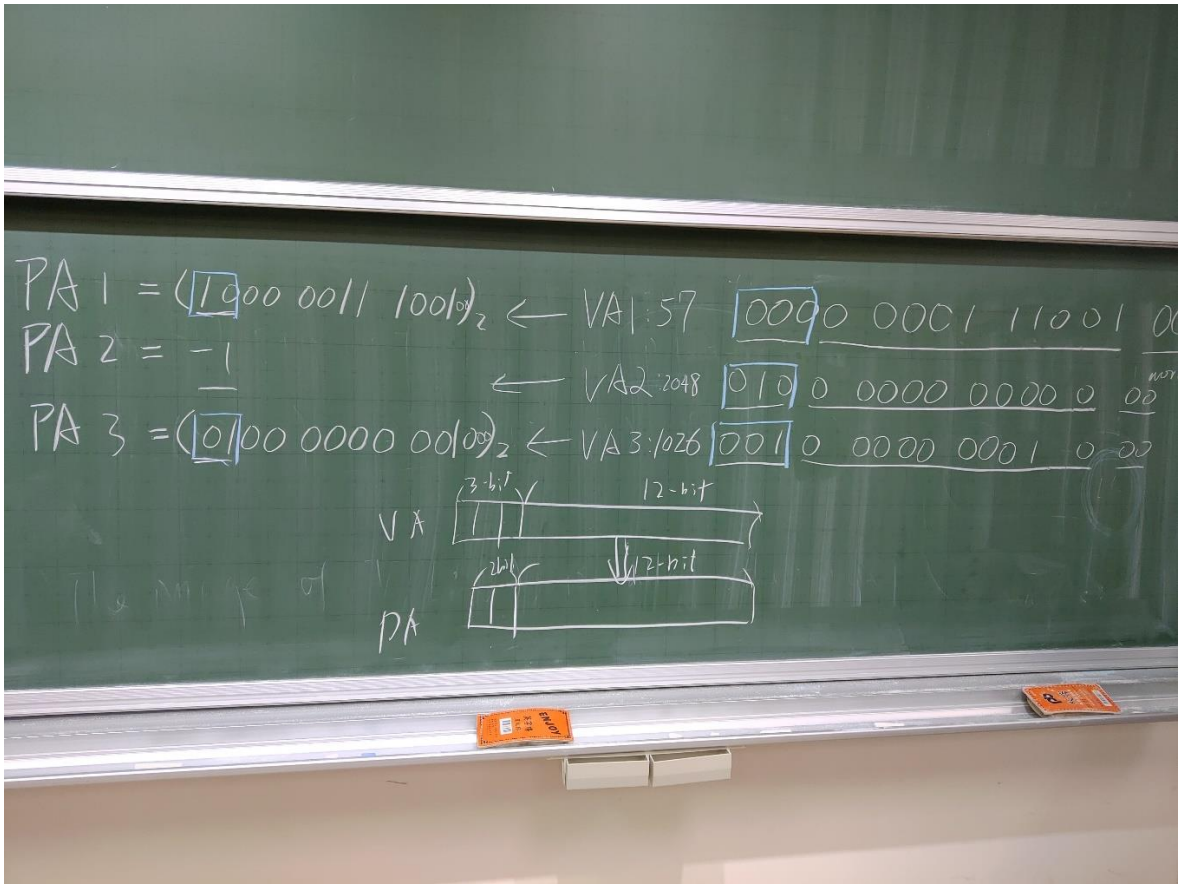
[group 10] (對抗賽)

4. The information of a virtual memory system is assumed to be:
   - Page size: 1024 words
   - Number of virtual pages: 8
   - Number of physical pages: 4
   - The current page table is

VPN	0	1	2	3	4	5	6	7
PPN	2	1	NULL	NULL	3	NULL	0	NULL

For the following (decimal) virtual word addresses: VA1: 57, VA2: 2048, VA3: 1026, VA4:7749, VA5 6150, their corresponding physical addresses are PA1, PA2, PA3, PA4, PA5. And PA =-1 if it is a page fault. Please write down PA1~PA5, separately.

Ans:



[group12]

5. Answer the following questions:
   (1) What design changes can be used to improve any one of the 3Cs?
   (2) What possible negative effect may occur for each of the design changes?

	Compulsory	Capacity	Conflict
(1)			
(2)			

Hints: Increase cache size; Increase block size; Increase access time; Increase associativity; Increase miss penalty.

ANS:

	Compulsory	Capacity	Conflict
(1)	Increase block size	Increase cache size	Increase associativity
(2)	Increase miss penalty	Increase access time	Increase access time

[group8] (對抗賽)

6. Which of the following statements are true?
   (a) All addresses generated by the program are physical addresses
   (b) One memory reference only needs one memory access.
   (c) We use hardware to detect page fault and handle the faults in software.
   (d) Array of page table entries, indexed by page offset.
   (e) PTE can refer to location in swap space on disk.

ANS: C, E

(a) all addresses generated by the program are **virtual** addresses

(b) One memory reference only needs **two** memory access: access page table and access physical memory.

(d) Array of page table entries, indexed by **virtual page number**.

[group13] (對抗賽)

7. Which statements are true? If it's false, please explain why.
   (a) When you want to access data in the memory without using TLB strategy, you can directly access it.
   (b) Page fault means that page is not resident in memory.
   (c) Hardware can handle the page faults by itself.
   (d) Following (c), we can infer that OS doesn't need to know where to find the page.
   (e) As TLB hit on write happens, dirty bit should be toggled in addition to write back to page table on replacement.
   (f) TLB hit and Page table miss can happen simultaneously.

ANS:

(a) False, you should access page table first so that you can access data stored in the memory.

(b) True.

(c) Hardware should trap to the OS so that it can remedy page faults.

(d) False, OS should need to know where to find the page.

(e) True.

(f) False, PTE haven't been moved to memory so that TLB hit is impossible.

[group 5] (對抗賽)

8. True or False

a. Every process on OS has its own page table.

~~b. 刪除~~

c. CPU doesn't need to visit TLB before fetching instruction.

d. Without virtual memory, memory access can be faster.

e. In terms of general-purpose OS, when a user process does something like:

```
int x = 1;
printf("%p", &x);
```

the standard output shows the physical address of variable x.

Ans:

(a) T

~~(b) 刪除~~

(c) F, TLB is needed.

(d) T

(e) F, Virtual address

[group 4]

9. Which of the following statements are true? if not please elaborate the reasons

(A) Reducing the page fault is important because the miss penalty is huge up to millions of cycles.

(B) As the TLB miss occurs, if the page is not in the memory, it can be fixed by hardware method.

(C) TLB is like a cache for a disk.

(D) It is possible that miss happens in TLB and page table in the same time while cache is hit.

(E) When TLB hit and read it will trigger the dirty bit.

Ans:

(A) True

(B) False, it can only be solved by software method which OS will handle fetching the page and updating the page table.

(C) True

(D) False, it is not possible since it will not be cache if it is not in the memory.

(E) False, as TLB hit and write, it will trigger the dirty bit.