Computer Architecture

Fall, 2020

Week 13

2020.12.7

Group:

組員簽名：_____

[group 8] (對抗賽)

1. Consider the following pipeline MIPS datapath with forwarding and stall control.

   A code sequence:

```
add   $1 ,$1 ,$2
add   $2 ,$2 ,$3
lw    $4 ,0($2)
add   $4 ,$4 ,$1
lw    $5 ,4($4)
lw    $5 ,0($5)
```

   (A) How many cycles does it take to complete the execution of the code?

   (B) How about no forwarding?

Ans: (A) 12 and (B) 18

(A) with forwarding

RAW: (3,4)、(5,6)

+1 +1

6+4+2=12

(B) no forwarding

RAW: (2,3)、(3,4)、(4,5)、(5,6)

+2 +2 +2 +2

6+4+8=18

[group 2] (對抗賽)

2. Please write down the correct descriptions, if it is incorrect, please also explain why.

   (A) When handling data hazards, we can insert NOP through the compiler or apply forwarding and stalls to solve the problem.

   (B) if EX/MEM.RegisterRd = MEM/WB.RegisterRd, this is a signal of forwarding.

   (C) No matter whether RegWrite is enabled or not, we still need to forward.

   (D) If RegisterRd = 0, we should not forward.

Ans: (A)(D)

(B) EX/MEM.RegisterRd = ID/EX.RegisterRs or EX.RegisterRt

(C) We only forward when RegWrite is enabled.

[group 3]

3. Determine that which of the following statements is true. Then correct the other statements.
   (a) We cannot solve all hazards by inserting nop.
   (b) We can solve all hazards by forwarding.
   (c) In MIPS, we can just stall the instruction by changing all the control signals to 0.
   (d) There is data hazard when two instructions have data dependency.

Ans:

(a) F, we can solve all hazards by inserting nop

(b) F, we cannot solve all hazards by forwarding, for example, load-use hazard and control hazard.

(c) T

(d) F, only RAW hazard leads to data hazard.

[group 4] (對抗賽)

4. Assume that there is a MIPS processor and contains forwarding and stall hardware handling data hazards. Which of the following code takes longer time to execute?

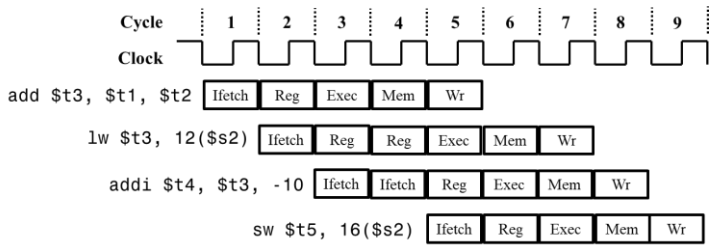
Code A (data hazard handled by stall hardware)	Code B (data hazard handled by manually inserting NOP)

add $t3, $t1, $t2
lw $t3, 12($s2)
addi $t4, $t3, -10
sw $t5, 16($s2)
	add $t3, $t1, $t2
	lw $t3, 12($s2)
	noop //no operation
	addi $t4, $t3, -10
	sw $t5, 16($s2)

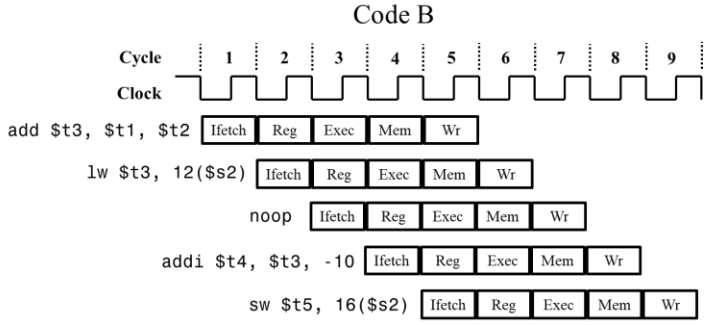
Ans:

Both of them take same clock cycles to run.

Code A



Code B



[group13] (對抗賽)

5. Which of the following statements are true? If the statement is false, please explain why.
   (A) If (Rd(MEM/WB) or Rd(EX/MEM)) = (Rs(ID/EX) or Rt(ID/EX)), then forwarding will occur.
   (B) If both value in EX/MEM and MEM/WB need to forward, then the closer one will do so.
   (C) If a stall occurs, then it will affect both first stage and second stage.
   (D) If Rt(ID/EX) = (Rs(IF/ID) or Rt(IF/ID)), then a stall will occur.
   (E) When a stall occurs, then both first stage and second stage need to repeat, and it means that "don't change IF/ID" only.
   (F) The earliest stage to sense load-use hazard is IF.
   (G) The method to stall IF stage in Stalls way can be done by enabling PCWrite and IF/IDWrite.

ANS:

(A) F, the previous instruction needs to contains "register write enable"

(B) T

(C) T

(D) F, MemRead(ID/EX) should also be true

(E) F, don't change IF/ID and "PC"

(F) F, the earliest stage to sense load-use hazard is ID.

(G) F, the method to stall IF stage in Stalls way can be done by disabling PCWrite and IF/IDWrite.

[group10] (對抗賽)

6. Refer to the following instruction sequences.

	Instruction Sequence
A	I1 lw $1, 40($2) I2 add $2, $3, $3 I3 add $1, $1, $2 I4 sw $1, 20($2)
B	I1 add $1, $2, $3 I2 sw $2, 0($1) I3 lw $1, 4($2) I4 add $2, $2, $1

(1) Find all data dependences in this instruction sequence.

	RAW	WAR	WAW
A	I1 to I3 ($1) I2 to I3, I4 ($2) I3 to I4 ($1)	I1 to I2 ($2) ~~I3 to I4 ($1)~~ 註(1)	I1 to I3 ($1)
B	I1 to I2 ($1) I3 to I4 ($1)	I1, I2, I3 to I4 ($2) I2 to I3 ($1)	I1 to I3 ($1)

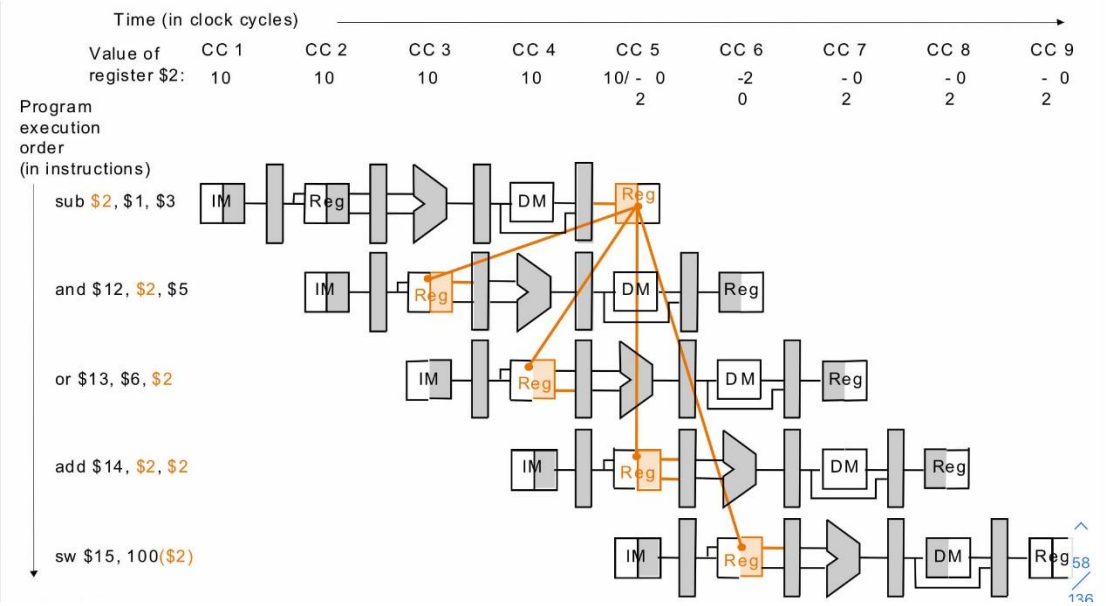
(2) Find all hazards in this instruction sequence for a five-stage pipeline with and then without forwarding.

	With forwarding	Without forwarding
A		I1 to I3 ($1) I2 to I3, I4 ($2) I3 to I4 ($1)
B	($1) I3 to I4 (Load-use)	I1 to I2 ($1) I3 to I4 ($1)

註(1): 下課有同學反應 I3 to I4 ($1)應該有算在 WAR 中，但其實是沒有。WAR、RAW、WAW 是考慮 register，而 A code 中 I4 是 Read register 的值再(寫)入 memory 中，故沒與 I3 發生 WAR 情況。

[group1] (對抗賽)

7. (a) In which instructions would cause data hazard and which would not? Explain why cause and why not cause.(Assume there's internal forwarding in register file)
   (b) Give two solutions to deal with the hazard.



ANS:

(a) and $2　　or $2　都會得到未更新的$2

(b) forwarding insert nops and
insert 2 nops or insert 1 nop

[group 12] (對抗賽)

8. A pipelined datapath has five stages, i.e., instruction fetch, decode, execution, memory, and write back. It has a hazard detection unit. An instruction will be stalled at the decode stage if any of its operations is not ready. Consider executing the following code on this datapath:

```
Lw      $2, 10($1)
sub     $4, $3, $2
add     $5, $6, $7
and     $8, $4, $5
or      $9, $8, $3
```

(1)

At the end of the fifth cycle of execution, what instruction will be in each of the pipeline stages?

IF	ID	EX	MEM	WB
add	sub	nop	nop	lw

(2)

If the datapath has a forwarding unit to resolve the data hazard, what instruction will be in each of the pipeline stages at the end of the fifth cycle?

IF	ID	EX	MEM	WB
and	add	sub	nop	lw