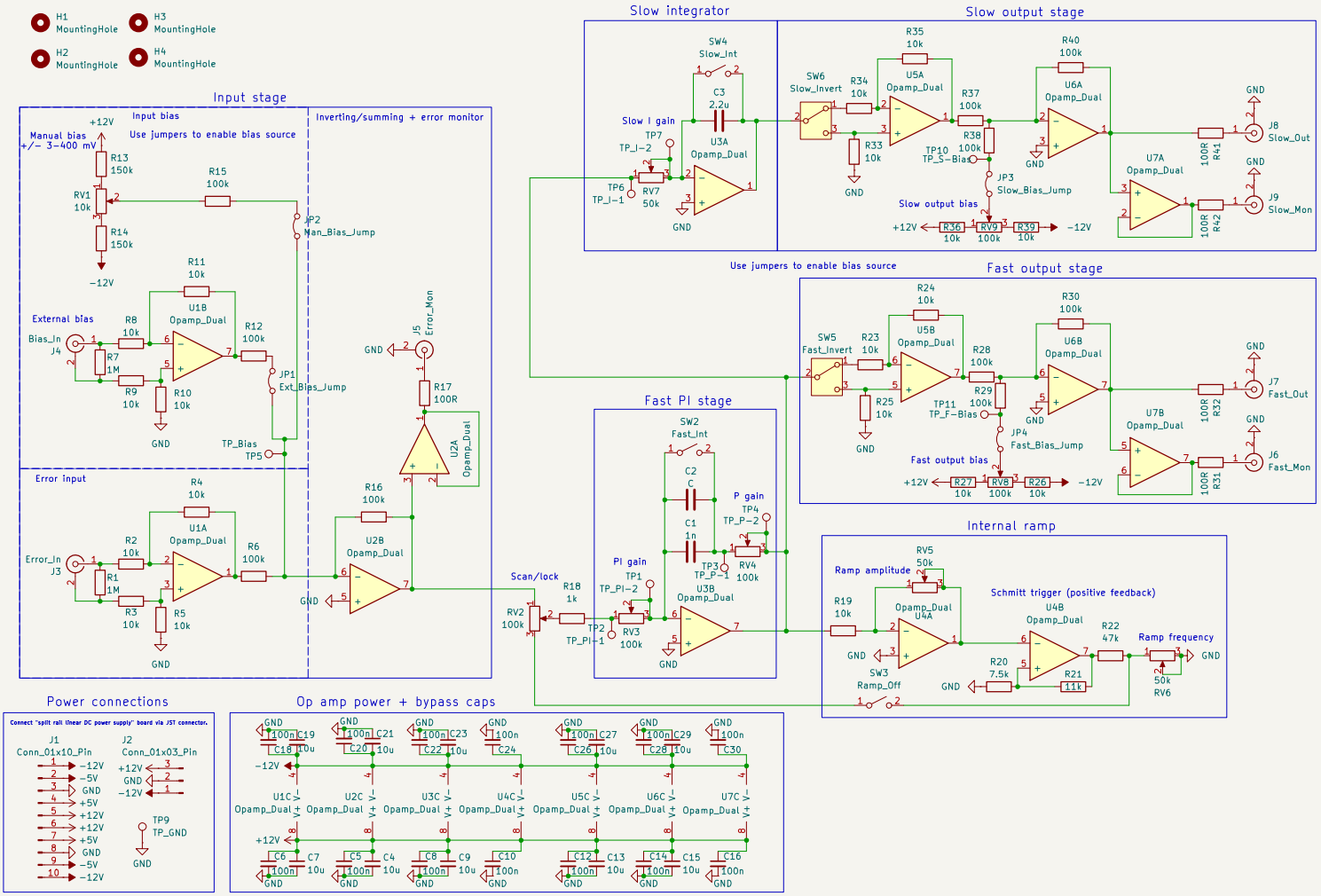
H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole
Input stage
Input bias
Use jumpers to enable bias source
Inverting/summing + error monitor
Manual bias +/- 3-400 mV
+12V
R13 150k
RV1 10k
R14 150k
-12V
R15 100k
JP2 Man_Bias_Jump
R11 10k
U1B Opamp_Dual
External bias
Bias_In J4
R8 10k
R7 1M
R9 10k
R10 10k
R12 100k
JP1 Ext_Bias_Jump
GND
TP_Bias TP5
J5 Error_Mon
R17 100R
U2A Opamp_Dual
Error input
R4 10k
U1A Opamp_Dual
Error_In J3
R2 10k
R1 1M
R3 10k
R5 10k
R6 100k
R16 100k
U2B Opamp_Dual
Slow integrator
SW4 Slow_Int
C3 2.2u
Slow I gain
TP7 TP_I-2
TP6 TP_I-1
RV7 50k
U3A Opamp_Dual
Slow output stage
R35 10k
U5A Opamp_Dual
SW6 Slow_Invert
R34 10k
R33 10k
R37 100k
R38 100k
TP10 TP_S-Bias
JP3 Slow_Bias_Jump
Slow output bias
R36 10k
RV9 100k
R39 10k
R40 100k
U6A Opamp_Dual
U7A Opamp_Dual
100R R41
100R R42
J8 Slow_Out
J9 Slow_Mon
Use jumpers to enable bias source
Fast output stage
R24 10k
U5B Opamp_Dual
SW5 Fast_Invert
R23 10k
R25 10k
R28 100k
R29 100k
TP11 TP_F-Bias
JP4 Fast_Bias_Jump
Fast output bias
R27 10k
RV8 100k
R26 10k
R30 100k
U6B Opamp_Dual
U7B Opamp_Dual
100R R32
100R R31
J7 Fast_Out
J6 Fast_Mon
Fast PI stage
SW2 Fast_Int
C2 C
C1 1n
P gain
TP4 TP_P-2
TP3 TP_P-1
RV4 100k
PI gain
TP1 TP_PI-2
TP2 TP_PI-1
RV3 100k
U3B Opamp_Dual
Scan/lock
RV2 100k
R18 1k
Internal ramp
RV5 50k
Ramp amplitude
R19 10k
Opamp_Dual U4A
SW3 Ramp_Off
Schmitt trigger (positive feedback)
U4B Opamp_Dual
R20 7.5k
R21 11k
R22 47k
Ramp frequency
50k RV6
Power connections
Connect "split rail linear DC power supply" board via JST connector.
J1 Conn_01x10_Pin
J2 Conn_01x03_Pin
+12V
-12V
-5V
GND
+5V
TP9 TP_GND
Op amp power + bypass caps
C19 100n
C18 10u
C20 100n
C21 10u
C22 10u
C23 100n
C24 100n
C26 10u
C27 100n
C28 10u
C29 100n
C30 100n
U1C Opamp_Dual
U2C Opamp_Dual
U3C Opamp_Dual
U4C Opamp_Dual
U5C Opamp_Dual
U6C Opamp_Dual
U7C Opamp_Dual
C6 100n
C7 10u
C5 100n
C4 10u
C8 100n
C9 10u
C10 100n
C12 100n
C13 10u
C14 100n
C15 10u
C16 100n