**Compact MOSFET Circuitry for Simulating Neural Ion Channels**

**Keywords:** neuromorphic computing, neuron simulation, MOSFET circuitry

**Introduction:** The ion channel of a neuron is a key functional component to the operation of living organisms, as they allow the cell to react to and generate signals (Llinas, 1988). Previous silicon models of neurons relied on complicated, power-intensive circuitry to “linearize” the channel, but it has been shown that the physical properties of a MOSFET in subthreshold mode are mathematically isomorphic to the voltage-dependent properties of biological ion channels (Hynna and Boahen, 2007). The simplest tenable silicon neuron circuit requires 8 NMOS transistors, and is limited in the way that can have incredibly rapid transitions, due to the way it linearizes voltage, that are not possible biology. In this model, two transistors serve to simulate the actual neuron while the others control and measure its operation. Building more powerful and realistic neuromorphic systems depends on designing more compact and realistic silicon models. Using CMOS technology with both PMOS and NMOS transistors is one way to reduce the footprint of a single circuit and capture the nonlinear properties of real neurons.

**Research Questions:** Because half of the transistors in the 8-transistor model are dedicated to inverting the membrane voltage on one of the neuron’s NMOS transistors, it would be advantageous to replace this component with a PMOS transistor. The two transistors that comprise the “neuron” would inherently have opposite responses to the membrane voltage. Furthermore, this would effectively free up real-estate for introducing new circuitry to build a more accurate model. Rather than building the model to have a linear voltage dependence and an extra transistor to limit the maximum current, a simple circuit with a resistor and MOSFET in saturation can be used to exploit the quadratic relationship between gate voltage and current.

**Research Plan:** The two proposed tweaks to the 8-transistor model, namely incorporating a PMOS instead of an inverter and allowing for a quadratic voltage dependence, should be done in parallel because of the long lead times associated with fabricating CMOS circuits and the fact that their behaviors are decoupled electronically. SPICE software will be used to simulate the behavior of the silicon neuron when a PMOS transistor is put in place of the inverter in order to assess the feasibility of the design and optimize the intrinsic properties of the circuit. This circuit must demonstrate the same thermodynamic isomorphism to biological neurons as the original circuit to be a valid tweak. Next, the current-limiting MOSFET will be replaced with a voltage-controlling circuit containing a MOSFET in saturation. Simulations of this circuit must demonstrate the neuron’s robustness against unrealistically fast transition rates. Finally, these two changes can be merged to create a new silicon neuron model that is both more compact and more accurate.

**Intellectual Merit & Broader Impacts:** Although we currently understand the chemistry behind how neurons communicate and the resultant emergent behavior of the brain, we only have theories about what happens in between these two levels. Not only will a functioning neuromorphic system that employs silicon neurons give neuroscientists the opportunity to peer into these inner layers for the first time, but it will also enable the next generation of low power supercomputers. One such application of neuromorphic devices is deep space exploration, where radiation and power limitations pose to be challenges with modern CPUs. Neuromorphic systems would be inherently parallelized and robust to corruption, just like the human brain can function despite having noisy hardware.

**References:**

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