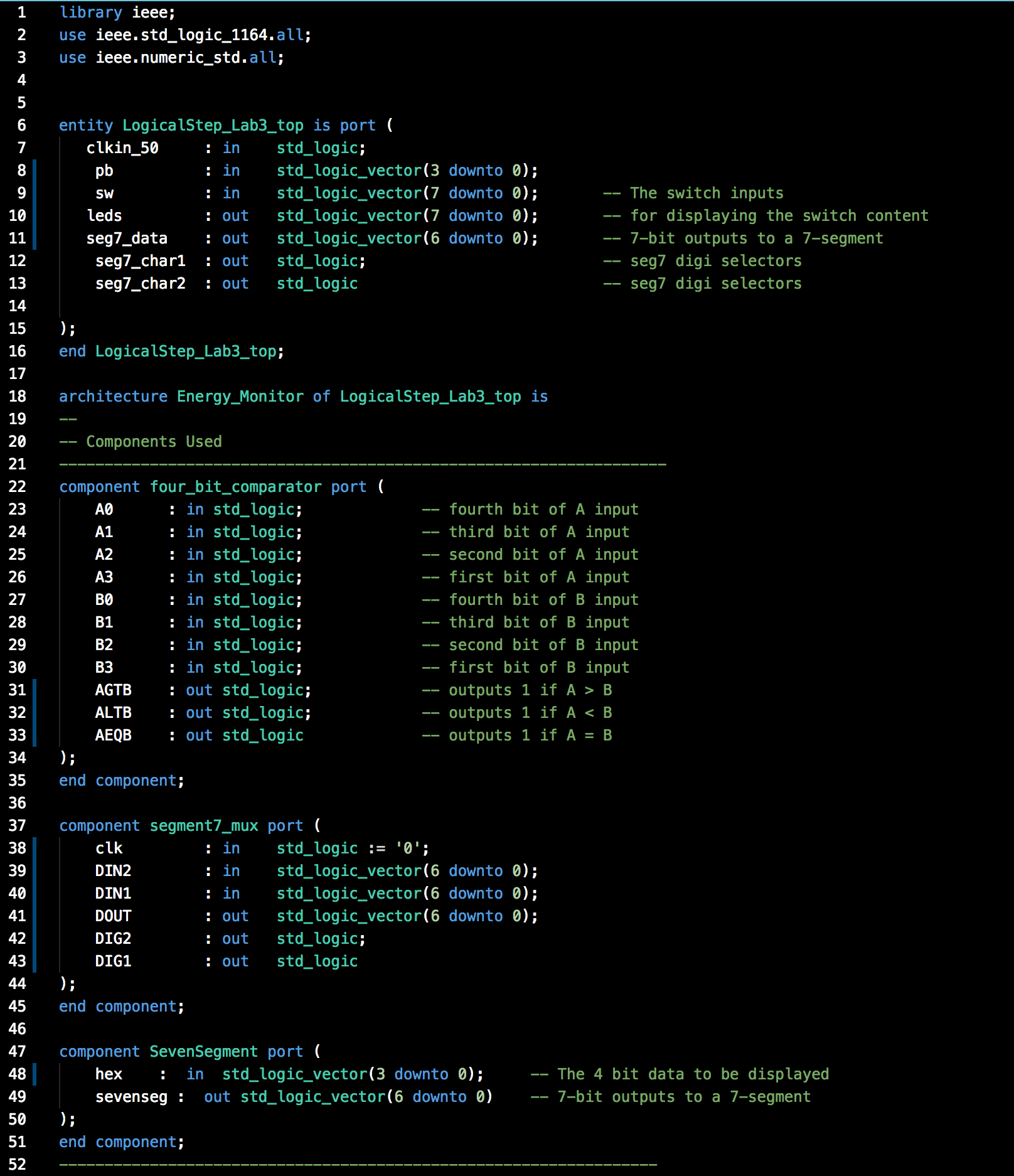
LAB3 REPORT

*GRP 19 | SESS 204*

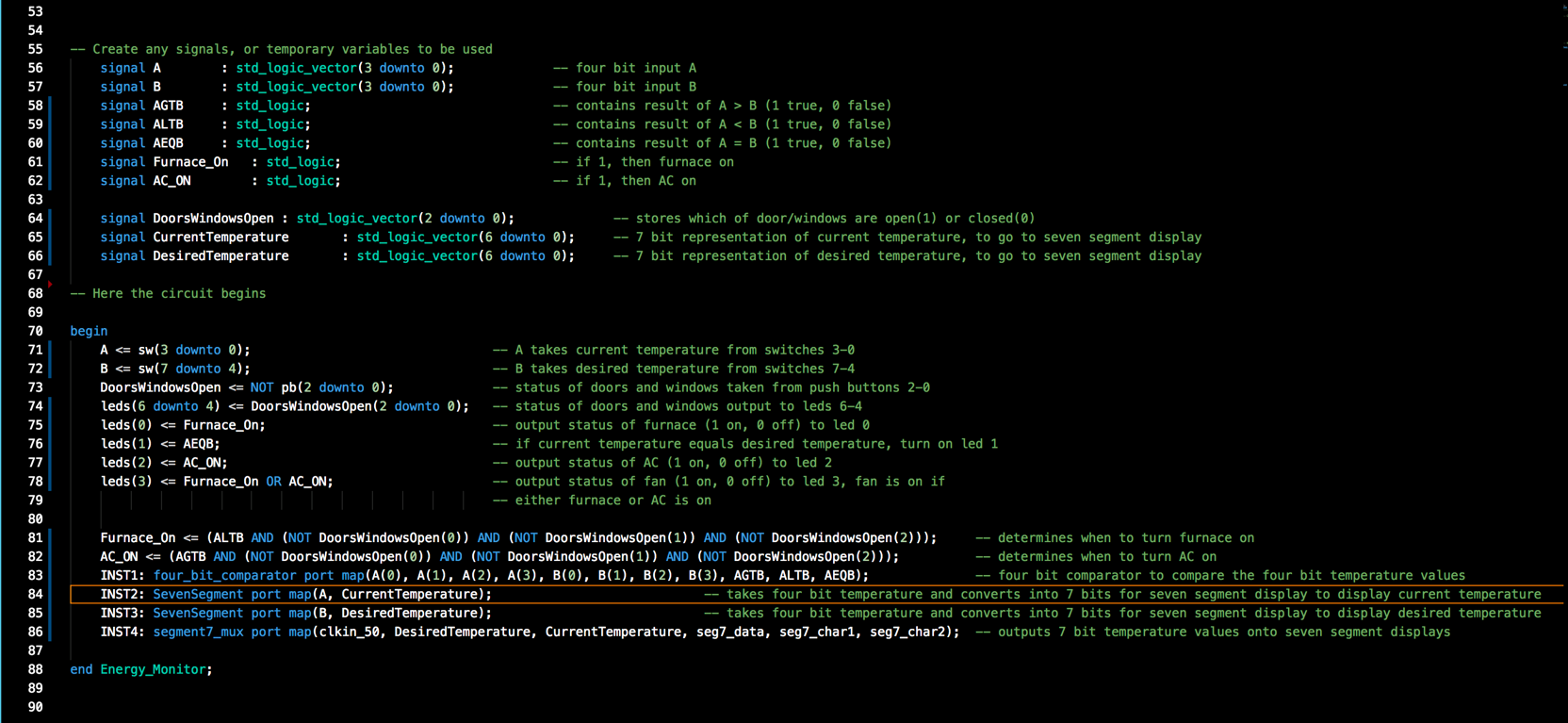
20714953 CHANG HEI MATTHIAS FUNG | 20733210 COLTON WESLEY MILLS

Part 1)

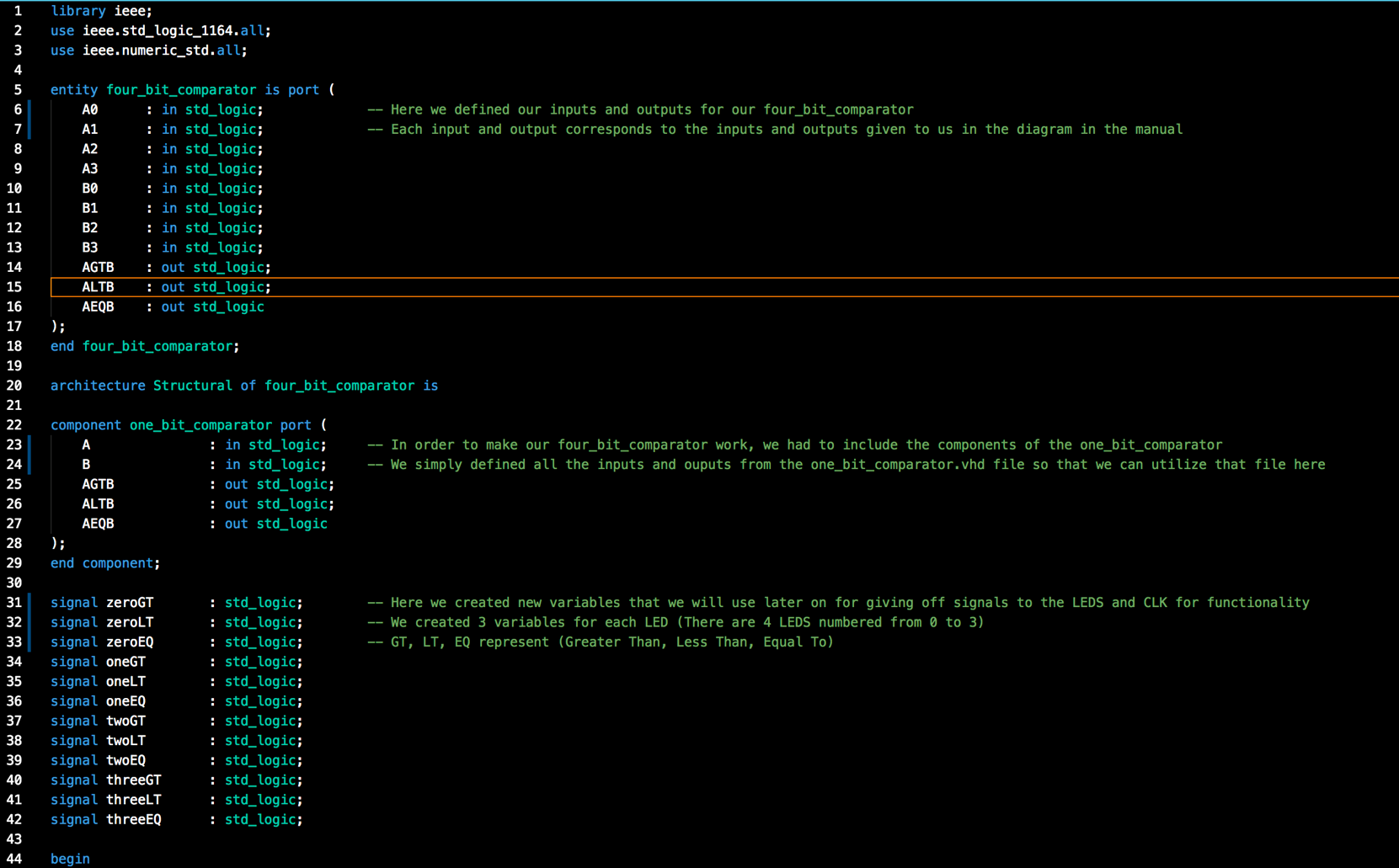
LogicalStep\_Lab3\_top.vhd file:

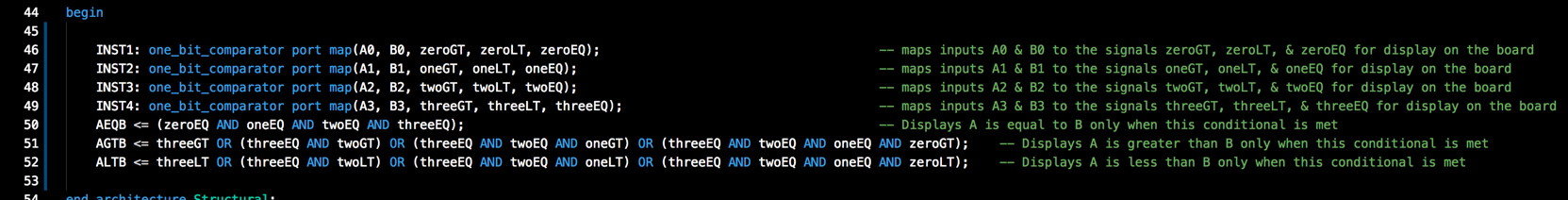


To be continued on next page...

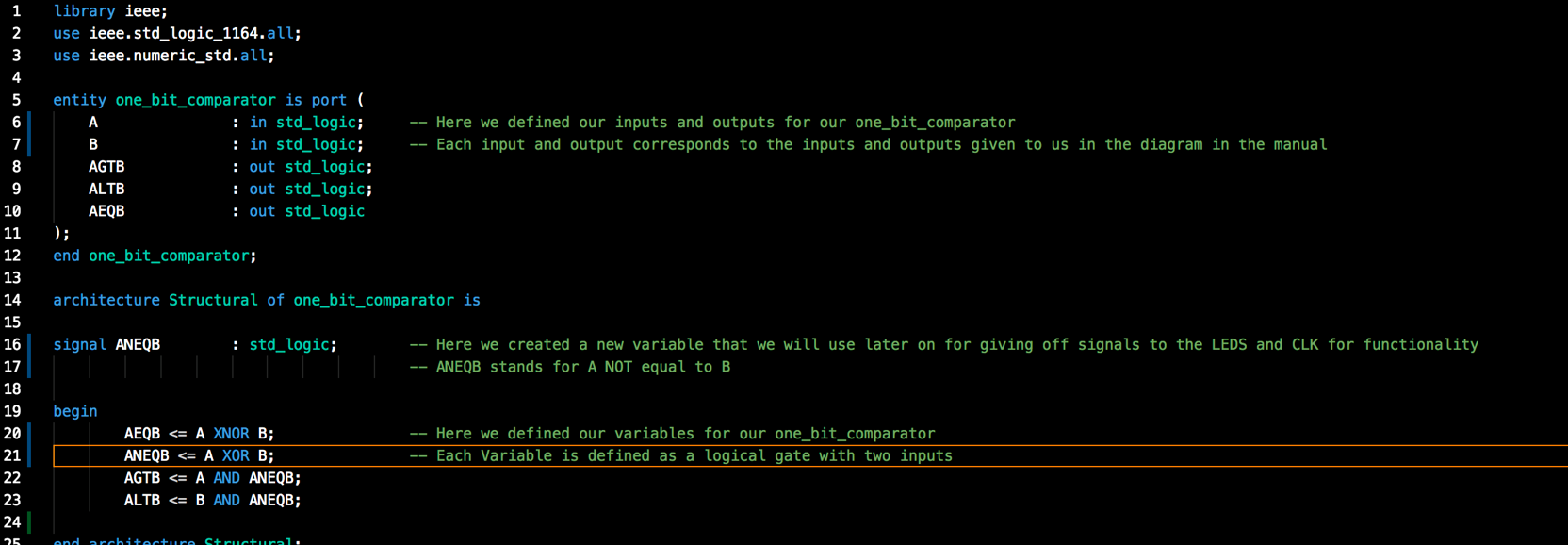


four\_bit\_comparator.vhd file:

**

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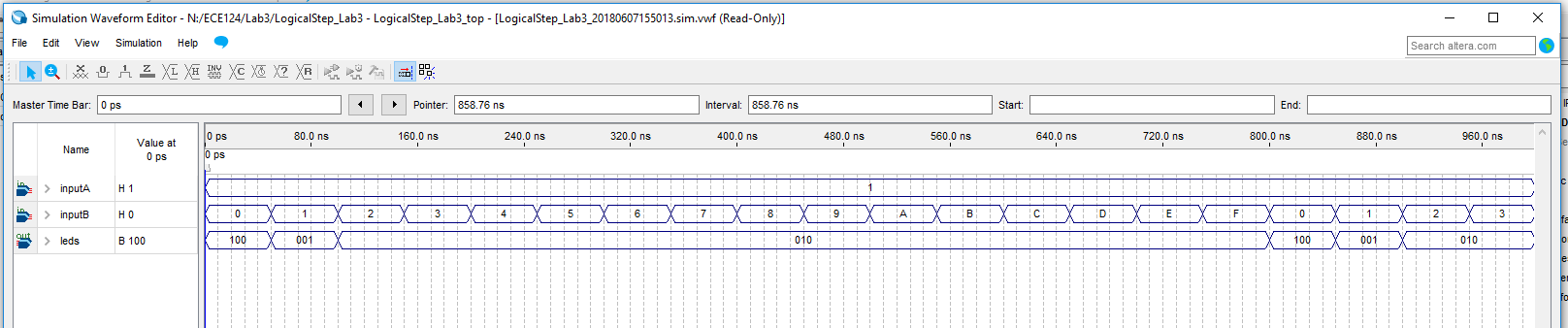
one\_bit\_comparator.vhd file:

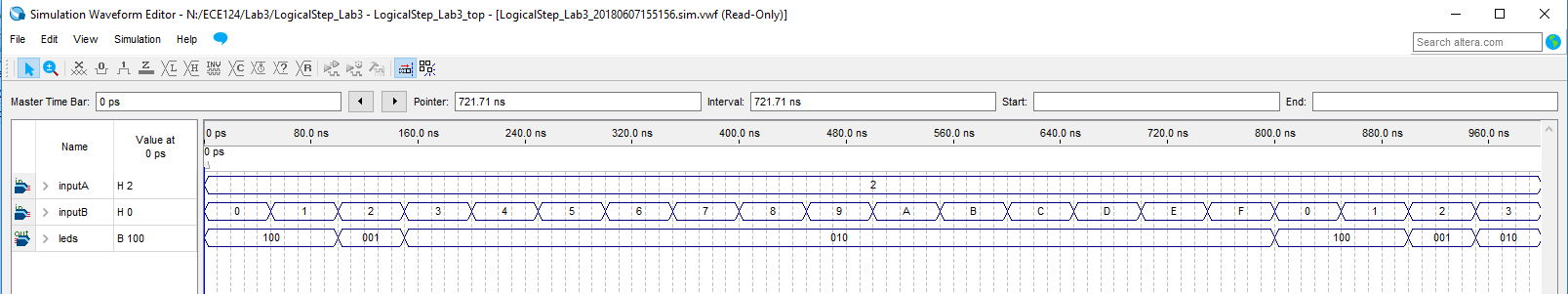
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Part 2) Supporting documentation:

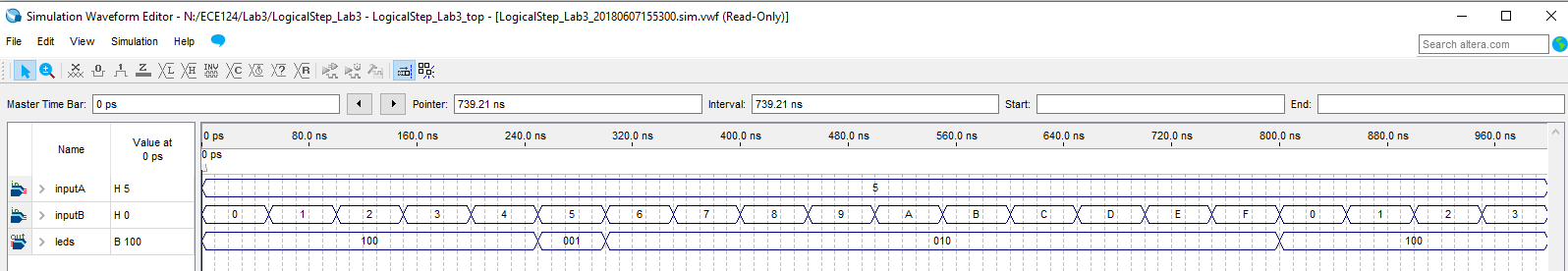
*Truth Table for 4-bit Comparator:*

*Simulations:*

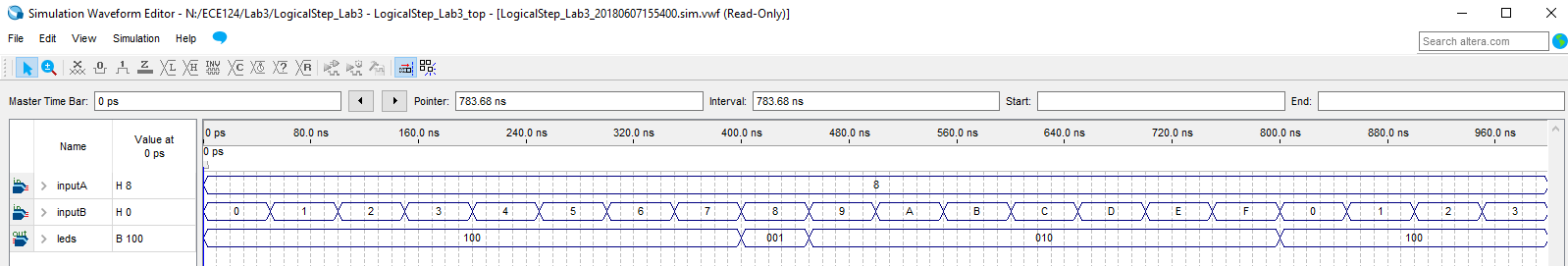
**Input\_A to Static Value of Hex 1** **

**Input\_A to Static Value of Hex 2****

**Input\_A to Static Value of Hex 5**

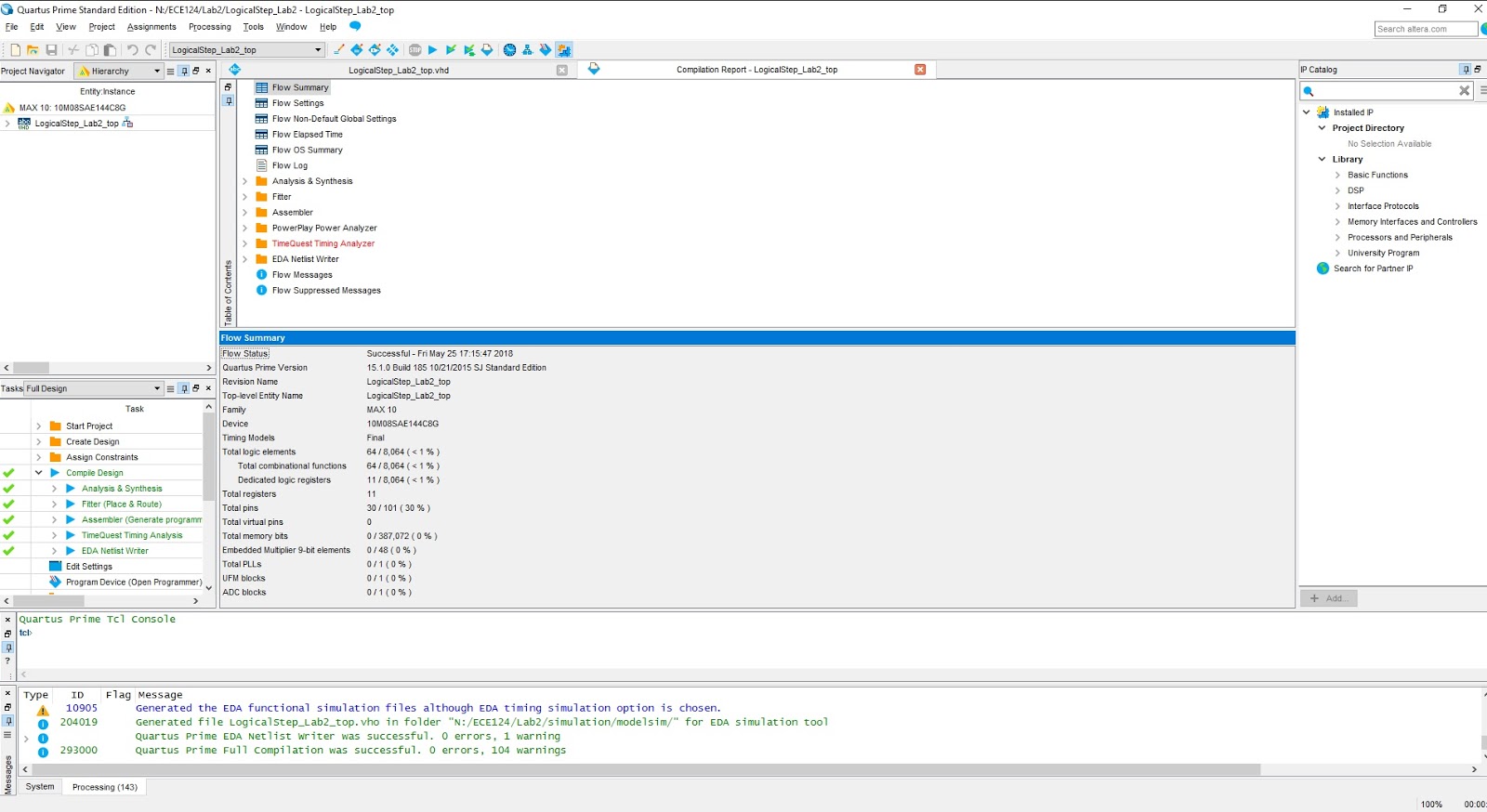
**

**Input\_A to Static Value of Hex 8**

**

*RTL Diagram of the Design:*

*Compile Report Information:*



*Figure 3: Sample Compilation Report*

The figure above shows a sample compilation report from simulating the VHDL code we wrote. As shown, the report tells us the statistics, compilation status and other details about the compilation of our code. The report is very helpful as sometimes when we get errors from our code, we gain direction on where the error is occurring and allows us to quickly sort out the error. A total of **64 Design Logic Elements** were used.