nRF5340

Engineering A

Errata

v1.1

NORDIC® SEMICONDUCTOR

Contents

1 nRF5340 Engineering A Errata . . . 4

2 Change log . . . 5

3 New and inherited anomalies . . . 8

3.1 [3] SAADC: VDDHDIV5 is not functional . . . 10
3.2 [4] CLOCK: Changing application core frequency register HFCLKCTRL requires additional register initialization . . . 11
3.3 [5] TAD: Trace is not functional when application core is running at 128 MHz . . . 11
3.4 [6] NVMC: Disabling instruction cache causes skip of next instruction . . . 12
3.5 [7] USBD: USBD is not functional . . . 13
3.6 [8] WDT: WDT1 is not functional . . . 13
3.7 [9] TAD: TPIU is missing from ROM table . . . 14
3.8 [10] CCM: Reading CNFPTR, INPTR, OUTPTR, and SCRATCHPTR pointers returns incorrect address . . . 16
3.9 [11] ACL: Reading ACL[n].ADDR returns incorrect address . . . 16
3.10 [12] QSPI: SCKFREQ is not functional at 96 MHz . . . 17
3.11 [13] GPIO: Bits in LATCH register are incorrectly set to 1 . . . 17
3.12 [14] TIMER: CC[6] and CC[7] are not functional . . . 18
3.13 [15] UARTE: Odd parity setting is not functional . . . 18
3.14 [16] RADIO: POWER register is not functional . . . 19
3.15 [18] I2S: 32-bit sample widths and 8-bit sample in a 16-bit half-frame are not functional . . . 19
3.16 [19] SPU: Flash memory space is divided into 32 regions of 32 KiB . . . 20
3.17 [20] RTC: TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional . . . 20
3.18 [21] TWIM: 1000 kbps baud rate is not functional . . . 21
3.19 [22] SPU: CPULOCK register is not functional . . . 21
3.20 [23] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST enabled . . . 22
3.21 [26] CTRL-AP: APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional . . . 22
3.22 [27] CTRL-AP: STATUS register is not functional . . . 23
3.23 [28] TIMER: INTEN register is not functional . . . 23
3.24 [29] SWI: SWIRQ is not functional . . . 24
3.25 [30] RESET: LCTRLAP field in RESETREAS register is not functional . . . 24
3.26 [32] GPIO: GPIO pins assigned to network core do not retain their state in System OFF mode . . . 25
3.27 [33] CLOCK: LFRC frequency starts drifting even if calibration task is triggered . . . 25
3.28 [37] TWIM: First clock pulse after clock stretching may be too long or too short . . . 26
3.29 [42] CLOCK: Reset value of HFCLKCTRL is invalid . . . 26
3.30 [43] QSPI: Reading QSPI registers after XIP might halt application CPU . . . 27
3.31 [44] UARTE: TASKS_RESUME impacts UARTE . . . 27
3.32 [45] SPIM: Receive is not functional at 32 Mbps . . . 28
3.33 [46] CLOCK: LFRC has higher current consumption . . . 29
3.34 [47] TWIM: I2C timing spec is violated at 400 kHz . . . 29
3.35 [49] POWER: SLEEPENTER and SLEEPEXIT events are asserted after pin reset . . . 30
3.36 [50] SPU: Arm TrustZone region numbers for FICR, UICR, CACHEINFO, and CACHEDATA are incorrect . . . 31
3.37 [51] SPU: Accessing FICR, UICR, CACHEINFO, or CACHEDATA from non-secure state gives bus error . . . 31
3.38 [53] REGULATORS: Current consumption in normal voltage mode is higher in System ON idle . . . 32

3.39 [54] REGULATORS: Current consumption in normal voltage mode is higher in System ON idle and System OFF . . . 33
3.40 [55] RESET: Bits in RESETREAS are set when they should not be . . . 33
3.41 [57] I2S: EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional . . . 34
3.42 [58] I2S: BYPASS in CONFIG.CLKCONFIG is not functional . . . 34
3.43 [59] QDEC: QDEC0 is not functional . . . 35
3.44 [62] UICR: HFXOCNT register is not functional . . . 35
3.45 [64] REGULATORS: VREGMAIN has invalid configuration when CPU is running . . . 36
3.46 [65] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST disabled . . . 36
3.47 [69] REGULATORS: VREGMAIN configuration is not retained in System OFF . . . 37
3.48 [72] REGULATORS: Current consumption in high voltage mode is higher in System ON idle and System OFF . . . 38
3.49 [73] TIMER: ONESHOTEN[n] registers are located at an incorrect address offset . . . 38
3.50 [74] TIMER: COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register . . . 39
3.51 [79] QDEC: QDEC1 is not functional . . . 39
3.52 [80] PWM: PWM3 is not functional . . . 40
3.53 [81] SPIM: SPIM2 and SPIM3 are not functional . . . 40
3.54 [82] TWIM: TWIM2 and TWIM3 are not functional . . . 41
3.55 [83] SPIS: SPIS2 and SPIS3 are not functional . . . 41
3.56 [84] UARTE: UARTE2 and UARTE3 are not functional . . . 41

1 nRF5340 Engineering A Errata

This Errata document contains anomalies for the nRF5340 chip, revision Engineering A (QKAA-AB0).

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF5340 Engineering A v1.1	09.12.2019	• Updated: No. 42. “Reset value of HFCLKCTRL is invalid” • Updated: No. 59. “QDEC is not functional” • Added: No. 43. “Reading QSPI registers after XIP might halt application CPU” • Added: No. 62. “HFXOCNT register is not functional” • Added: No. 64. “VREGMAIN has invalid configuration when CPU is running” • Added: No. 73. “ONESHOTEN[n] registers are located at an incorrect address offset” • Added: No. 74. “COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register” • Added: No. 79. “QDEC1 is not functional” • Added: No. 80. “PWM3 is not functional” • Added: No. 81. “SPIM2 and SPIM3 are not functional” • Added: No. 82. “TWIM2 and TWIM3 are not functional” • Added: No. 83. “SPIS2 and SPIS3 are not functional” • Added: No. 84. “UARTE2 and UARTE3 are not functional”

Version	Date	Change
nRF5340 Engineering A v1.0	14.11.2019	• Added: No. 3. “VDDHDIV5 is not functional” • Added: No. 4. “Changing application core frequency register HFCLKCTRL requires additional register initialization” • Added: No. 5. “Trace is not functional when application core is running at 128 MHz” • Added: No. 6. “Disabling instruction cache causes skip of next instruction” • Added: No. 7. “USBD is not functional” • Added: No. 8. “WDT1 is not functional” • Added: No. 9. “TPIU is missing from ROM table” • Added: No. 10. “Reading CNFPTR, INPTR, OUTPTR, and SCRATCHPTR pointers returns incorrect address” • Added: No. 11. “Reading ACL[n].ADDR returns incorrect address” • Added: No. 12. “SCKFREQ is not functional at 96 MHz” • Added: No. 13. “Bits in LATCH register are incorrectly set to 1” • Added: No. 14. “CC[6] and CC[7] are not functional” • Added: No. 15. “Odd parity setting is not functional” • Added: No. 16. “POWER register is not functional” • Added: No. 18. “32-bit sample widths and 8-bit sample in a 16-bit half-frame are not functional” • Added: No. 19. “Flash memory space is divided into 32 regions of 32 KiB” • Added: No. 20. “TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional” • Added: No. 21. “1000 kbps baud rate is not functional” • Added: No. 22. “CPULOCK register is not functional” • Added: No. 23. “Events are not generated when switching from scan mode to no-scan mode with BURST enabled” • Added: No. 26. “APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional” • Added: No. 27. “STATUS register is not functional” • Added: No. 28. “INTEN register is not functional” • Added: No. 29. “SWIRQ is not functional” • Added: No. 30. “LCTRLAP field in RESETREAS register is not functional” • Added: No. 32. “GPIO pins assigned to network core do not retain their state in System OFF mode” • Added: No. 33. “LFRC frequency starts drifting even if calibration task is triggered” • Added: No. 37. “First clock pulse after clock stretching may be too long or too short” • Added: No. 42. “Reset value of HFCLKCTRL is invalid” • Added: No. 44. “TASKS_RESUME impacts UARTE” • Added: No. 45. “Receive is not functional at 32 Mbps” • Added: No. 46. “LFRC has higher current consumption” • Added: No. 47. “I2C timing spec is violated at 400 kHz” • Added: No. 49. “SLEEPENTER and SLEEPEXIT events are asserted after pin reset”

Version	Date	Change
		• Added: No. 50. “Arm TrustZone region numbers for FICR, UICR, CACHEINFO, and CACHEDATA are incorrect” • Added: No. 51. “Accessing FICR, UICR, CACHEINFO, or CACHEDATA from non-secure state gives bus error” • Added: No. 53. “Current consumption in normal voltage mode is higher in System ON idle” • Added: No. 54. “Current consumption in normal voltage mode is higher in System ON idle and System OFF” • Added: No. 55. “Bits in RESETREAS are set when they should not be” • Added: No. 57. “EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional” • Added: No. 58. “BYPASS in CONFIG.CLKCONFIG is not functional” • Added: No. 59. “QDEC is not functional” • Added: No. 65. “Events are not generated when switching from scan mode to no-scan mode with BURST disabled” • Added: No. 69. “VREGMAIN configuration is not retained in System OFF” • Added: No. 72. “Current consumption in high voltage mode is higher in System ON idle and System OFF”

3 New and inherited anomalies

The following anomalies are present in revision Engineering A of the nRF5340 chip.

ID	Domain	Module	Description	New in Engineering A
3	Application	SAADC	VDDHDIV5 is not functional	X
4	Application	CLOCK	Changing application core frequency register HFCLKCTRL requires additional register initialization	X
5	Application	TAD	Trace is not functional when application core is running at 128 MHz	X
6	Network	NVMC	Disabling instruction cache causes skip of next instruction	X
7	Application	USBD	USBD is not functional	X
8	Application	WDT	WDT1 is not functional	X
9	Application	TAD	TPIU is missing from ROM table	X
10	Network	CCM	Reading CNFPTR, INPTR, OUTPTR, and SCRATCHPTR pointers returns incorrect address	X
11	Network	ACL	Reading ACL[n].ADDR returns incorrect address	X
12	Application	QSPI	SCKFREQ is not functional at 96 MHz	X
13	Application, Network	GPIO	Bits in LATCH register are incorrectly set to 1	X
14	Network	TIMER	CC[6] and CC[7] are not functional	X
15	Application, Network	UARTE	Odd parity setting is not functional	X
16	Network	RADIO	POWER register is not functional	X
18	Application	I2S	32-bit sample widths and 8-bit sample in a 16-bit half-frame are not functional	X
19	Application	SPU	Flash memory space is divided into 32 regions of 32 KiB	X
20	Application, Network	RTC	TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional	X
21	Application, Network	TWIM	1000 kbps baud rate is not functional	X
22	Application	SPU	CPULOCK register is not functional	X
23	Application	SAADC	Events are not generated when switching from scan mode to no-scan mode with BURST enabled	X
26	Application, Network	CTRL-AP	APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional	X

ID	Domain	Module	Description	New in Engineering A
27	Application, Network	CTRL-AP	STATUS register is not functional	X
28	Application, Network	TIMER	INTEN register is not functional	X
29	Network	SWI	SWIRQ is not functional	X
30	Network	RESET	LCTRLAP field in RESETREAS register is not functional	X
32	Network	GPIO	GPIO pins assigned to network core do not retain their state in System OFF mode	X
33	Application	CLOCK	LFRC frequency starts drifting even if calibration task is triggered	X
37	Application, Network	TWIM	First clock pulse after clock stretching may be too long or too short	X
42	Application	CLOCK	Reset value of HFCLKCTRL is invalid	X
43	Application	QSPI	Reading QSPI registers after XIP might halt application CPU	X
44	Application, Network	UARTE	TASKS_RESUME impacts UARTE	X
45	Application	SPIM	Receive is not functional at 32 Mbps	X
46	Application	CLOCK	LFRC has higher current consumption	X
47	Application, Network	TWIM	I2C timing spec is violated at 400 kHz	X
49	Application, Network	POWER	SLEEPENTER and SLEEPEXIT events are asserted after pin reset	X
50	Application	SPU	Arm TrustZone region numbers for FICR, UICR, CACHEINFO, and CACHEDATA are incorrect	X
51	Application	SPU	Accessing FICR, UICR, CACHEINFO, or CACHEDATA from non-secure state gives bus error	X
53	Application	REGULATORS	Current consumption in normal voltage mode is higher in System ON idle	X
54	Network	REGULATORS	Current consumption in normal voltage mode is higher in System ON idle and System OFF	X
55	Application, Network	RESET	Bits in RESETREAS are set when they should not be	X
57	Application	I2S	EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional	X
58	Application	I2S	BYPASS in CONFIG.CLKCONFIG is not functional	X
59	Application	QDEC	QDEC0 is not functional	X
62	Application, Network	UICR	HFXOCNT register is not functional	X

ID	Domain	Module	Description	New in Engineering A
64	Application	REGULATORS	VREGMAIN has invalid configuration when CPU is running	X
65	Application	SAADC	Events are not generated when switching from scan mode to no-scan mode with BURST disabled	X
69	Application	REGULATORS	VREGMAIN configuration is not retained in System OFF	X
72	Application	REGULATORS	Current consumption in high voltage mode is higher in System ON idle and System OFF	X
73	Application, Network	TIMER	ONESHOTEN[n] registers are located at an incorrect address offset	X
74	Application, Network	TIMER	COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register	X
79	Application	QDEC	QDEC1 is not functional	X
80	Application	PWM	PWM3 is not functional	X
81	Application	SPIM	SPIM2 and SPIM3 are not functional	X
82	Application	TWIM	TWIM2 and TWIM3 are not functional	X
83	Application	SPIS	SPIS2 and SPIS3 are not functional	X
84	Application	UARTE	UARTE2 and UARTE3 are not functional	X

Table 1: New and inherited anomalies

3.1 [3] SAADC: VDDHDIV5 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

Conditions

Always.

Consequences

VDDHDIV5 setting on CH[x].PSELP and CH[x].PSELN is not functional.

Workaround

None.

3.2 [4] CLOCK: Changing application core frequency register HFCLKCTRL requires additional register initialization

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

RAM content is corrupted.

Conditions

Switching application core between 64 MHz and 128 MHz.

Consequences

RAM content is corrupted.

Workaround

When changing HFCLKCTRL from 64 MHz to 128 MHz:

1. Complete all memory transactions.
2. Execute the following commands:

```
*(volatile uint32_t *)0x5084450C= 0x4040;
*(volatile uint32_t *)0x50026548 = 0x40;
*(volatile uint32_t *)0x50081EE4 = 0x4D;
NRF_CLOCK_S.HFCLKCTRL = 0;
```

When changing HFCLKCTRL from 128 MHz to 64 MHz:

1. Complete all memory transactions.
2. Execute the following commands:

```
NRF_CLOCK_S.HFCLKCTRL = 1;
*(volatile uint32_t *)0x5084450C= 0x0;
*(volatile uint32_t *)0x50026548 = 0x0;
*(volatile uint32_t *)0x50081EE4 = 0x0D;
```

3.3 [5] TAD: Trace is not functional when application core is running at 128 MHz

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Trace packets are lost.

Conditions

Trace port is enabled and application core runs at 128 MHz.

Consequences

Trace bandwidth is reduced. Trace packet loss may increase.

Workaround

Run application core at 64 MHz during trace.

3.4 [6] NVMC: Disabling instruction cache causes skip of next instruction

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

The CPU skips the first instruction after instruction cache is disabled.

Conditions

The code executes instructions to disable the instruction cache.

Consequences

The program does not execute as expected.

Workaround

Use the following function to disable instruction cache:

```
_attribute_((aligned(ICACHE_LINE_SIZE)))

void icache_disable(void) {
    int key = DisableInterrupts();
    __ISB();
    NRF_NVMC->ICACHECNF = 0;
    __ISB();
    EnableInterrupts(key);
}
```

3.5 [7] USBD: USBD is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

USBD is not functional.

Conditions

Always.

Consequences

USBD is not functional.

Workaround

None.

3.6 [8] WDT: WDT1 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Watchdog timer 1 is not functional.

Conditions

Always.

Consequences

Watchdog timer 1 is not functional.

Workaround

None.

3.7 [9] TAD: TPIU is missing from ROM table

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

AHB-AP points to the Cortex-M33 ROM table and not the Application core ROM table.

Conditions

Always.

Consequences

IDEs cannot automatically configure TPIU for trace output.

Workaround

Initialize trace modules manually with the following code and, if necessary, use debug probe-dependent mechanisms to set up extra ROM table addresses.

```
#define ARM_CS_LOCK 0x00000000
#define ARM_CS_UNLOCK 0xC5ACCE55

#define ETM_TRCPRGCTLR_Enable (1 << 0)
#define ETM_TRCCONFIGR_BranchBroadcast_En (1 << 3)
#define ETM_TRCCONFIGR_Timestamp_En (1 << 11)
#define ETM_TRCCONFIGR_ReturnStack_En (1 << 12)
#define ETM_TRCEVENTCTL0R_Sel0_Resources2 (2 << 0)
#define ETM_TRCEVENTCTL1R_Insten_Event0_En (1 << 0)
#define ETM_TRCRSCTLR2_Select_Resource0 (1 << 0)
#define ETM_TRCRSCTLR2_Group_Resource0 (1 << 16)
#define ETM_TRCSTALLCTLR_Level_ZeroInvasion (0 << 0)
#define ETM_TRCSYNCPR_Period_12 (12 << 0)
#define ETM_TRCTSCTLR_Event_0 (0 << 0)
#define ETM_TRCTRACEIDR_TraceId (1 << 0)
#define ETM_TRCVICTLR_StartStopLogic_On (1 << 9)
#define ETM_TRCVICTLR_Event_0 (1 << 0)

#define ETM_TRCPRGCTLR 0xE0041004
#define ETM_TRCCONFIGR 0xE0041010
#define ETM_TRCEVENTCTL0R 0xE0041020
#define ETM_TRCEVENTCTL1R 0xE0041024
#define ETM_TRCSTALLCTLR 0xE004102C
#define ETM_TRCTSCTLR 0xE0041030
#define ETM_TRCSYNCPR 0xE0041034
#define ETM_TRCTRACEIDR 0xE0041040
#define ETM_TRCVICTLR 0xE0041080
#define ETM_TRCRSCTLR2 0xE0041208
#define ETM_TRCLAR 0xE0041FB0

#define TPIU_SPPR_ParallelMode 0x0
#define TPIU_FFCR_EnFCont (1 << 1)

#define TPIU_CSPSR 0xE0040004
#define TPIU_SPPR 0xE00400F0
#define TPIU_FFCR 0xE0040304
#define TPIU_LAR 0xE0040FB0

void etm_init(void)
{
    uint32_t etm_stable = 0x00000000;

    // Basic programming of ETM
    *(uint32_t*)(ETM_TRCLAR) = ARM_CS_UNLOCK;
    *(uint32_t*)(ETM_TRCCONFIGR) = ETM_TRCCONFIGR_Timestamp_En |
 ETM_TRCCONFIGR_ReturnStack_En;
    *(uint32_t*)(ETM_TRCEVENTCTL0R) = ETM_TRCEVENTCTL0R_Sel0_Resources2;
    *(uint32_t*)(ETM_TRCEVENTCTL1R) = ETM_TRCEVENTCTL1R_Insten_Event0_En;
```

```
    *(uint32_t*)(ETM_TRCRSCTLR2) = ETM_TRCRSCTLR2_Select_Resource0 |
 ETM_TRCRSCTLR2_Group_Resource0;
    *(uint32_t*)(ETM_TRCSTALLCTLR) = ETM_TRCSTALLCTLR_Level_ZeroInvasion;
    *(uint32_t*)(ETM_TRCSYNCPR) = ETM_TRCSYNCPR_Period_12;
    *(uint32_t*)(ETM_TRCTRACEIDR) = ETM_TRCTRACEIDR_TraceId;
    *(uint32_t*)(ETM_TRCTSCTLR) = ETM_TRCTSCTLR_Event_0;
    *(uint32_t*)(ETM_TRCVICTLR) = ETM_TRCVICTLR_StartStopLogic_On | ETM_TRCVICTLR_Event_0;

    // Enable ETM
    *(uint32_t*)(ETM_TRCPRGCTLR) = ETM_TRCPRGCTLR_Enable;
    *(uint32_t*)(ETM_TRCLAR) = ARM_CS_LOCK;
}

void tpiu_init(void)
{
    *(uint32_t*)(TPIU_LAR) = ARM_CS_UNLOCK;

    *(uint32_t*)(TPIU_CSPSR) = (1 << 3);
    *(uint32_t*)(TPIU_SPPR) = TPIU_SPPR_ParallelMode;
    *(uint32_t*)(TPIU_FFCR) = TPIU_FFCR_EnFCont;

    *(uint32_t*)(TPIU_LAR) = ARM_CS_LOCK;
}
```

3.8 [10] CCM: Reading CNFPTR, INPTR, OUTPTR, and SCRATCHPTR pointers returns incorrect address

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Conditions

On reading CCM pointers CNFPTR, INPTR, OUTPTR, and SCRATCHPTR.

Consequences

CCM pointers CNFPTR, INPTR, OUTPTR, and SCRATCHPTR return incorrect address on read.

Workaround

Logically OR the read CCM pointers CNFPTR, INPTR, OUTPTR, and SCRATCHPTR with 0x0100_0000 to get the correct address.

3.9 [11] ACL: Reading ACL[n].ADDR returns incorrect address

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

Reading ACL[n].ADDR returns incorrect address.

Conditions

Always.

Consequences

Reading ACL[n].ADDR returns incorrect address.

Workaround

None.

3.10 [12] QSPI: SCKFREQ is not functional at 96 MHz

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SCKFREQ is not functional at 96 MHz.

Conditions

Always.

Consequences

QSPI is not functional at 96 MHz SCK frequency when HFCLK is configured for the 128 MHz mode. QSPI is not functional at 48 MHz SCK frequency when HFCLK is configured for the 64 MHz mode.

Workaround

Use QSPI at 48 MHz SCK frequency when HFCLK is configured for the 128 MHz CPU frequency. Use QSPI at 24 MHz SCK frequency when HFCLK is configured for the 64 MHz CPU frequency.

3.11 [13] GPIO: Bits in LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

GPIO.PIN_CNF[n].SENSE is set to low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.

3.12 [14] TIMER: CC[6] and CC[7] are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

CC[6] and CC[7] are not functional.

Conditions

Using Capture/Compare channel registers 6 and 7.

Consequences

Channels 6 and 7 in registers CC, PUBLISH_COMPARE, TASKS_CAPTURE, SUBSCRIBE_CAPTURE, EVENTS_COMPARE, and ONESHOTEN are not functional.

Workaround

None.

3.13 [15] UARTE: Odd parity setting is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

Odd parity setting is not functional.

Conditions

Always.

Consequences

Odd parity setting in CONFIG is not functional.

Workaround

None.

3.14 [16] RADIO: POWER register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

POWER register is not functional.

Conditions

Always.

Consequences

POWER register is not functional.

Workaround

Reset all RADIO registers in firmware.

3.15 [18] I2S: 32-bit sample widths and 8-bit sample in a 16-bit half-frame are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

32-bit sample width is not functional.

Conditions

Using CONFIG.SWIDTH to configure I2S for 32Bit, 8BitIn16, 8BitIn32, 16BitIn32, or 24BitIn32.

Consequences

32-bit sample width is not functional.

Workaround

None.

3.16 [19] SPU: Flash memory space is divided into 32 regions of 32 KiB

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Flash memory space is divided into 32 regions of 32 KiB instead of 64 regions of 16 KiB.

Conditions

Always.

Consequences

FLASHREGION[n].PERM (n=32..63) registers are not functional.

Workaround

Use FLASHREGION[n].PERM (n=0..31) registers to configure the entire flash region.

3.17 [20] RTC: TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional.

Conditions

Always.

Consequences

TASKS_CAPTURE[n], SUBSCRIBE_CAPTURE[n], and SHORTS registers are not functional.

Workaround

None.

3.18 [21] TWIM: 1000 kbps baud rate is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

TWIM in 1000 kbps baud rate is not functional.

Conditions

TWIM is configured with 1000 kbps baud rate.

Consequences

TWIM in 1000 kbps baud rate is not functional.

Workaround

None.

3.19 [22] SPU: CPULOCK register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

CPULOCK register is not functional.

Conditions

Always.

Consequences

CPULOCK register is not functional.

Workaround

None.

3.20 [23] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST enabled

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SAADC stops working.

Conditions

Switching from single channel to multiple channels when BURST is enabled.

Consequences

SAADC internally locks up and does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration.

- Secure mode:

```
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```
NRF_SAADC_NS->TASKS_STOP = 1;
```

3.21 [26] CTRL-AP: APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional.

Conditions

Always.

Consequences

APPROTECT.DISABLE and SECUREAPPROTECT.DISABLE registers are not functional.

Workaround

None.

3.22 [27] CTRL-AP: STATUS register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

STATUS register is not functional.

Conditions

Always.

Consequences

STATUS register is not functional.

Workaround

None.

3.23 [28] TIMER: INTEN register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

INTEN register is not functional.

Conditions

Always.

Consequences

Timer interrupts cannot be configured using Timer INTEN register.

Workaround

Use INTENSET to enable interrupts and INTENCLR to disable interrupts.

3.24 [29] SWI: SWIRQ is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

SWIRQ is not functional.

Conditions

Always.

Consequences

SWIRQ is not functional.

Workaround

Use EGU or trigger interrupts in peripherals to generate interrupts.

3.25 [30] RESET: LCTRLAP field in RESETREAS register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

LCTRLAP field in RESETREAS register is not functional.

Conditions

Always.

Consequences

LCTRLAP field in RESETREAS register is not functional. Network core cannot detect if it has been reset by debugger using CTRL-AP.

Workaround

None.

3.26 [32] GPIO: GPIO pins assigned to network core do not retain their state in System OFF mode

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Conditions

GPIO pins are assigned to network core and device is in System OFF mode.

Consequences

GPIO pins do not retain their state.

Workaround

Before entering System OFF, configure application core to hold the GPIO pin's state.

3.27 [33] CLOCK: LFRC frequency starts drifting even if calibration task is triggered

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

LFRC frequency starts drifting even if calibration task is triggered.

Conditions

If any of following takes place:

- Triggering LFCLKSTOP task during calibration
- Changing LFCLK source from LFRC to any other source during calibration
- Starting calibration before LFRC is started

Consequences

LFRC frequency drifts. WDT and RTC may stop working even after soft reset.

Workaround

Avoiding conditions that cause this anomaly. If the anomaly is triggered, do a pin reset, System OFF reset, application watchdog reset, or power cycle.

3.28 [37] TWIM: First clock pulse after clock stretching may be too long or too short

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

When the TWI slave exits a clock stretching state, the first clock pulse from the master is too long or too short.

The following deviations from the normal clock pulse length can occur:

400 kHz

- Minimum: 0.7 µs
- Maximum: 3.0 µs

100 kHz

- Minimum: 0.7 µs
- Maximum: 11.0 µs

Conditions

TWI slave uses clock stretching.

Consequences

The slave may give an error condition due to a too long or too short clock pulse or the pulse may be lost. This depends on the slave clock stretching behavior.

Workaround

None.

3.29 [42] CLOCK: Reset value of HFCLKCTRL is invalid

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Reset value of HFCLKCTRL is invalid.

Conditions

Always.

Consequences

Application core has lower performance.

Workaround

Apply the following code at startup:

```
*((volatile uint32_t *)0x50039530ul) = 0xBEEF0044ul;
NRF_CLOCK_S->HFCLKCTRL = CLOCK_HFCLKCTRL_HCLK_Div2 << CLOCK_HFCLKCTRL_HCLK_Pos;
```

A workaround is implemented in MDK version 8.29.0 and later.

3.30 [43] QSPI: Reading QSPI registers after XIP might halt application CPU

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Application CPU halts.

Conditions

Init and start QSPI, use XIP, then write to or read any QSPI register starting from offset 0x600 and above.

Consequences

Application CPU halts.

Workaround

Trigger QSPI TASKS_ACTIVATE after XIP is used before accessing any QSPI register with an offset above 0x600.

3.31 [44] UARTE: TASKS_RESUME impacts UARTE

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

Issuing TASKS_RESUME results in bit(s) being set in the UARTE ERRORSRC register after it is enabled, even when not started.

Conditions

The internal state of a disabled UARTE changes when any of the tasks TASKS_RESUME, TASKS_STARTRX, and TASKS_STARTTX is triggered. These tasks are shared by UARTE, TWIM, TWIS, and SPIM.

Consequences

UARTE starts transmitting immediately after being enabled.

Workaround

Depending on which UARTE instance is affected, apply the following steps before enabling UARTE.

- If TXENABLE reads '1', trigger TASKS_STOPTX.
- If RXENABLE reads '1':
  - Enable UARTE.
  - Trigger TASKS_STOPRX.
  - Wait until RXENABLE reads '0'.
  - Clear ERRORSRC register.

The exact address depends on the UARTE instance. See the following table.

UARTE Instance	RXENABLE	TXENABLE
UARTE0:NS	0x40008564	0x40008568
UARTE0:S	0x50008564	0x50008568
UARTE1:NS	0x40009564	0x40009568
UARTE1:S	0x50009564	0x50009568
UARTE2:NS	0x4000A564	0x4000A568
UARTE2:S	0x5000A564	0x5000A568
UARTE3:NS	0x4000B564	0x4000B568
UARTE3:S	0x5000B564	0x5000B568

Table 2: Register addresses

3.32 [45] SPIM: Receive is not functional at 32 Mbps

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SPIM receive is not functional at 32 Mbps.

Conditions

Always.

Consequences

In 128 MHz mode, SPIM receive fails at 32 Mbps. In 64 MHz mode, SPIM receive fails at 16 Mbps. SPIM transmit works as per specification.

Workaround

Use SPIM at lower frequency. In 128 MHz mode, SPIM max receive frequency is 16 Mbps. In 64 MHz mode, SPIM max receive frequency is 8 Mbps.

3.33 [46] CLOCK: LFRC has higher current consumption

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

LFRC has higher power consumption.

Conditions

Always.

Consequences

Current consumption is higher than expected.

Workaround

Apply the following code in secure mode at startup:

```
*((volatile uint32_t *)0x5003254Cul) = 0;
```

This workaround is implemented in MDK version 8.29.0 and later.

3.34 [47] TWIM: I2C timing spec is violated at 400 kHz

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

The low period of the SCL clock is too short to meet the I2C specification at 400 kHz. The actual low period of the SCL clock is 1.25 µs while the I2C specification requires the SCL clock to have a minimum low period of 1.3 µs.

Conditions

Using TWIM at 400 kHz.

Consequences

TWI communication might not work at 400 kHz with I2C compatible devices.

Workaround

If communication does not work at 400 kHz with an I2C compatible device that requires the SCL clock to have a minimum low period of 1.3 µs, use 390 kHz instead of 400 kHz by writing 0x06200000 to the FREQUENCY register. With this setting, the SCL low period is greater than 1.3 µs.

3.35 [49] POWER: SLEEPENTER and SLEEPEXIT events are asserted after pin reset

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

EVENTS_SLEEPENTER and EVENTS_SLEEPEXIT are asserted.

Conditions

After device reset.

Consequences

If the firmware evaluates EVENTS_SLEEPENTER or EVENTS_SLEEPEXIT events, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore NRF_POWER->EVENTS_SLEEPENTER and NRF_POWER->EVENTS_SLEEPEXIT. Apply the following code after any reset:

```
For Application:
if (NRF_RESET_S->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_POWER_S->EVENTS_SLEEPENTER = 0;
    NRF_POWER_S->EVENTS_SLEEPEXIT = 0;
}
For Network:
if (NRF_RESET_NS->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_POWER_NS->EVENTS_SLEEPENTER = 0;
    NRF_POWER_NS->EVENTS_SLEEPEXIT = 0;
}
```

This workaround is implemented in MDK version 8.29.0 and later.

3.36 [50] SPU: Arm TrustZone region numbers for FICR, UICR, CACHEINFO, and CACHEDATA are incorrect

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Arm® TrustZone® region numbers for FICR, UICR, CACHEINFO, and CACHEDATA are incorrect.

Conditions

In secure state.

Consequences

TT-group of instructions cannot be used to test the security state of these addresses.

Workaround

None.

3.37 [51] SPU: Accessing FICR, UICR, CACHEINFO, or CACHEDATA from non-secure state gives bus error

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Accessing FICR, UICR, CACHEINFO, or CACHEDATA from non-secure state gives bus error.

Conditions

Accessing from non-secure state.

Consequences

Bus error.

Workaround

None.

3.38 [53] REGULATORS: Current consumption in normal voltage mode is higher in System ON idle

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Current consumption is higher in System ON idle.

Conditions

DC/DC mode is enabled in the VREGMAIN regulator and the device is in System ON idle.

Consequences

Current consumption is higher than expected.

Workaround

When enabling the DC/DC mode in VREGMAIN, apply the following code:

```
*((uint32_t *)0x50004728ul) =0x1;
```

3.39 [54] REGULATORS: Current consumption in normal voltage mode is higher in System ON idle and System OFF

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Network

Symptoms

Current consumption is higher in System ON idle and System OFF.

Conditions

DC/DC mode is enabled in the VREGRADIO regulator and the device is in System ON idle or System OFF mode.

Consequences

Current consumption is higher than expected.

Workaround

None.

3.40 [55] RESET: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Note: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
For Application:
if (NRF_RESET_S->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET_S->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
For Network:
if (NRF_RESET->RESETREAS & RESET_RESETREAS_RESETPIN_Msk)
{
    NRF_RESET->RESETREAS = ~RESET_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.29.0 and later.

3.41 [57] I2S: EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional.

Conditions

Always.

Consequences

EVENTS_FRAMESTART and PUBLISH_FRAMESTART registers are not functional.

Workaround

None.

3.42 [58] I2S: BYPASS in CONFIG.CLKCONFIG is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

BYPASS in CONFIG.CLKCONFIG is not functional.

Conditions

Always.

Consequences

BYPASS in CONFIG.CLKCONFIG is not functional.

Workaround

None.

3.43 [59] QDEC: QDEC0 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

QDEC0 is not functional.

Conditions

Always.

Consequences

QDEC0 is not functional.

Workaround

None.

3.44 [62] UICR: HFXOCNT register is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

HFXOCNT register is not functional.

Conditions

Always.

Consequences

HFXOCNT register is not functional. A fixed debounce value of 256 µs is used.

Workaround

Control the debounce time by using a timer if additional time is needed.

3.45 [64] REGULATORS: VREGMAIN has invalid configuration when CPU is running

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

The voltage on the DECD pin drops which can trigger a reset of the device.

Conditions

DC/DC mode is enabled in the VREGMAIN regulator and CPU is running.

Consequences

DC/DC mode cannot be enabled in the VREGMAIN regulator when CPU is running.

Workaround

Apply the following code after any reset:

```
*((volatile uint32_t *)0x5000470Cul) =0x29ul;
*((volatile uint32_t *)0x5000473Cul) =0x3ul;
```

This workaround is implemented in MDK version 8.30.0 and later.

3.46 [65] SAADC: Events are not generated when switching from scan mode to no-scan mode with BURST disabled

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SAADC stops working.

Conditions

Switching from single channel to multiple channels when BURST is disabled and acquisition time less than 10 us.

Consequences

SAADC internally locks up and does not generate the expected events.

Workaround

Execute the following code before changing the channel configuration.

- Secure mode:

```
NRF_SAADC_S->TASKS_STOP = 1;
```

- Non-secure mode:

```
NRF_SAADC_NS->TASKS_STOP = 1;
```

3.47 [69] REGULATORS: VREGMAIN configuration is not retained in System OFF

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Current consumption is excessive in System OFF mode.

Conditions

DC/DC mode is enabled in the VREGMAIN regulator and the device is in System OFF mode.

Consequences

Current consumption is higher than expected.

Workaround

Apply the following code after any reset:

```
*((uint32_t *)0x5000470Cul) =0x65;
```

3.48 [72] REGULATORS: Current consumption in high voltage mode is higher in System ON idle and System OFF

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

Current consumption is excessive in System ON idle or System OFF mode.

Conditions

DC/DC mode is enabled in the VREGH regulator and the device is in System ON idle or System OFF mode.

Consequences

Current consumption is higher than expected.

Workaround

None.

3.49 [73] TIMER: ONESHOTEN[n] registers are located at an incorrect address offset

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

ONESHOTEN[n] registers are located at an incorrect address offset.

Conditions

Always.

Consequences

ONESHOTEN[n] registers are located at an incorrect address offset.

Workaround

Use address offset 0x514 for ONESHOTEN[n] registers.

3.50 [74] TIMER: COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application, Network

Symptoms

COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register.

Conditions

Always.

Consequences

COMPARE[i]_STOP is located at an incorrect bit number in the SHORTS register.

Workaround

COMPARE[i]_STOP group starts at bit number 8. Use bit number 8+i for COMPARE[i]_STOP.

3.51 [79] QDEC: QDEC1 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

QDEC1 is not functional.

Conditions

Always.

Consequences

QDEC1 is not functional.

Workaround

None.

3.52 [80] PWM: PWM3 is not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

PWM3 is not functional.

Conditions

Always.

Consequences

PWM3 is not functional.

Workaround

None.

3.53 [81] SPIM: SPIM2 and SPIM3 are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SPIM2 and SPIM3 are not functional.

Conditions

Always.

Consequences

SPIM2 and SPIM3 are not functional.

Workaround

None.

3.54 [82] TWIM: TWIM2 and TWIM3 are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

TWIM2 and TWIM3 are not functional.

Conditions

Always.

Consequences

TWIM2 and TWIM3 are not functional.

Workaround

None.

3.55 [83] SPIS: SPIS2 and SPIS3 are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

SPIS2 and SPIS3 are not functional.

Conditions

Always.

Consequences

SPIS2 and SPIS3 are not functional.

Workaround

None.

3.56 [84] UARTE: UARTE2 and UARTE3 are not functional

This anomaly applies to IC Rev. Engineering A, build codes QKAA-AB0.

Domains

Application

Symptoms

UARTE2 and UARTE3 are not functional.

Conditions

Always.

Consequences

UARTE2 and UARTE3 are not functional.

Workaround

None.