ECE 3561 MT Register Set

12/03/19

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regLine Code Listing

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY regLine IS
      PORT (
            ABUS, BBUS                                    : INOUT
std_logic_vector(15 DOWNTO 0);
            Aload, Bload, Adrive, Bdrive, Arsel, Brsel  : IN std_logic
      );
END regLine;

ARCHITECTURE one OF regLine IS

      -- define subcomponents
      COMPONENT busdr IS
            PORT (
                  dr       : IN std_logic;
                  datain   : IN std_logic_vector(15 DOWNTO 0);
                  dataout  : OUT std_logic_vector(15 DOWNTO 0)
            );
      END COMPONENT;
      FOR ALL : busdr USE ENTITY work.busdr(one);

      COMPONENT reg16 IS
            PORT (
                  din   : IN std_logic_vector(15 DOWNTO 0);
                  dout  : OUT std_logic_vector(15 DOWNTO 0);
                  load  : IN std_logic
```

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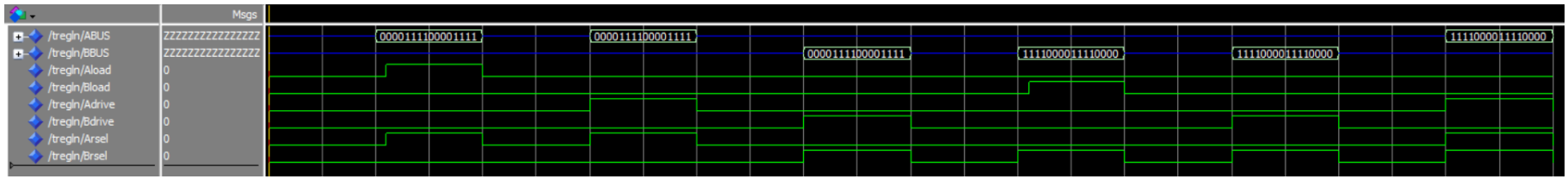
        );
    END COMPONENT;
    FOR ALL : reg16 USE ENTITY WORK.reg16(one);

    COMPONENT mux2_to_1x16 IS
        PORT (
            a, b    : IN std_logic_vector(15 DOWNTO 0);
            sa, sb  : IN std_logic;
            muxout  : OUT std_logic_vector(15 DOWNTO 0)
        );
    END COMPONENT;
    SIGNAL mux0_out, regOut : std_logic_vector(15 DOWNTO 0);
    SIGNAL regLoad, Abusdr_load, Bbusdr_load : std_logic;

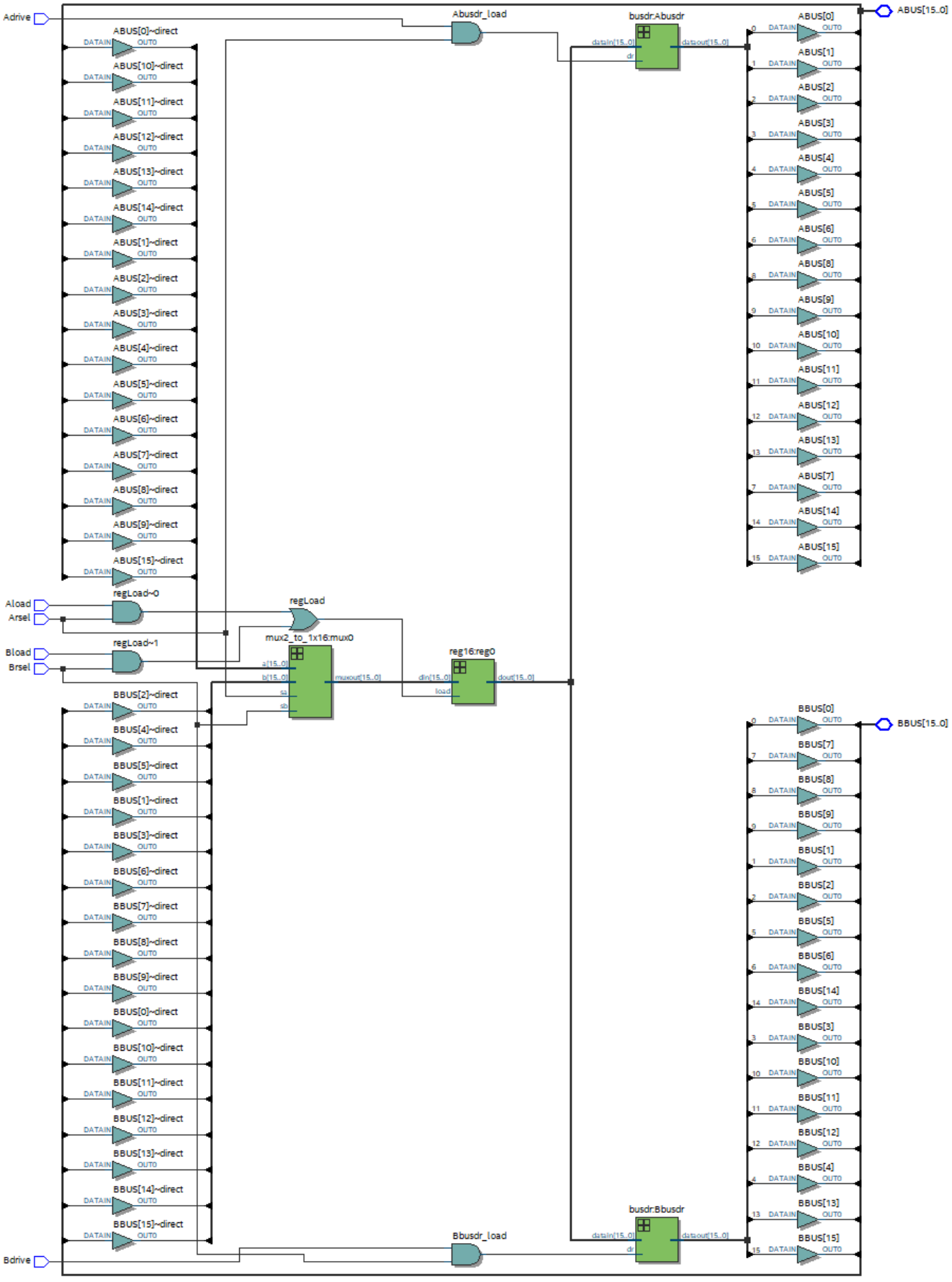
    BEGIN
        mux0 : mux2_to_1x16
        PORT MAP(ABUS, BBUS, Arsel, Brsel, mux0_out);

        reg0 : reg16      PORT MAP(mux0_out, regOut, regLoad);
        Abusdr : busdr    PORT MAP(Abusdr_load, regOut, ABUS);
        Bbusdr : busdr    PORT MAP(Bbusdr_load, regOut, BBUS);

        Abusdr_load <= (Adrive) AND (Arsel);
        Bbusdr_load <= (Bdrive) AND (Brsel);
        regLoad <= (Aload AND Arsel) OR (Bload AND Brsel);
END one;
```



Flow Status	Successful - Tue Dec 03 17:13:23 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	MT1Q
Top-level Entity Name	regLine
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	10 / 32,070 (< 1 %)
Total registers	16
Total pins	38 / 457 (8 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)


Adrive
Abusdr_load
busdr:Abusdr
datain[15..0]
dr
dataout[15..0]
ABUS[15..0]
ABUS[0]~direct
ABUS[10]~direct
ABUS[11]~direct
ABUS[12]~direct
ABUS[13]~direct
ABUS[14]~direct
ABUS[1]~direct
ABUS[2]~direct
ABUS[3]~direct
ABUS[4]~direct
ABUS[5]~direct
ABUS[6]~direct
ABUS[7]~direct
ABUS[8]~direct
ABUS[9]~direct
ABUS[15]~direct
ABUS[0]
ABUS[1]
ABUS[2]
ABUS[3]
ABUS[4]
ABUS[5]
ABUS[6]
ABUS[8]
ABUS[9]
ABUS[10]
ABUS[11]
ABUS[12]
ABUS[13]
ABUS[7]
ABUS[14]
ABUS[15]
Aload
Arsel
regLoad~0
regLoad
Bload
Brsel
regLoad~1
mux2_to_1x16:mux0
a[15..0]
b[15..0]
sa
sb
muxout[15..0]
reg16:reg0
din[15..0]
load
dout[15..0]
BBUS[2]~direct
BBUS[4]~direct
BBUS[5]~direct
BBUS[1]~direct
BBUS[3]~direct
BBUS[6]~direct
BBUS[7]~direct
BBUS[8]~direct
BBUS[9]~direct
BBUS[0]~direct
BBUS[10]~direct
BBUS[11]~direct
BBUS[12]~direct
BBUS[13]~direct
BBUS[14]~direct
BBUS[15]~direct
BBUS[0]
BBUS[7]
BBUS[8]
BBUS[9]
BBUS[1]
BBUS[2]
BBUS[5]
BBUS[6]
BBUS[14]
BBUS[3]
BBUS[10]
BBUS[11]
BBUS[12]
BBUS[4]
BBUS[13]
BBUS[15]
BBUS[15..0]
busdr:Bbusdr
Bbusdr_load
Bdrive

regSet Code Listing

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY regSet IS
      PORT (
            ABUS, BBUS                    : INOUT std_logic_vector(15 DOWNTO
0);
            Aload, Bload, Adrive, Bdrive  : IN std_logic;
            Aregno,Bregno                 : IN std_logic_vector(2 downto 0)
      );
END regSet;

ARCHITECTURE one OF regSet IS

      -- define subcomponents
      COMPONENT regLine IS
      PORT (
            ABUS, BBUS                                  : INOUT
std_logic_vector(15 DOWNTO 0);
            Aload, Bload, Adrive, Bdrive, Arsel, Brsel  : IN std_logic
      );
      END COMPONENT;
      COMPONENT pri3to8 IS
            PORT (pri : IN std_logic_vector(2 downto 0);
            p0,p1,p2,p3,p4,p5,p6,p7 : OUT std_logic);
      END COMPONENT;



      SIGNAL Arsel0,Arsel1,Arsel2,Arsel3,Arsel4,Arsel5,Arsel6,Arsel7 :
std_logic;
```

```
      SIGNAL Brsel0,Brsel1,Brsel2,Brsel3,Brsel4,Brsel5,Brsel6,Brsel7 :
std_logic;



      BEGIN

      regLine0 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel0,
Brsel0);

      regLine1 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel1,
Brsel1);

      regLine2 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel2,
Brsel2);

      regLine3 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel3,
Brsel3);

      regLine4 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel4,
Brsel4);

      regLine5 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel5,
Brsel5);

      regLine6 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel6,
Brsel6);

      regLine7 : regLine PORT MAP(ABUS,BBUS,Aload,Bload,Adrive,Bdrive,Arsel7,
Brsel7);

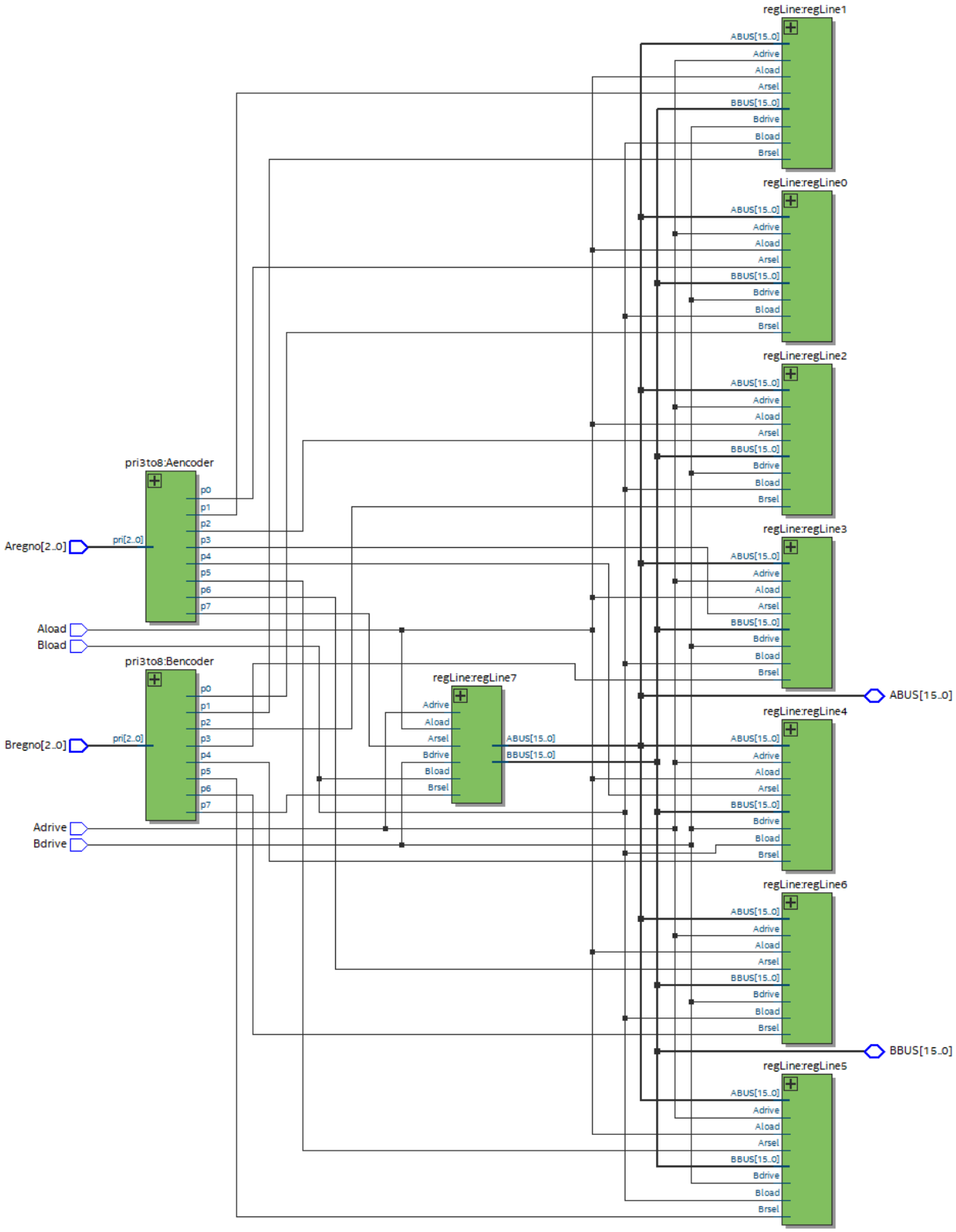


      Aencoder : pri3to8 PORT
MAP(Aregno,Arsel0,Arsel1,Arsel2,Arsel3,Arsel4,Arsel5,Arsel6,Arsel7);

      Bencoder : pri3to8 PORT
MAP(Bregno,Brsel0,Brsel1,Brsel2,Brsel3,Brsel4,Brsel5,Brsel6,Brsel7);


END one;
```

Flow Status	Successful - Tue Dec 03 17:54:34 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	MT1Q
Top-level Entity Name	regSet
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	174 / 32,070 (< 1 %)
Total registers	128
Total pins	42 / 457 (9 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)


regLine:regLine1
regLine:regLine0
regLine:regLine2
regLine:regLine3
regLine:regLine4
regLine:regLine6
regLine:regLine5
regLine:regLine7
ABUS[15..0]
Adrive
Aload
Arsel
BBUS[15..0]
Bdrive
Bload
Brsel
pri3to8:Aencoder
pri3to8:Bencoder
p0
p1
p2
p3
p4
p5
p6
p7
pri[2..0]
Aregno[2..0]
Bregno[2..0]
Aload
Bload
Adrive
Bdrive
ABUS[15..0]
BBUS[15..0]