MT ALU Assignment

ECE 3561, 12/04/19

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Alu Code Listing

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY alu IS
  PORT (a,b : IN std_logic_vector (15 downto 0);
        cin,arlo : IN std_logic;
      ltt : std_logic_vector(0 to 3);
        res : OUT std_logic_vector (15 downto 0);
        cout : OUT std_logic);
END alu;

ARCHITECTURE one OF alu IS

      COMPONENT mux2_to_1x16 IS
   PORT (a,b : IN std_logic_vector(15 downto 0);
         sa,sb : IN std_logic;
         muxout : OUT std_logic_vector(15 downto 0));
END COMPONENT;

COMPONENT log16 IS
  PORT(a,b : IN std_logic_vector(15 downto 0);
       res : OUT std_logic_vector(15 downto 0);
       ltt : IN std_logic_vector(0 to 3));
END COMPONENT;

COMPONENT add16 IS
  PORT (a,b : IN std_logic_vector (15 downto 0);
        cin : IN std_logic;
```

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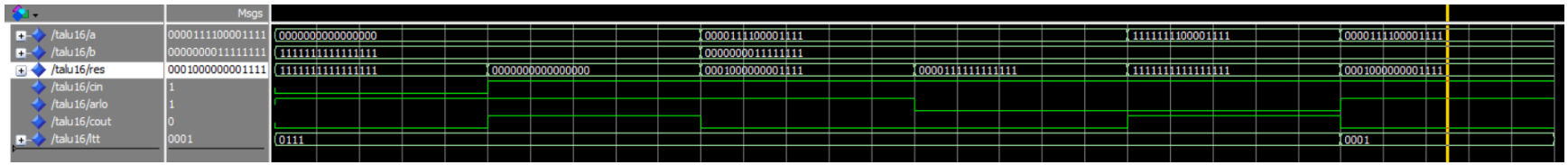
        sum : OUT std_logic_vector (15 downto 0);
        cout : OUT std_logic);
END COMPONENT;


SIGNAL lu_result,addr_result : std_logic_vector (15 downto 0);
SIGNAL notArlo : std_logic;
BEGIN

logicUnit0 : log16 PORT MAP(a,b,lu_result,ltt);
addr0 : add16 PORT MAP(a,b,cin,addr_result,cout);
mux0 : mux2_to_1x16 PORT MAP(addr_result,lu_result,arlo,notArlo,res);

notArlo <= not(arlo);
END one;
```


Msgs
/talu16/a
0000111100001111
/talu16/b
0000000011111111
/talu16/res
0001000000001111
/talu16/cin
1
/talu16/arlo
1
/talu16/cout
0
/talu16/ltt
0001
0000000000000000
0000111100001111
1111111100001111
0000111000011111
1111111111111111
0000000011111111
0001000000001111
0000111111111111
1111111111111111
0001000000001111
0111
0001