MT3

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ECE3561

11/8/2019

addSub

```
-- File: alu.vhdl
-- Engineer: Matt Gambill
-- Date: 11/8/2019
-- Synopsis: File Defines a 16 bit add/subtractor with overflow
detection
-- operation =0 is addition, operation=1 is subtraction
-- if the unit overflows the operation is invalid
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;

ENTITY addSub IS
     PORT
     (
          operation : IN std_logic;
          A, B      : IN std_logic_vector(15 DOWNTO 0);

          sum  : OUT std_logic_vector(15 DOWNTO 0);
          overflow,Cout  : OUT std_logic);
END addSub;

ARCHITECTURE rtl OF addSub IS
SIGNAL Cvec : std_logic_vector(16 DOWNTO 0);
SIGNAL Aop  : std_logic_vector(15 DOWNTO 0);
BEGIN
```

```
     Cvec(0)           <= operation;                          --
operation could also be named Cin

     Aop               <= NOT A WHEN operation = '1' ELSE A; -- Take
2's Complement if subtraction operation is asserted


     sum               <= Aop XOR B XOR Cvec(15 DOWNTO 0);

     Cvec(16 DOWNTO 1) <= (Aop AND B) OR (Aop AND Cvec(15 DOWNTO 0))
OR (B AND Cvec(15 DOWNTO 0));


     overflow          <= Cvec(16) XOR Cvec(15);

  Cout              <= Cvec(16);

END rtl;
```

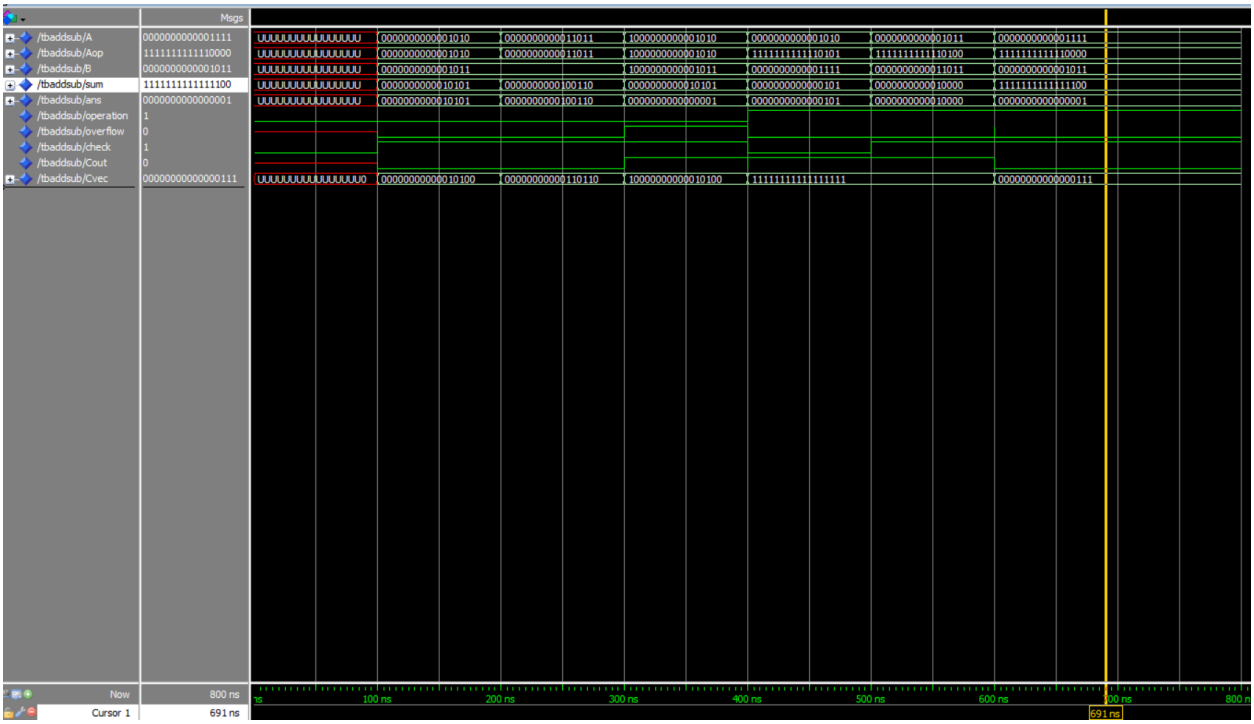
Test Bench

```
-- File: tbalu.vhdl

-- Engineer: Matt Gambill

-- Date: 11/8/2019

-- Synopsis: File Defines a 16 bit add/subtractor with overflow
detection

-- operation =0 is addition, operation=1 is subtraction

-- if the unit overflows the operation is invalid

LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

USE ieee.std_logic_arith.ALL;


entity tbaddSub is

end entity;


ARCHITECTURE one of tbaddSub is

  SIGNAL A,B,sum,ans,Aop  : std_logic_vector(15 DOWNTO 0);

  SIGNAL operation, overflow, check,Cout  : std_logic := '0';

  SIGNAL Cvec : std_logic_vector(16 DOWNTO 0);

  BEGIN
```

```
  dut : entity work.addSub
  port map(operation =>
operation,A=>A,B=>B,Cvec=>Cvec,sum=>sum,Aop=>Aop,overflow=>overflow,Co
ut=>Cout);


  simulation : process
  begin
    operation <='0';
    wait for 100 ns;
    A   <= "0000000000001010";
    B   <= "0000000000001011";
    ans <= "0000000000010101";
    if (sum = ans) then
      check <= '1';
    else
      check <='0';
    end if;

    wait for 100 ns;
    operation <='0';
    A   <= "0000000000011011";
    B   <= "0000000000001011";
    ans <= "0000000000100110";
    if (sum = ans) then
      check <= '1';
    else
      check <='0';
    end if;

    wait for 100 ns;
    operation <='0';
```

```
A   <= "1000000000001010";
B   <= "1000000000001011";
ans <= "0000000000000001";
if (ans(0) = overflow) then
  check <= '1';
else
  check <='0';
end if;

-- Subtraction test

wait for 100 ns;
operation <='1';
A   <= "0000000000001010";
B   <= "0000000000001111";
ans <= "0000000000000101";
if (sum = ans) then
  check <= '1';
else
  check <='0';
end if;

wait for 100 ns;
operation <='1';
B   <= "0000000000011011";
A   <= "0000000000001011";
ans <= "0000000000010000";
if (sum = ans) then
  check <= '1';
else
```

```
      check <='0';
    end if;

    wait for 100 ns;
    operation <='1';
    B   <= "0000000000001011";
    A   <= "0000000000000000";
    ans <= "0000000000000001";
    if (ans(0) = overflow) then
      check <= '1';
    else
      check <='0';
    end if;
    wait for 200 ns;
    wait;
  end process;


end ARCHITECTURE one;
```



Flow Status	Successful - Fri Nov 08 23:29:27 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	MT1Q
Top-level Entity Name	addSub
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	27 / 32,070 (< 1 %)
Total registers	0
Total pins	51 / 457 (11 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)