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ECE 3561

MT2

**Nor\_16\_wide**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

Entity nor\_16\_wide IS

port(input : IN std\_logic\_vector(15 downto 0); z : OUT std\_logic);

End nor\_16\_wide;

ARCHITECTURE BEHAVIORAL OF nor\_16\_wide IS

BEGIN

z <= not(input(0) or input(1) or input(2) or input(3) or input(4) or input(5) or input(6) or input(7) or input(8) or input(9) or input(10) or input(11) or input(12) or input(13) or input(14) or input(15));

END BEHAVIORAL;

**Test Bench**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_arith.ALL;

ENTITY tbnor\_16\_wide IS

END ENTITY;

ARCHITECTURE one OF tbnor\_16\_wide IS

COMPONENT nor\_16\_wide

PORT (

input : IN std\_logic\_vector(15 DOWNTO 0);

z : OUT std\_logic);

END COMPONENT;

SIGNAL s1 : std\_logic\_vector(15 DOWNTO 0) := "0000000000000000";

SIGNAL z : std\_logic := '0';

BEGIN

ng16\_0 : nor\_16\_wide PORT MAP(s1,z);

process

begin

FOR i IN 0 TO 15 LOOP

s1(i) <= '1';

WAIT for 10 ns;

s1 <= "0000000000000000";

WAIT for 10 ns;

END LOOP;

end process;

END ARCHITECTURE;





