**MT4**

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**ECE3561**

**dff\_en**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

Entity dff\_en IS

port(d,clk,en : IN std\_logic; q : OUT std\_logic);

End dff\_en;

ARCHITECTURE BEHAVIORAL OF dff\_en IS

BEGIN

Process

BEGIN

Wait UNTIL clk='1' AND clk'event;

IF en='1' THEN

q<=d;

END IF;

END PROCESS;

END BEHAVIORAL;

**Test Bench**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

ENTITY tbdff\_en IS

END tbdff\_en;

ARCHITECTURE one OF tbdff\_en IS

COMPONENT dff\_en

port(d,clk,en : IN std\_logic; q : OUT std\_logic);

END COMPONENT;

SIGNAL d,q,en : std\_logic := '0';

SIGNAL s1 : std\_logic\_vector(3 downto 0);

signal i : integer := 0;

SIGNAL clk : std\_logic :='1';

BEGIN

dff0 : dff\_en PORT MAP(d,clk,en,q);

clk <= NOT clk AFTER 10 ns;

PROCESS(clk)

BEGIN

IF (i<4) THEN

s1 <= conv\_std\_logic\_vector(i, s1'length);

d <= s1(1);

i <= i + 1;

ELSE

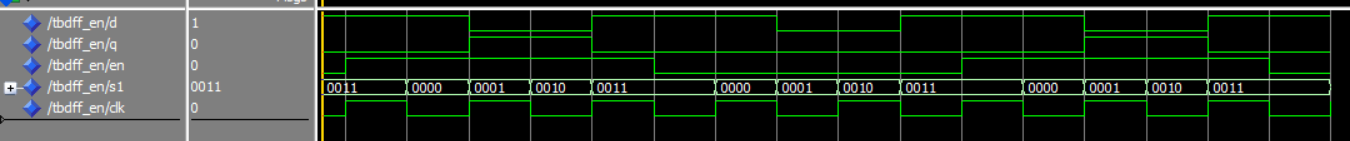
i<=0;

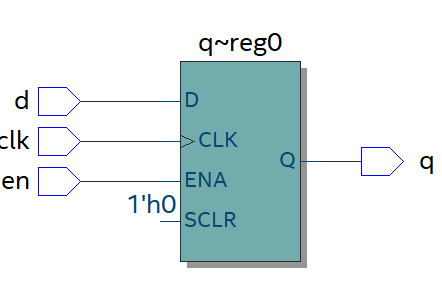
en <= NOT en;

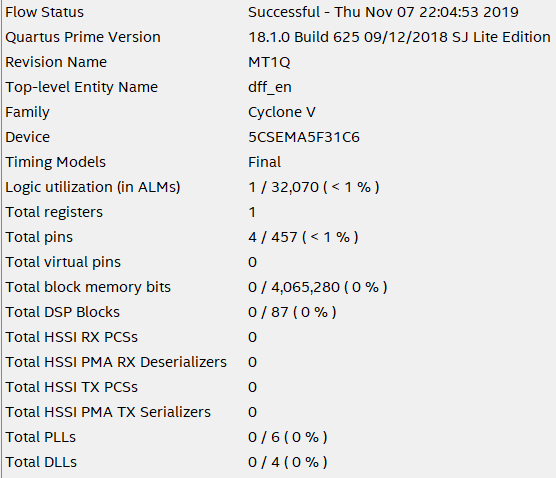
END IF;

END PROCESS;

END one;







**dff\_en\_16\_wide**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

Entity dff\_en\_16\_wide IS

port(clk : IN std\_logic; d,en : IN std\_logic\_vector(15 downto 0); q : OUT std\_logic\_vector(15 downto 0));

End dff\_en\_16\_wide;

ARCHITECTURE BEHAVIORAL OF dff\_en\_16\_wide IS

BEGIN

Process

BEGIN

Wait UNTIL clk='1' AND clk'event;

for i in 15 downto 0 loop

IF en(i)='1' THEN

q(i)<=d(i);

END IF;

end loop;

END PROCESS;

END BEHAVIORAL;

**Test Bench**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

ENTITY tbdff\_en\_16\_wide IS

END tbdff\_en\_16\_wide;

ARCHITECTURE one OF tbdff\_en\_16\_wide IS

COMPONENT dff\_en\_16\_wide

port(clk : IN std\_logic; d,en : IN std\_logic\_vector(15 downto 0); q : OUT std\_logic\_vector(15 downto 0));

END COMPONENT;

SIGNAL d,q,en : std\_logic\_vector(15 downto 0) := "0000000000000000";

SIGNAL s1 : std\_logic\_vector(3 downto 0);

signal i : integer := 0;

SIGNAL clk : std\_logic :='1';

BEGIN

dff0 : dff\_en\_16\_wide PORT MAP(clk, d,en,q);

clk <= NOT clk AFTER 10 ns;

PROCESS(clk)

BEGIN

IF (i<4) THEN

s1 <= conv\_std\_logic\_vector(i, s1'length);

i <= i + 1;

ELSE

i<=0;

en <= NOT en;

END IF;

for i in 15 downto 0 loop

d(i) <= s1(1);

end loop;

END PROCESS;

END one;

