**MT5**

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**BUSDR\_1\_WIDE**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY BUSDR\_1\_WIDE IS

PORT (

drive : IN STD\_LOGIC;

data : IN STD\_LOGIC;

intbus : OUT STD\_LOGIC

);

END BUSDR\_1\_WIDE;

ARCHITECTURE Behavioral OF BUSDR\_1\_WIDE IS

BEGIN

intbus <= data WHEN (drive = '1') ELSE 'Z';

END Behavioral;

**Test Bench**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

ENTITY tbBUSDR\_1\_WIDE IS

END tbBUSDR\_1\_WIDE;

ARCHITECTURE one OF tbBUSDR\_1\_WIDE IS

COMPONENT BUSDR\_1\_WIDE

PORT (

drive : IN STD\_LOGIC;

data : IN STD\_LOGIC;

intbus : OUT STD\_LOGIC

);

END COMPONENT;

SIGNAL en,data\_i,data\_o : std\_logic := '0';

SIGNAL s1 : std\_logic\_vector(3 downto 0);

signal i : integer := 0;

SIGNAL clk : std\_logic :='1';

BEGIN

busdr0 : BUSDR\_1\_WIDE PORT MAP(en,data\_i,data\_o);

clk <= NOT clk AFTER 10 ns;

PROCESS(clk)

BEGIN

IF (i<4) THEN

s1 <= conv\_std\_logic\_vector(i, s1'length);

data\_i <= s1(1);

i <= i + 1;

ELSE

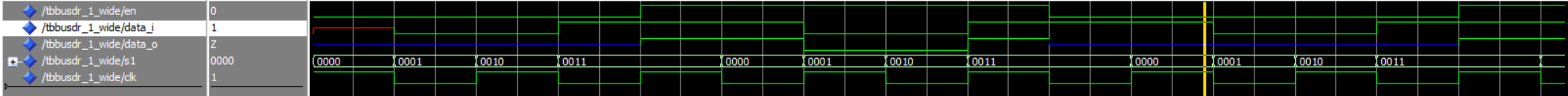
i<=0;

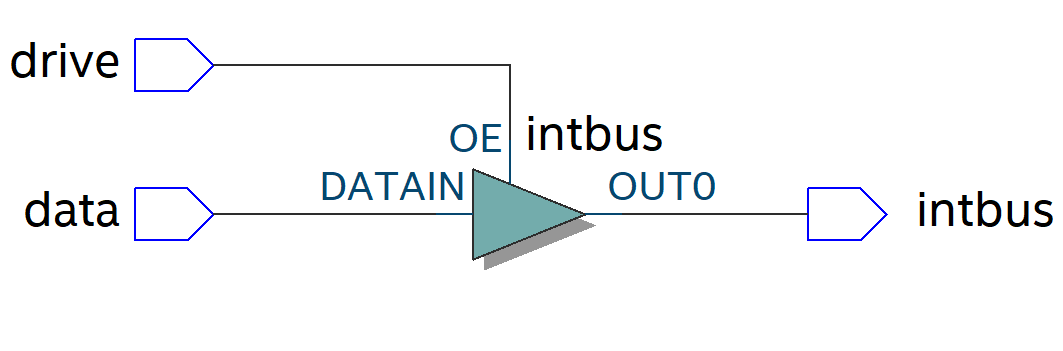
en <= NOT en;

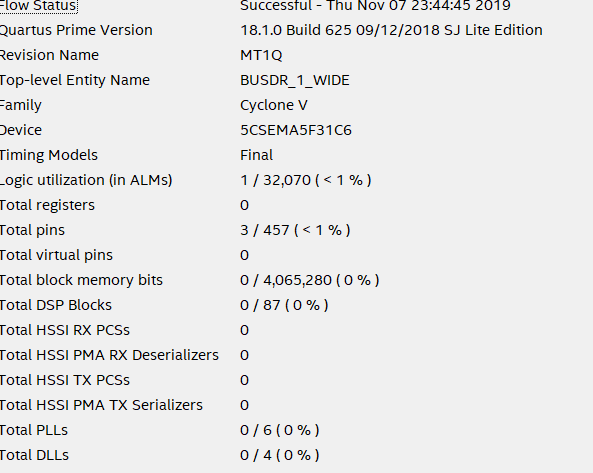
END IF;

END PROCESS;

END one;

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**BUSDR\_16\_WIDE**

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY busdr\_16\_wide IS

PORT (

drive : IN STD\_LOGIC;

data : IN STD\_LOGIC\_VECTOR(15 DOWNTO 0);

intbus : OUT STD\_LOGIC\_VECTOR(15 DOWNTO 0)

);

END busdr\_16\_wide;

ARCHITECTURE Behavioral OF busdr\_16\_wide IS

BEGIN

intbus <= data WHEN (drive = '1') ELSE "ZZZZZZZZZZZZZZZZ";

END Behavioral;

**Test Bench**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

ENTITY tbBUSDR\_16\_WIDE IS

END tbBUSDR\_16\_WIDE;

ARCHITECTURE one OF tbBUSDR\_16\_WIDE IS

COMPONENT BUSDR\_16\_WIDE

PORT (

drive : IN STD\_LOGIC;

data : IN STD\_LOGIC\_VECTOR(15 DOWNTO 0);

intbus : OUT STD\_LOGIC\_VECTOR(15 DOWNTO 0)

);

END COMPONENT;

SIGNAL data\_i,data\_o : std\_logic\_vector(15 downto 0) := "0000000000000000";

SIGNAL s1 : std\_logic\_vector(3 downto 0);

signal i : integer := 0;

SIGNAL en : std\_logic :='0';

SIGNAL clk : std\_logic :='1';

BEGIN

busdr0 : BUSDR\_16\_WIDE PORT MAP(en,data\_i,data\_o);

clk <= NOT clk AFTER 10 ns;

PROCESS(clk)

BEGIN

IF (i<4) THEN

s1 <= conv\_std\_logic\_vector(i, s1'length);

i <= i + 1;

ELSE

i<=0;

en <= NOT en;

END IF;

for i in 15 downto 0 loop

data\_i(i) <= s1(1);

end loop;

END PROCESS;

END one;

