

MONASH UNIVERSITY

HONOURS THESIS

# Thin oxides in graphene devices



IMAGE  
PLACEHOLDER

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# Abstract

I present a review of the use of graphene in electronic devices, both in its shortfalls and exciting properties. The electronic structure is detailed, along with various scattering sources that affect electron transport and ultimately the goal of room temperature, electronic devices. Considering heterostructures and the use of other materials to enhance graphene, I discuss the potential use of hafnium dioxide, and other oxides, as an excellent gate dielectric material for potential use in graphene field-effect devices.

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# Foreword

This thesis serves the purpose presenting the conclusions of my research into thin oxides on graphene. I will be arguing , and how that fits into a bigger picture of materials science and particular applications.

In chapter 1, I will outline what I hope to achieve in this project. I begin by discussing the theoretical properties of graphene and why it has attracted so much interest as an electronic material. I will also describe some challenges facing new computing technologies, including the use of dielectrics, and how my work contributes to realising solutions to new generations of this technology. I will outline a theoretical and experimental summary of the results to date seen in introducing dielectrics to graphene.

In chapter 2, I describe the various ways of producing and identifying graphene in lab use, and the characterisations I have conducted. This will include our use of atomic force microscopy (AFM), optical microscopy and Raman spectroscopy.

I will then describe the devices and measurements I have made in chapter 3. This will regard connections to devices, which allow the measurements I have perform, and the processes used to fabricate our devices. I have made graphene devices using lithography and evaporation methods, to create electrical contacts. I will also describe the oxides I have investigated in this chapter, and the methods I have used to transfer them.

In chapter 4 I will present the data and results from my measurements of the respective devices which will be placed on  $\text{SiO}_2$ . The results to here will be compared alongside data after stamping the same devices with thin oxides in chapter 5.

# **Chapter 1**

## **Introduction**

### **1.1 Preface**

The mechanical exfoliation of atomically thin materials in 2004 sparked a flurry of research into many materials with unique properties. Graphene, the first of these, rose to prominence in research and has begun finding applications in industrial contexts.

Materials that are two dimensional restrict the movement of electrons to a plane. Because of this, these materials exhibit unique electronic properties. A clear example of this is a hexagonal lattice of carbon atoms, or graphene, which gives rise to a 'dirac' point in the band structure (see section 1.3.1).

### **1.2 Transistors - the field effect**

#### **1.2.1 Conductivity in FETs**

#### **1.2.2 Mobility in FETs**

### **1.3 Graphene**

#### **1.3.1 Electronic properties**

Why is it a good conductor?

Hybridisation

Electronic dispersion

Charged puddling

## 1.4 Transport and scattering in graphene

1.4.1 Charged impurities

1.4.2 Phonon scattering

1.4.3 Dielectric screening

Charge screening

Fine structure constant

Tuning the fine structure constant

High  $\kappa$  materials

1.4.4 Remote phonon scattering

1.5

# Chapter 2

## Experimental techniques

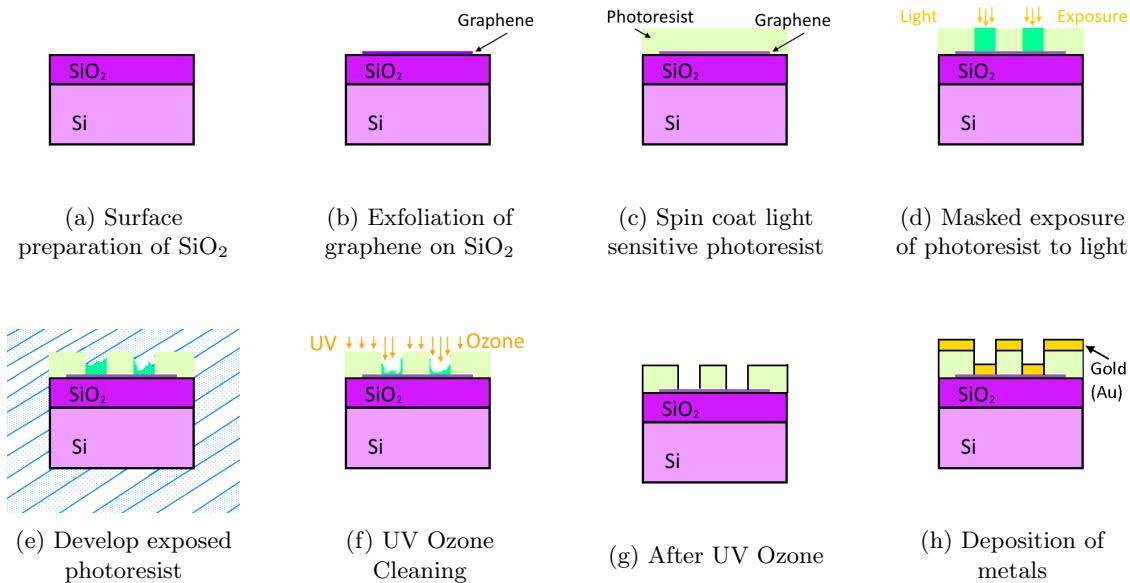
Two aspects are involved in performing electronic measurements of materials, namely fabrication and measurement techniques.

Physical devices containing graphene need to be fabricated allow measurements to take place. This primarily deals with the production of materials (graphene, oxides) and the processes to develop connectable devices. Some of the tools and techniques used include lithography, electron beam evaporation, and etching. The processes used in this project are detailed in section 2.1.

To measure the properties of graphene, particular experimental methods and procedures are required to control the environment and obtain useful data. Section 2.2 primarily deals with the operation of the experimental apparatus used to measure the electronic properties of graphene.

### 2.1 Fabrication

To create graphene devices where we can measure the electronic properties referenced in sections 1.2 and 1.3.1, a variety of steps need to be taken in order to probe electronic flow. Figure 2.1 describes the general process for exfoliated graphene (see section 2.1.3), the bulk of the devices.



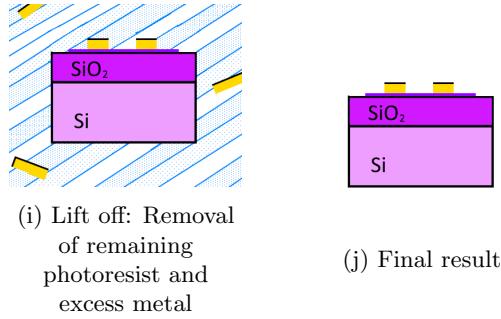


Figure 2.1: Device fabrication process from exfoliated graphene to a FET device.

### 2.1.1 Graphene

Since the realisation of graphene in 2004<sup>[1]</sup>, much research has been focused to finding efficient ways of producing large amounts of graphene<sup>[2]</sup>. Originally, the first samples ever created which have primarily been used for sensitive measurements have been conducted using a method of exfoliation (section 2.1.3). These samples typically exhibit better electronic properties than those produced by other methods. Since 2008/2009, CVD (section 2.1.2) of carbon to create graphene films has provided another prominent method to produce large films for industrial scale applications. In particular, growth of graphene on copper sheets<sup>[3]</sup> has been a reliable way producing these large uniform sheets.

There are other methods not used in this thesis, such as epitaxial growth of graphene via SiC uses heating to boil off silicon atoms to form a layer of graphene on it's surface.

### 2.1.2 Chemical vapour deposition graphene

Graphene can be growth via chemical vapour deposition, resulting in particularly large uniform sheets when grown on copper<sup>[3]</sup>. This is a widely used method of producing readily available graphene. Graphene produced in this fashion needs to be transferred onto an insulating layer of oxide to create a gate, or be gated by using a deposition method. We have used the former, which will introduce some cracks, folding and wrinkling disorder when transferred.

To achieve this, a process<sup>[4]</sup> using poly-methyl methacrylate (PMMA) is used to 'wet transfer' CVD graphene onto a  $\text{SiO}_2$  wafer with pre-deposited Au pads, from a masked e-beam deposition (see section 2.1.6).

Copper grown CVD graphene, covered by PMMA, is placed in an ammonium persulfate solution, dissolving the copper. The remaining graphene and PMMA remains hydrophobic on the surface, and allows substrates to collect the sample beneath. After the transfer is complete, the sample is soaked in PG remover to clean off PMMA. An example device is shown in fig. 2.2.

We seldom used this technique to produce graphene devices due to the area coverage requirement of an oxide as well as the lack of geometric definition.

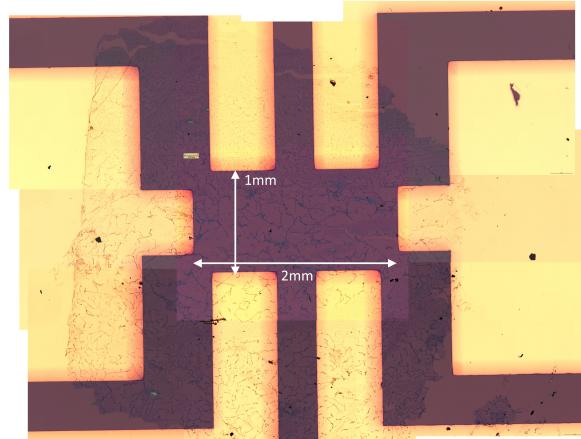


Figure 2.2: CVD graphene grown on Cu transferred onto  $\text{SiO}_2$  and Au pads. The contrast differences due to the autoexposure of the camera software.

### 2.1.3 Exfoliation of graphene

Exfoliation in materials refers to the cleaving thin layers (or leaves) off a larger sample, and acquiring them onto the substrate. We exfoliate graphene onto Si/SiO<sub>2</sub> wafers. Generally exfoliation involves pressing tape/surfaces against a bulk crystal (such as highly orientated pyrolytic graphite (HOPG), Kish graphite, natural graphite, or graphenium). Due to van der Waals interactions, layers of graphite are transferred to the desired surface. By repeated peeling of the same tape, a thin coverage can be obtained and then transferred onto substrates, such as SiO<sub>2</sub>. Exfoliation can take a variety of forms, from Geim's method<sup>[5]</sup>, to directly applying scotch tape to HOPG and then pressing against SiO<sub>2</sub>, before peeling the tape off.

Huang *et al* investigated a reliable method of exfoliation to produce large area and high quality samples<sup>[6]</sup>, which has been widely cited. Tape with graphite flakes is brought into contact with a silicon dioxide wafer, and an annealing process of heating the tape and wafer for 2-5m at  $\sim 100^{\circ}\text{C}$  on a conventional lab hot plate is used. After allowing cooling to room temperature, the tape is removed. They find under optical microscopy that graphene flakes with uniform thickness routinely range from  $\sim 20\mu\text{m}$  to above  $100\mu\text{m}$ . In this context, annealing is expected to increase traction due to the remove of gas molecules trapped between SiO<sub>2</sub> and graphite.

The following steps make up the process of exfoliation we optimised:

1. (Optional) Use a plasma ashing/etcher with an argon/oxygen plasma to the clean surface of SiO<sub>2</sub>. This can increase the adhesion between graphene and the surface by removing organic absorbates<sup>[6]</sup>. Alternatively, clean wafers of Si/SiO<sub>2</sub> in acetone, tilted in an ultrasonic bath for 30s. Repeat the same in isopropanol, before rinsing in ethanol and drying with N<sub>2</sub> gas.
2. Cleave a layer of HOPG graphite by using scotch tape to peel off a thick film.
3. Use a secondary piece of scotch tape to exfoliate a thinner layer off master tape. Ensure good coverage by reattaching a couple times.
4. Attach Si/SiO<sub>2</sub> wafers to graphite covered areas of secondary tape. The SiO<sub>2</sub> face should be contacting the graphite.
5. Attach the tape and wafers firmly to a glass slide, before using a tissue/cotton-bud to press the surface of the tape into the wafer.
6. Place glass slide on a hotplate at  $100^{\circ}\text{C}$  for two minutes, before removing and cooling for two minutes.
7. Slowly peel tape at an acute angle from the glass slide, roughly at 6s per cm over the wafer.

We found success can depend on HOPG crystal, given we tried cleavage using ZYA and ZYB quality crystals and had repeated failure. Changing to a new ZYA crystal provided immediate results using the same process.

After exfoliation, graphene was identified under a 20x microscope lens, raster scanning across wafers to identify any samples big enough. Typically to make a device using photolithography, a sample of graphene required a minimum  $8\mu\text{m}$  in dimensional length to be useful.

### 2.1.4 Lithography

Lithography can be used to create polymer structures that allow the deposition of desired material in 2D geometries. This is used to create electrical contacts onto graphene. This process and the adjustments made for fabricating our devices are described in this section.

Lithography typically consists of three main steps.

1. Spin coating - covering a sample with a uniform layer of polymer, and baking it on.

2. Exposure - The polymer undergoes chemical changes to its properties when exposed to particular wavelengths of light. This differentiates exposed areas to those unexposed.
3. Developer solution - developer solution removes intended areas of photoresist to create structures.

### Spin coating photoresists

A spin coater is used to deposit thin films of materials. A vacuum holds a sample on the spinner, before drops of photoresist are introduced to the sample, which is then spun over sometime to achieve a uniform thickness of photoresist. Baking on a hotplate follows to set the photoresist layer on the sample.

Photoresists vary in their spinning thickness, but also their exposure rates. Positive photoresists dissolve in particular developer solutions when exposed to light, while negative photoresists dissolve if not exposed to light. We have only used positive photoresists, as we have primarily been creating structures for deposition, and not etching material where you want the bulk of the wafer exposed.

**HMDS & AZ-1512HS** Initially devices were fabricated using the AZ-1512HS polymer, with the additional use of hexamethyldisilazane (HMDS) as an adhesion promoter between  $\text{SiO}_2$  and AZ-1512HS. Devices were spun initially for 10 s at 1000 rpm, before being spun between 2000 and 3000 rpm for 30 s, per resist layer. This leaves a thickness of 1.7  $\mu\text{m}$  to 1.39  $\mu\text{m}$ <sup>[7]</sup>. Devices were then baked at 100 °C for 1 minute.

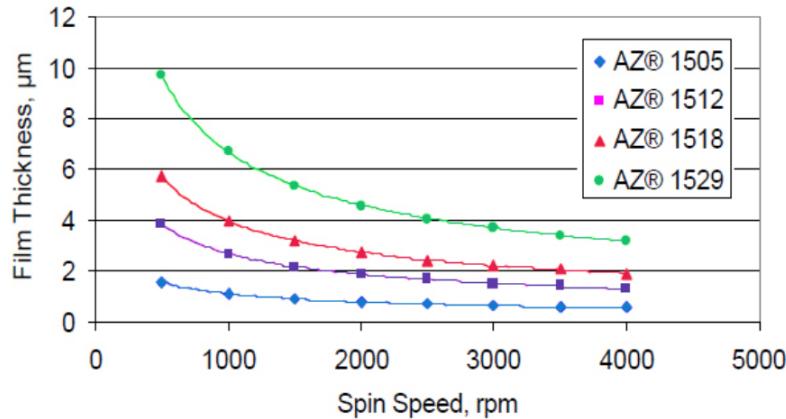


Figure 2.3: Spin curve of AZ-1512HS (Source: EMD Performance Materials<sup>[8]</sup>)

**Skin issues with HMDS** When using HMDS and AZ-1512HS in conjunction, significant amounts of deposition remenants were found on samples as seen in fig. 2.4.

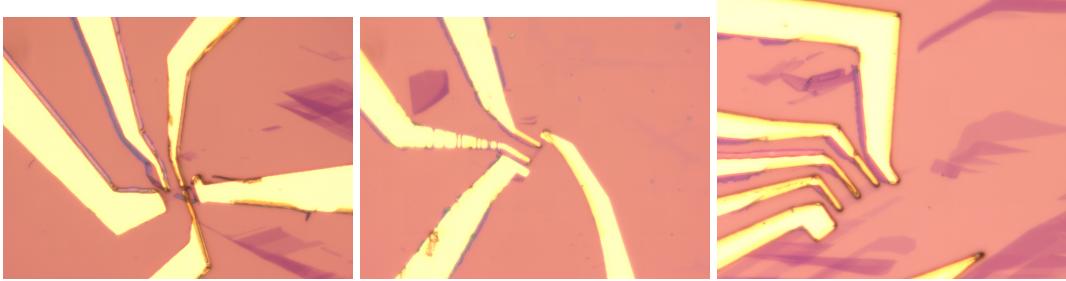


Figure 2.4: Material remnants from lithography. Gold edges exhibit a bluish remnant edge.

This is likely due to metal deposition (i.e. Chromium, see section 2.1.6) forming layers on the sides of lithography wells, as the skins have very similar geometry to that of either the wells or the edges. The spinning speeds give resist heights (i.e. the well edge heights) roughly the same as feature width ( $\approx 1\mu\text{m}$  minimum), matching the observed result.

Ultrasonication (see section 2.1.7) can be used to attempt to remove edges after lift off, however there is risk of damaging samples of graphene.

**LOR-1A & AZ-1512HS** The issue with a single layer photoresist processes, outlined above, is that well edges allow deposited materials to adhere, leaving 'skins'. One way to prevent this from happening is to use a multilayer process. Two resist layers are spun onto the sample, with the bottom film being more sensitive to the lithography process than the top (i.e., develops faster, or is more sensitive to exposure). When developed, the bottom layer *undercuts* the top layer, stopping adhesion to edges of the well when material is deposited. This process is depicted in fig. 2.5.

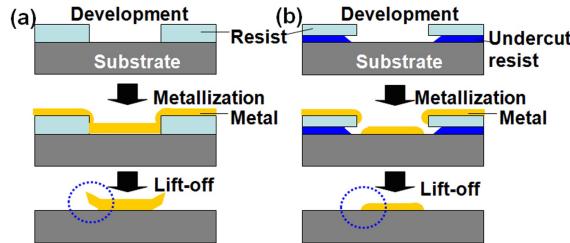


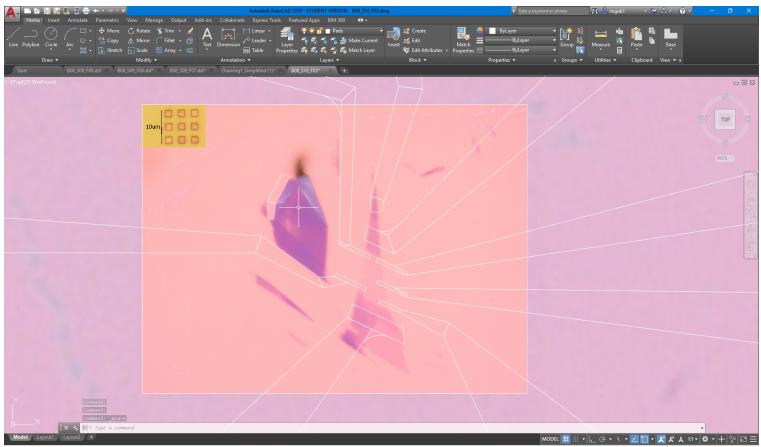
Figure 2.5: Bilayer lithography process (Source: Park *et al*<sup>[9]</sup>)

LOR-1A is an actinic lift off resist, responding to UV light from 240 nm to 290 nm<sup>[10]</sup>. When the resist films are exposed to the developer, LOR-1A is removed below an overhanging AZ1512-HS layer due to additional development, leaving the desired undercut effect.

## Exposure

After spinning, a mask writer tool is used to expose the wafer and resist films to UV light. A mask writer is composed of a mask, or a DMD (digital micro-mirror device) which allows filtering of pixel like squares, based on an input image. Actinic reactions occur from the UV light with the photoresist, forming desired pad structures in the resist. Prepared CAD files are used to generate masks used by the DMD as seen in fig. 2.6.

An important parameter in the mask writing process is the exposure time, which affects the ability to develop fine structures. By using an array of different exposure times (fig. 2.7), the optimal feature result was found for a typical developing time.



(a) DMD masks created using Autocad™. Additional structures are created to help position the mask when using a 20x lens, as graphene can be difficult to see in a mask writer tool.



(b) Photolithography structure from mask writing and development.

Figure 2.6: Photolithography mask writing

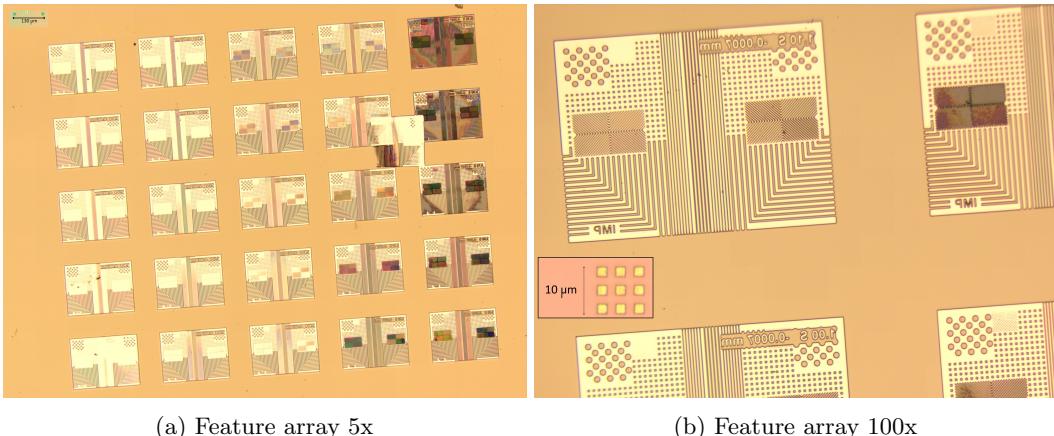


Figure 2.7: Developing an exposure array on SiO<sub>2</sub>

## Developers

Developers are used to dissolve exposed / unexposed areas of photoresist films. We use AZ-726 in conjunction with AZ-1512HS. Using a development time complementary to the exposure time is important to not overdevelop features, as material in proximity to exposed areas is at risk of some structural damage, and developers continue to react with the remaining structure over time.

## Contact pad dimensions

To make contacts large enough to connect probestation probes to (see section 2.2.2), Au pads were created usually with a minimum dimension of  $400\mu\text{m}$  width, and a larger length dimension. This meant that wirebonding was not necessary for small contacts, which saved one step of the measurement process, although PCB boards had been designed with wirebonding in mind (see section 2.1.9).

### 2.1.5 UV Ozone surface preparation

Large resistances can occur when trying to make contact with graphene. This can be for a variety of reasons. Resist residues between the deposited pads and graphene can be insulating, perhaps non-metallic bonding occurs between deposited metals and graphene, or the oxidisation of metals being deposited (i.e., chromium oxide) could occur.

Several studies by Li *et al.*<sup>[11]</sup> and Nath *et al.*<sup>[12;13]</sup> have shown the ability to reduce contact resistance of graphene by using UV ozone treatment, to less than  $200\ \Omega$ , a small contact resistance.

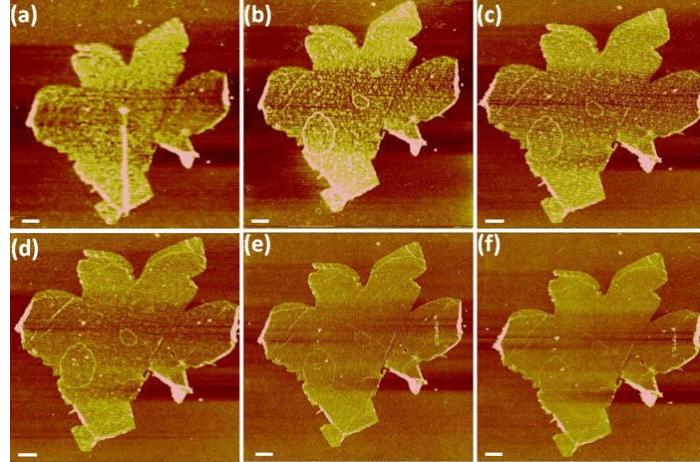


Figure 2.8: Cleaning of graphene using UV Ozone (Source: Li *et al.*<sup>[11]</sup>)

(a) Before transfer (b) After photolithography (c)→(f) UVO treatment for 5, 10, 16, 22min, respectively. Scale bar:  $1\mu\text{m}$ .

UV Ozone treatment refers to the use of UV light to generate photochemical reactions on sample surfaces. 185nm light is used to generate ozone  $\text{O}_3$  from bonding molecular ( $\text{O}_2$ ) oxygen, while 254nm light is used to dissociate ozone to molecular and singlet oxygen ( $\text{O}_1$ ), the latter of which is reactive with substrate surfaces. Increasing stage temperature also will increase the etching rate that occurs. UV Ozone is used in this context to clean the graphene exposed in our developed wells, as seen in fig. 2.8.

To determine an appropriate etching time for the particular tool used, two wafers with graphene flakes at times of 5m and 15m were cleaned using UV Ozone. The 15m devices were etched away completely, however the 5m device provided the first low resistance contact observed, after many iterations of devices.

### 2.1.6 Deposition

Once a designed structure is built to make contacts with graphene and cleaned using UV Ozone, material can now be deposited onto the device. There are many different methods, including sputtering and thermal evaporation, however electron beam evaporation (fig. 2.9) was used for these devices, due to its uniformity, control of deposition rate, and the availability of various material crucibles.

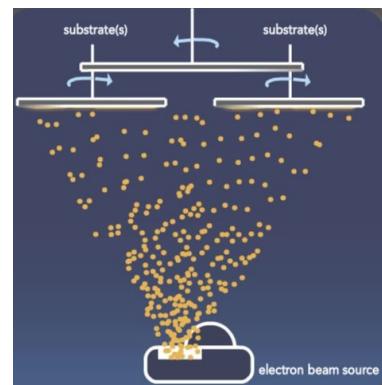


Figure 2.9: E-beam Evaporation  
(Source:<sup>[14]</sup>)

50nm of Au (Gold) was originally deposited with a Cr (Chromium) adhesion layer of 5nm to promote contact to  $\text{SiO}_2$ , however issues with metallic contact to graphene arose. In case of chromium oxidisation during deposition, creating an insulating layer to graphene, a thinner layer (2nm) of chromium was instead deposited. This is reasonable as pinhole effects resulting from a thin deposited Cr layer do not affect bulk transport.

### Oxide Protection

In using metal liquids to cover devices with oxides, the gold reacted strongly to the liquid metallic environment, destroying pre-established pads. This is further described in chapter 5, however the result was to use additional layers, another layer of Cr 2nm and a layer of  $\text{SiO}_2$  20nm. These additional layers do not prevent contact through contact probes and provide insulation from the bulk of metal liquid reactions.

#### 2.1.7 Lift-off

To remove the remaining gold covered photoresist on the substrate, a solvent called PG remover is used to emerse samples at 80 °C. Using a pipette to generate soft fluid flow around the device, the excess gold is slowly removed.



Figure 2.10: PG Remover liftoff

### Ultrasonication

After lift off, the presence of skin remenants (described in section 2.1.4) could sometimes be cleaned off through the use of ultrasonication (fig. 2.11), however this had a large risk of damaging the graphene, seen in fig. 2.12.



Figure 2.11: Ultrasonication used to remove material remnants from lithography.  
Note the movement or loss of gold material on the middle probes.

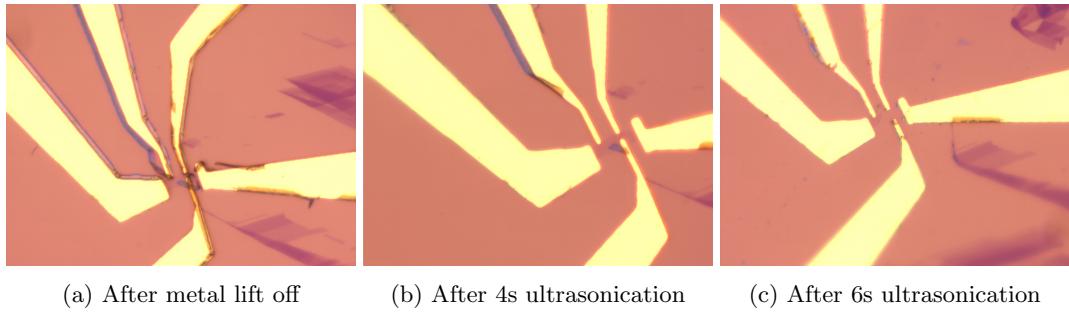


Figure 2.12: Ultrasonication that has broken graphene sample.

### 2.1.8 Argon/Hydrogen Annealing

Many researchers who have produced electronic devices from graphene use an Argon/Hydrogen annealing process to clean their samples from polymer residues remaining from transfer or lithography processes. [15;16;17;18]

We use a process of heating for 30 minutes to 340 °C, annealing with flow rates of 400 sccm Ar / 200 sccm H for 2 hours, before naturally cooling back to ambient temperature.

### 2.1.9 PCB board mounting



Figure 2.13: Ag/H annealing of exfoliated graphene devices



Figure 2.14: PCB for mounting wafers to connect backgates and wirebond pads of device.

PCB boards were designed for mounting small 1 cm<sup>2</sup> Si—SiO<sub>2</sub> wafers. Wafers are mounted using a conductive silver epoxy (CircuitWorks Conductive Epoxy) from Chemtronics. PCB's were produced through PCBway.com, using a single layer design with immersion gold surface finishing. Unfortunately the FR4-TG (flame retardant glass transition temperature) was selected at 130-140, which means these boards cannot withstand temperatures above 140 °C. PCBway also offer a 180 TG option, which would be used in the future.

These PCB boards provide pads to connect probes to the backgated Si. Additionally, to avoid scratching of lithography pads, extra pads surround the mounting point to wirebond connections to, and then place probes onto.

PCB Designs using Autocad Eagle software can be found at [github.com/mattgebert/eaglecircuits](https://github.com/mattgebert/eaglecircuits).

### 2.1.10 Oxide stamping

Zavabeti *et al*'s<sup>[19]</sup> work on thin oxides synthesised by liquid metal introduces two methods to create such oxides. The first involves the exfoliation of oxide layers from the surface of metal droplets, and the second involves the suspension of oxide layers in water, created by injecting gas through the metal liquid. This section will only describe the former in detail, which is used in this project. Refer to chapter 5 for further optimisation and exploration of the liquid metal technique.

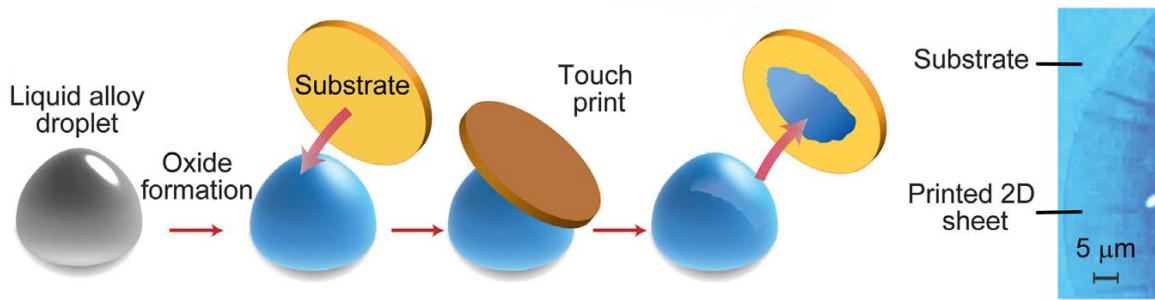


Figure 2.15: Process of liquid metal oxide exfoliation (source: Zavabeti *et al*<sup>[19]</sup>)

A eutectic gallium melt is made by combining elements such as gallium, indium and tin. At room temperature these alloys are metallic liquids, and form atomically thin oxides on their surfaces. Because the formation of oxides change the Gibbs free energy of the system, those that provide the greatest reduction dominate the surface<sup>[19]</sup>. After the melt is formed and exposed to oxygen for some time, the oxide is isolated by a van der Waals exfoliation technique, touching the liquid metal droplet to the solid substrate, as seen in fig. 2.15.

For the primary example of creating  $\text{AlO}_3$ , aluminium pieces are cleaned using a tissue, before being cut up into a few mm long segments. After heating a gallium based melt into a liquid inside a glovebox with roughly 0.2-0.3% oxygen, the gallium and aluminium are ground together using a mortar and pestle.

## 2.2 Measurement techniques

To measure the electrical properties of graphene devices (such as those detailed in section 2.1), particular equipment and methods are employed to observe relevant properties.

### 2.2.1 4 probe measurements

4 probe measurements, also known as Kelvin sensing, utilise four probes to make a more accurate measurement than regular two probe measurements.

Conventional multimeters use a probing voltage with a galvanometer to detect a current running through a sample (in this case, graphene). Based off the detected current, a measurement can be made of the resistance for the known voltage. Because exfoliated graphene can have very small channel widths, it is very sensitiviy to large currents and consequently makes using a multimeter dangerous. Using a multimeter would be fine however, for large area CVD graphene.

One advantage of using a 4 probe measurement is that you can use a current-limiting resistance, which has a much larger resistance than your sample ( $> 100\times$ ). This allows control of the current running through your sample, ensuring safe limits, and means the resistance of your sample will affect the current flow to less than 1%. By observing the voltage difference across the sample, a resistance can be inferred from the flowing current. Typical exfoliated graphene devices used in this project have a measured resistance on the order of  $\approx 5 \text{ K}\Omega$  (eq. (2.1)).

However, the most significant advantage of using a 4 probe measurement is the ability to avoid including contact resistance, created by the junctions between contact pads and the material of interest (graphene). This is illustrated in fig. 2.16. A 4 probe measurement uses a voltage difference measured by probes at different points on the sample material, thereby avoiding any contact resistance included in series, and sampling the voltage along the sample. An example resistance calculation is shown in eq. (2.1).

$$R = \frac{V_{b-a}}{I} = \frac{V_{b-a}}{(V_{\text{source}} - V_{\text{GND}}) / R_{\text{limit}}} = \frac{5 \times 10^{-3} \text{ V}}{1 \text{ V}/10^6 \Omega} = 5 \text{ K}\Omega \quad (2.1)$$

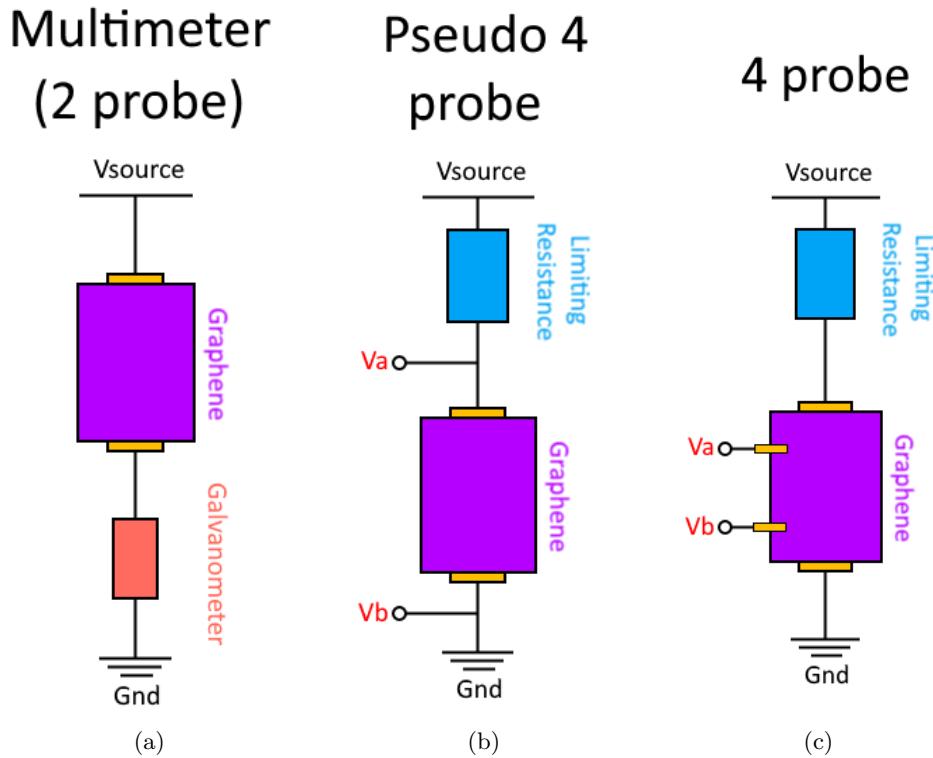


Figure 2.16: Schematics of resistance measurements. (a) A multimeter provides little control over the current through the sample, and measures any resistance formed between the gold contacts and the graphene. (b) A pseudo 4 probe measurement uses a voltage difference across the device to calculate it's resistance, inclusive of the series resistance due to the gold contacts. (c) A 4 probe measurement uses a voltage difference measured by probes at different points on the sample material, thereby avoiding any contact resistance included in series, and sampling the voltage along the sample.

### Sourcemeters

A sourcemeter has the ability to source and measure a stable DC voltage or current. They provide precision, low noise and stability. We use Keithley 2400 SourceMeters<sup>[20]</sup> which source voltage from  $5\mu\text{V}$  to 210V, and current from 50pA to 1.05A, and can deliver 520 readings per second at  $5\frac{1}{2}$  digits (ie, 199999).

A source meter is used in 4 probe measurements to apply a constant, controllable gate voltage to the Si as directed in fig. 2.17. Changing the potential of Si under  $\text{SiO}_2$  changes the charged carrier density (electrons, holes) on graphene by using the  $\text{SiO}_2$  as a capacitor dielectric. This allows the measurement of the resistivity of graphene as a function of carrier density.

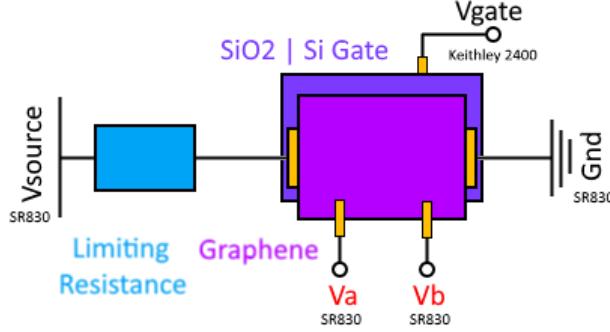


Figure 2.17: Instrumentation connections to a gated graphene FET, using a Keithley 2400 SourceMeter and a SR830 Lock-In Amplifier.

### Lock-in amplifiers

A lock in amplifier is used to measure very small AC signals. This project used a Stanford Research 830 Lock-in amplifier<sup>[21]</sup>, which uses a significant amount of digital signal processing (DSP) for its functionality. It operates on the principles of signal mixing - multiplying a input signal ( $f_s$ ) that is expected at a particular frequency by a reference signal ( $f_r$ ). This mixing generates a DC signal whose amplitude can be measured, directly inferring a signal strength. An example calculation of mixing is shown below in eq. (2.3).

$$f_s \otimes f_r = \cos(\omega_s t + \phi) \otimes \cos(\omega_r t) \quad (2.2)$$

$$\begin{aligned} &= [\cos(\omega_s t) \cos(\phi) - \sin(\omega_s t) \sin(\phi)] \otimes \cos(\omega_r t) \\ &= \cos(\phi) \frac{1}{2} [\cos((\omega_s + \omega_r)t) + \cos((\omega_s - i\omega_r)t)] \\ &\quad - \sin(\phi) \frac{1}{2} [\sin((\omega_s + \omega_r)t) + \sin((\omega_s - \omega_r)t)] \end{aligned} \quad (2.3)$$

When the two frequencies  $\omega_s$  and  $\omega_r$  are close, then the sinusoidal components  $\omega_s - \omega_r$  form a DC component, while high frequency compliment can be filtered. Only noise close to the signal frequency will be picked up in the filtering, and will only result in low frequency AC output.

The lock in amplifier uses a phase locked loop to generate a reference signal, which is a particular control circuit. The lock in amplifier can either run independently, generating its own output, or can be locked to an external signal. We use the former in our measurements, to pass a slow 17Hz signal of amplitude 1V<sub>rms</sub> through graphene devices.

A voltage difference is calculated between probes on graphene by the lock in amplifier and outputted. The real component of the voltage difference and the complex phase are recorded - we expect the bulk transport in graphene to be resistive, and a phase is measured to confirm that as we measure.

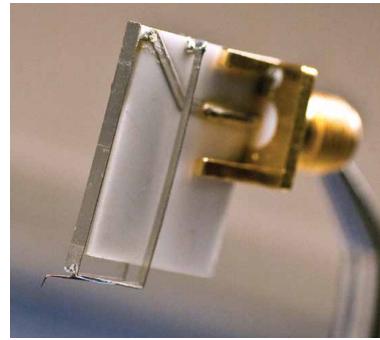
### 2.2.2 Probe station

A LakeShore cryogenic probestation (fig. 2.18) was used to load sample wafers and measure their electronic properties under controlled conditions. In particular, we will touch on temperature control,

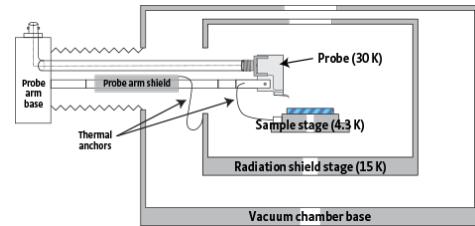
vacuum ability, and the risk of static discharge.



(a) LakeShore probestation, with coolant inlet, 6 probe arms, vacuum seal and microscope camera.



(b) Tungsten spring probes, 25  $\mu\text{m}$  radius tip



(c) Schematic diagram of probestation, showing connections from probe arms to sample stage and temperature limits of elements

Figure 2.18: LakeShore probestation

## Vacuum

A roughing pump is used in conjunction with a turbo pump to create pressures of  $1.5 \times 10^{-2}$  mBar and  $5 \times 10^{-5}$  mBar (turbo at 1.35 kHz operational frequency). This pumping removes any trapped oxygen and contamination of gasses that might condense onto our sample of graphene at low temperature.

## Temperature control

Temperature is controlled by a combination of heating and cooling power. The metallic inlet protruding from under the main stage in fig. 2.18 allows the flow of liquid nitrogen/helium through the sample stage to cool down the sample. This process is illustrated in fig. 2.19.

Heating is provided via a 50W calibrated silicon diode. Thermocouples with high accuracy allow the ability to control the heating power to stabilise to a setpoint temperature, with small fluctuation. This is achieved by the use of a PID controller system, where the measured temperature difference from a setpoint is used to control the diode power. By using the proportional, integral and differential gains, rapid and stable responses to shifts in desired temperature are

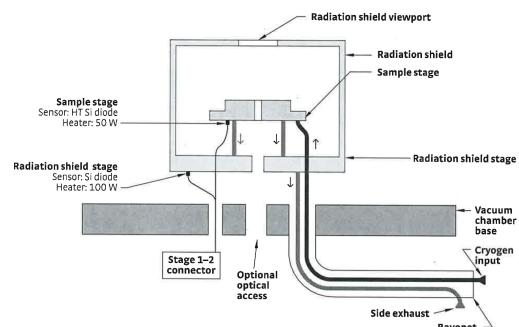


Figure 2.19: Probestation refrigerator

be controlled.

- Proportional gain adds some power based on the difference from the desired solution.
- Integral gain ramps the power over time, based off long term difference. This prevents offsets from a final setpoint.
- Differential gain only considers the changing response. It smoothens trajectory of PI controller, reducing overshoot and stabilising levels faster.

### Static Discharge

Care needs to be taken when using the probestation with small graphene samples. Static discharge can cause large potential differences across graphene, consequently burning the sample by a high current. Discharge can be protected against by taking some precautions below.

BNC cables employ a coaxial (ground and signal) wire configuration, and are used to connect to the probestation. This ensures the probestation shield is grounded, the same as the instrument ground. This protects the device from any external static buildup. If the probes are then grounded, they are at the same potential as the shield.

Additionally, when a measurement was not taking place, BNC connections to the device were grounded using  $50\Omega$  terminators, connected via T terminals to avoid floating connections and minimising static while connecting terminators. This meant that any external charge would have a low resistance current path to flow, thereby protecting the sample.

Static straps were also worn and connected to the instrument ground to ensure no clothing item would build up static on an individual.

### Probes

A combination of regular and flexible tungsten probes are used in the probestation to make electrical connections to samples. When touching probes down, the respective BNC was connected to a  $10 M\Omega$  resistance terminator. Rather than protecting from external static, this was in case the sample (sometimes doped) was resting at a potential other than ground, and had free charge to discharge. A high resistance terminator slows this current, before allowing the connection of an appropriate ground.

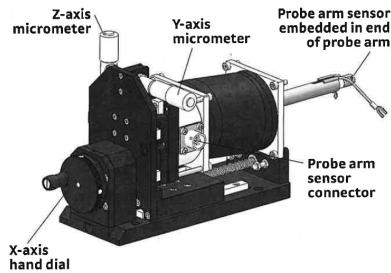


Figure 2.20: Probestation micro-manipulated stages

## Chapter 3

# Characterisation of graphene

## Chapter 4

# Electrical measurements of pristine graphene

### 4.1 CVD

### 4.2 Exfoliated

$$C_{\text{flake}} = \frac{G_{\text{SiO}_2} - G_{\text{flake}}}{G_{\text{SiO}_2}} \quad (4.1)$$

$$\partial R = \frac{\rho}{w} \partial L \quad (4.2)$$

$$R = \frac{V}{I} = \frac{V_a - V_b}{I_{in}} \quad (4.3)$$

$$\sigma = \sqrt{(N^* e \mu)^2 + \left( \rho_S + \frac{1}{N e \mu} \right)^{-2}} \quad (4.4)$$

$$N = \frac{C_g}{e} |V - V_G| \quad (4.5)$$

$$\rho[V_g, T] = \rho_0[V_g] + \rho_A[T] + \rho_B[Vg, T] \quad (4.6)$$

$$\rho_A[T] = \left( \frac{h}{e^2} \right) \frac{\pi 2 D a^2 k_B T}{2 h^2 \rho_S V_s^2 V_F^2} \quad (4.7)$$

$$\rho_B[V_G, T] = B \frac{h}{e^2} V_G^{-\alpha_1} \left( \frac{1}{\exp[(0.059 \text{ eV})/k_B T] - 1} + \frac{6.5}{\exp[(0.115 \text{ eV})/k_B T] - 1} \right) \quad (4.8)$$

#### 4.2.1 hBN transfer

# Chapter 5

## Thin oxides

### 5.1 Printing

5.1.1  $\text{Al}_2\text{O}_3$

5.1.2  $\text{SnO}$

5.1.3  $\text{Bi}_2\text{O}_3$

### 5.2 Smearing

5.2.1  $\text{Ga}_2\text{O}_3$

# **Chapter 6**

## **Conclusion**

**6.1 Future direction**

**6.2 Concluding remarks**

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# Appendices

## **Appendix A**

### **Raman spectroscopy samples**

## **Appendix B**

### **Labview programs**