

MONASH UNIVERSITY

HONOURS THESIS

Thin oxides in graphene devices

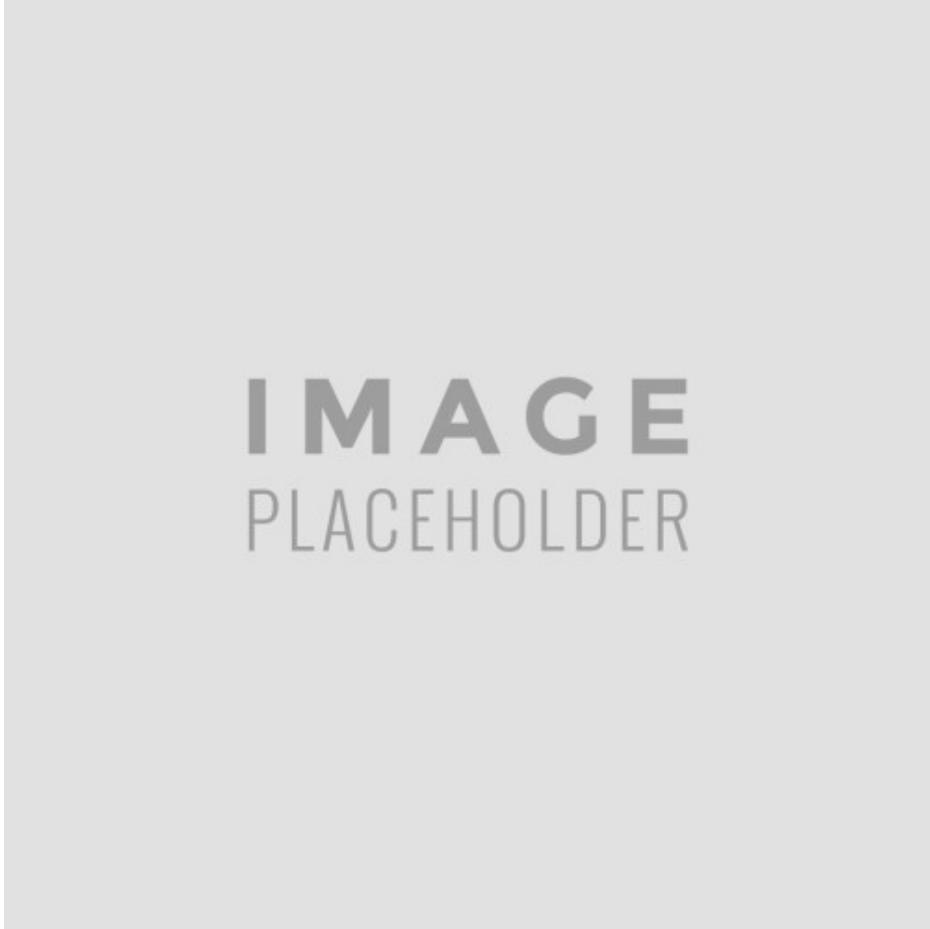


IMAGE
PLACEHOLDER

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Abstract

I present a review of the use of graphene in electronic devices, both in its shortfalls and exciting properties. The electronic structure is detailed, along with various scattering sources that affect electron transport and ultimately the goal of room temperature, electronic devices. Considering heterostructures and the use of other materials to enhance graphene, I discuss the potential use of hafnium dioxide, and other oxides, as an excellent gate dielectric material for potential use in graphene field-effect devices.

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Foreword

This thesis serves the purpose presenting the conclusions of my research into thin oxides on graphene. I will be arguing , and how that fits into a bigger picture of materials science and particular applications.

In chapter 1, I will outline what I hope to achieve in this project. I begin by discussing the theoretical properties of graphene and why it has attracted so much interest as an electronic material. I will also describe some challenges facing new computing technologies, including the use of dielectrics, and how my work contributes to realising solutions to new generations of this technology. I will outline a theoretical and experimental summary of the results to date seen in introducing dielectrics to graphene.

In chapter 2, I describe the various ways of producing and identifying graphene in lab use, and the characterisations I have conducted. This will include our use of atomic force microscopy (AFM), optical microscopy and Raman spectroscopy.

I will then describe the devices and measurements I have made in chapter 3. This will regard connections to devices, which allow the measurements I have perform, and the processes used to fabricate our devices. I have made graphene devices using lithography and evaporation methods, to create electrical contacts. I will also describe the oxides I have investigated in this chapter, and the methods I have used to transfer them.

In chapter 4 I will present the data and results from my measurements of the respective devices which will be placed on SiO_2 . The results to here will be compared alongside data after stamping the same devices with thin oxides in chapter 5.

Chapter 1

Introduction

1.1 Preface

The mechanical exfoliation of atomically thin materials in 2004 sparked a flurry of research into many materials with unique properties. Graphene, the first of these, rose to prominence in research and has begun finding applications in industrial contexts.

Materials that are two dimensional restrict the movement of electrons to a plane. Because of this, these materials exhibit unique electronic properties. A clear example of this is a hexagonal lattice of carbon atoms, or graphene, which gives rise to a 'dirac' point in the band structure (see section 1.3.1).

1.2 Transistors - the field effect

1.2.1 Conductivity in FETs

1.2.2 Mobility in FETs

1.3 Graphene

1.3.1 Electronic properties

Why is it a good conductor?

Hybridisation

Electronic dispersion

Charged puddling

1.4 Transport and scattering in graphene

1.4.1 Charged impurities

1.4.2 Phonon scattering

1.4.3 Dielectric screening

Charge screening

Fine structure constant

Tuning the fine structure constant

High κ materials

1.4.4 Remote phonon scattering

1.5

Chapter 2

Experimental techniques

2.1 Fabrication

To create devices where we can measure the electronic properties referenced in sections 1.2 and 1.3.1, metallic contacts need to be added to the graphene to measure electronic flow through the device.

To do this, lithography can be used to create polymer structures that allow the deposition of desired material in 2D geometries. This process and the adjustments made for fabricating our devices are described in the sections below.

2.1.1 Lithography

Lithography typically consists of three steps.

1. Spin coating - covering your sample with a uniform layer of polymer.
2. Exposure - exposing the polymer to light changes the chemical compounds and properties. This differentiates exposed areas to those unexposed.
3. Developer solution - developer solution removes intended areas of photoresist to create structures.

Spin coating photoresists

A spin coater is used to deposit thin films of materials. A vacuum is used to hold a sample horizontally on the spinner, before drops of photoresist are dropped onto the sample. The sample is then spun over sometime to achieve a uniform thickness of the photoresist, before baking on a hotplate occurs to set the sample.

Photoresists vary in their spinning thickness, but also their exposure rates. Positive photoresists dissolve in developer when exposed to light, while negative photoresists dissolve if not exposed to light. We have only used positive photoresists, as we have primarily been creating structures for deposition, and not etching material (protect your sample, but remove everything else).

HMDS & AZ-1512HS Initially devices were fabricated using the AZ-1512HS polymer, with the additional use of hexamethyldisilazane (HMDS) as an adhesion promoter between SiO_2 and AZ-1512HS. Devices were spun initially for 10 s at 1000 rpm, before being spun between 2000 and 3000 rpm for 30 s, per resist layer. This leaves a thickness of $1.7 \mu\text{m}$ to $1.39 \mu\text{m}$ ^[6]. Devices were then baked at 100°C for 1 minute.

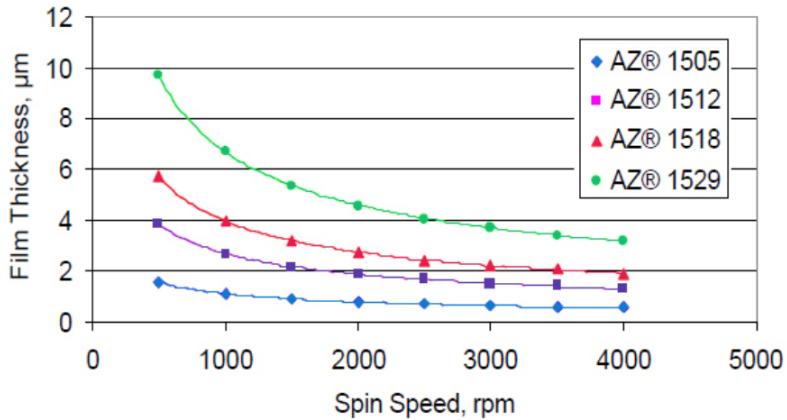


Figure 2.1: Spin curve of AZ-1512HS (Source: EMD Performance Materials^[7])

Skin issues with HMDS When using HMDS and AZ-1512HS in conjunction, significant amounts of deposition remenants were found on samples as seen in .

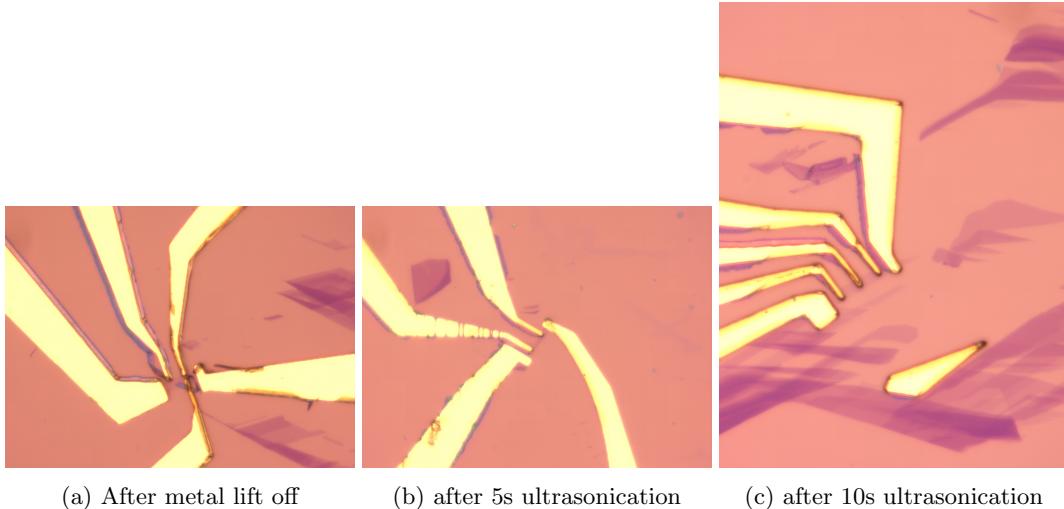


Figure 2.2: Material remanants from lithography

This is likely a result of initial layers of metal deposition (ie, Chromium, see section 2.1.3) forming layers on the sides of the developed lithography wells, as the skins have very similar geometry to that of either the wells or the edges. Futher evidence that supports this is that the spinning speeds give resist heights (ie, the well edge heights) roughly the same as feature width ($\approx 1\mu\text{m}$ minimum).

Sometimes these remenants could be cleaned off, through the use of ultrasonication, however this had a large risk of damaging the graphene, seen in fig. 2.2.

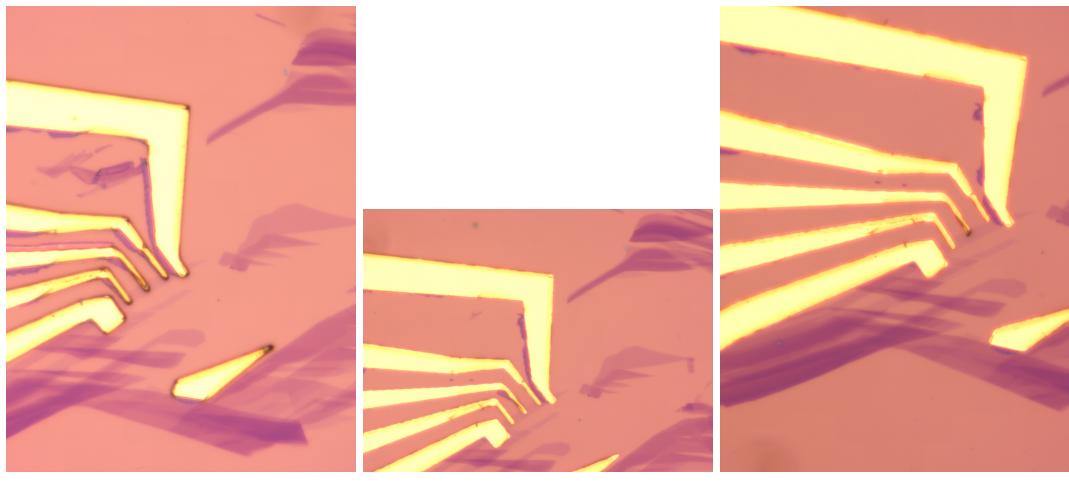


Figure 2.3: Material remnants from lithography

LOR-1A & AZ-1512HS An issue with a single layer photoresist processes is that well edges allow deposited materials to adhere, leaving 'skins'. One way to prevent this from happening is to use a multilayer process. Two resist layers are spun onto the sample, with the bottom film being more sensitive to the lithography process than the top (ie, develops faster, or is more sensitive to exposure). When developed, the bottom layer *undercuts* the top layer, stopping adhesion to the edges of the well when material is deposited. This process is depicted in fig. 2.4.

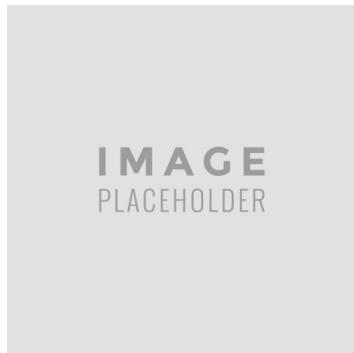


Figure 2.4: Bilayer lithography process

Rather than a photoresist, LOR-1A is a lift off resist. When the films are exposed to the developer, LOR-1A is also lifted off with the soluble AZ-1512HS. Additional material is pulled and dissolved from the well, leaving the desired undercut effect.

Exposure

After spinning, a mask writer tool is used to expose the wafer and resist films to UV light to develop desired pads. A mask writer usually is composed of a DMA (Digital Mirror Array) which allows filtering to pixel like squares.

An important parameter played with in this process is the exposure time, which affects your ability to develop fine structures. By using an array of different exposure times (fig. 2.5), we were

able to optimise our feature exposure for a typical developing time.

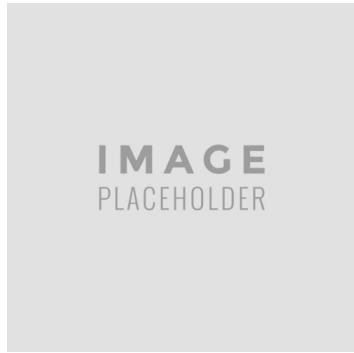


Figure 2.5: Developing an exposure array on SiO₂

Prepared CAD files, that specify the structure for desired contact pads onto devices, are used by the DMA to iteratively expose small areas of the film. These exposed areas undergo a chemical change, changing the structural properties for development.

Developers

Developers are used to dissolve exposed / unexposed areas of photoresist films. For example, we use AZ-726 in conjunction with AZ-1512HS. Using a development time complementary to your exposure time is important to not overdevelop your features, as material in proximity to exposed areas is at risk of some structural damage. Developers do still affect the remaining structure over time.

2.1.2 UV Ozone surface preparation

Large resistances can occur when trying to make contact with graphene. This can be for a variety of reasons. Resist residues between the deposited pads and graphene can be insulating, non-metallic bonding between deposited metals and graphene, or oxidisation of metals being deposited (ie, chromium oxide).

We use UV Ozone to clean the graphene exposed in our developed wells. UV Ozone cleaning blasts the surface with UV ozone light, while flowing oxygen gas. Overtime surfaces are slowly etched and material that is not strongly bonded is cleared.

In our optimisation we ran two wafers with devices at times of 5m and 15m respectively (see fig. 2.6). The 15m devices were etched away completely, however the 5m device provided the first low resistance contact observed, after many iterations of devices.

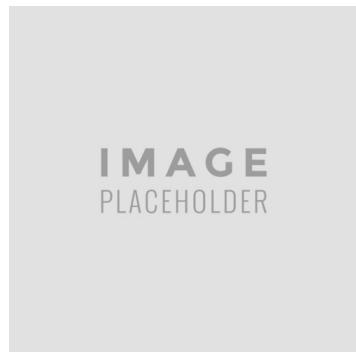


Figure 2.6: Cleaning before and after UV Ozone

2.1.3 Deposition

Once a designed structure is exposed to make contacts with graphene,

Oxide Protection

2.1.4 Lift-off

Ultrasonication

2.1.5 Oxide transfer

2.2 Measurement techniques

2.2.1 4 probe measurement

Limiting resistance

2.2.2 Probe station

Cooling

PID control

Vacuum

Cabling & Static Discharge

Chapter 3

Characterisation of graphene

3.1 Production

Since graphene's realisation in 2004^[1], much research has been focused to finding efficient ways of producing large amounts of graphene^[2]. Originally, the first samples ever created which have primarily been used for sensitive measurements have been conducted using a method of exfoliation (section 3.1.1). These samples typically exhibit better electronic properties than those produced by other methods. Since 2008/2009, CVD (section 3.1.2) of carbon to create graphene films has provided another prominent method to produce large films for industrial scale applications. In particular, growth of graphene on copper sheets^[3] has been a reliable way producing these large uniform sheets.

There are other methods not used in this thesis, such as epitaxial growth of graphene via SiC uses heating to boil off silicon atoms to form a layer of graphene on its surface.

3.1.1 Exfoliation

Originally made famous in the breakthrough method by Giem and Novoselov^[1;4], a mechanical exfoliation technique allowed for the isolation of atomically thin crystals of various materials. They reported the use of scotch tape to cleave thin layers from a larger crystal.

The common procedure involves pressing tape/surfaces against a bulk crystal (such as highly orientated pyrolytic graphite (HOPG), Kish graphite, natural graphite, or graphenium). Due to van der Waals interactions, layers of graphite are transferred to the desired surface. By repeated peeling of the same tape, a thin coverage can be obtained and then transferred onto substrates, such as SiO₂.

Thermal enhancement

Drawing on the methods described in Huang *et al*^[5], we developed a reliable method of exfoliation. Using

When bringing the tape with graphite flakes into contact with the SiO₂wafer, we use Huang *et al*'s method they use an annealing process of heating the tape and wafer for 2-5m at $\sim 100^{\circ}\text{C}$ on a conventional lab hot plate. After allowing cooling to room temperature, the tape is removed. They find under optical microscopy that graphene flakes with uniform thickness routinely range from $\sim 20\mu\text{m}$ to above $100\mu\text{m}$. The two additional steps to regular exfoliation methods were oxygen plasma cleaning and temperature annealing. Annealing is expected to increase traction due to the removal of gas molecules trapped between SiO₂ and graphite. Oxygen plasma is expected to remove absorbates on the substrate surface.

Huang *et al* suggest part of their success comes from applying larger uniform coverage on tape. They suggest that because the exfoliation comes from the competition of forces between the substrate

and the other graphene layers in multilayer graphite, using thinly covered tape is detrimental to the transfer.

Extra details Huang *et al* also specified further details about the parameter spaces they search for optimising their exfoliation.

- Only apply tape exfoliation maximum 3 to 4 times after removal from bulk graphite.
- Annealing time nor temperature not strongly affected coverage, but optimal at $\sim 100^{\circ}\text{C}$ & 2 mins. Longer time also implied more glue residue from the tape.

Rough surface adhesion

3.1.2 CVD

Dry transfer

3.2 Identification of Graphene

3.2.1 Optical Microscopy

3.2.2 Raman Spectroscopy

3.2.3 Atomic Force Microscopy Imaging

Chapter 4

Electrical measurements of pristine graphene

4.1 CVD

4.2 Exfoliated

$$C_{\text{flake}} = \frac{G_{\text{SiO}_2} - G_{\text{flake}}}{G_{\text{SiO}_2}} \quad (4.1)$$

$$\partial R = \frac{\rho}{w} \partial L \quad (4.2)$$

$$R = \frac{V}{I} = \frac{V_a - V_b}{I_{in}} \quad (4.3)$$

$$\sigma = \sqrt{(N^* e \mu)^2 + \left(\rho_S + \frac{1}{N e \mu} \right)^{-2}} \quad (4.4)$$

$$N = \frac{C_g}{e} |V - V_G| \quad (4.5)$$

$$\rho[V_g, T] = \rho_0[V_g] + \rho_A[T] + \rho_B[Vg, T] \quad (4.6)$$

$$\rho_A[T] = \left(\frac{h}{e^2} \right) \frac{\pi 2 D a^2 k_B T}{2 h^2 \rho_S V_s^2 V_F^2} \quad (4.7)$$

$$\rho_B[V_G, T] = B \frac{h}{e^2} V_G^{-\alpha_1} \left(\frac{1}{\exp[(0.059 \text{ eV})/k_B T] - 1} + \frac{6.5}{\exp[(0.115 \text{ eV})/k_B T] - 1} \right) \quad (4.8)$$

4.2.1 hBN transfer

Chapter 5

Thin oxides

5.1 Printing

5.1.1 Al_2O_3

5.1.2 SnO

5.1.3 Bi_2O_3

5.2 Smearing

5.2.1 Ga_2O_3

Chapter 6

Conclusion

6.1 Future direction

6.2 Concluding remarks

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Appendices

Appendix A

Raman spectroscopy samples

Appendix B

Labview programs