

MONASH UNIVERSITY

HONOURS THESIS

Thin oxides in graphene devices

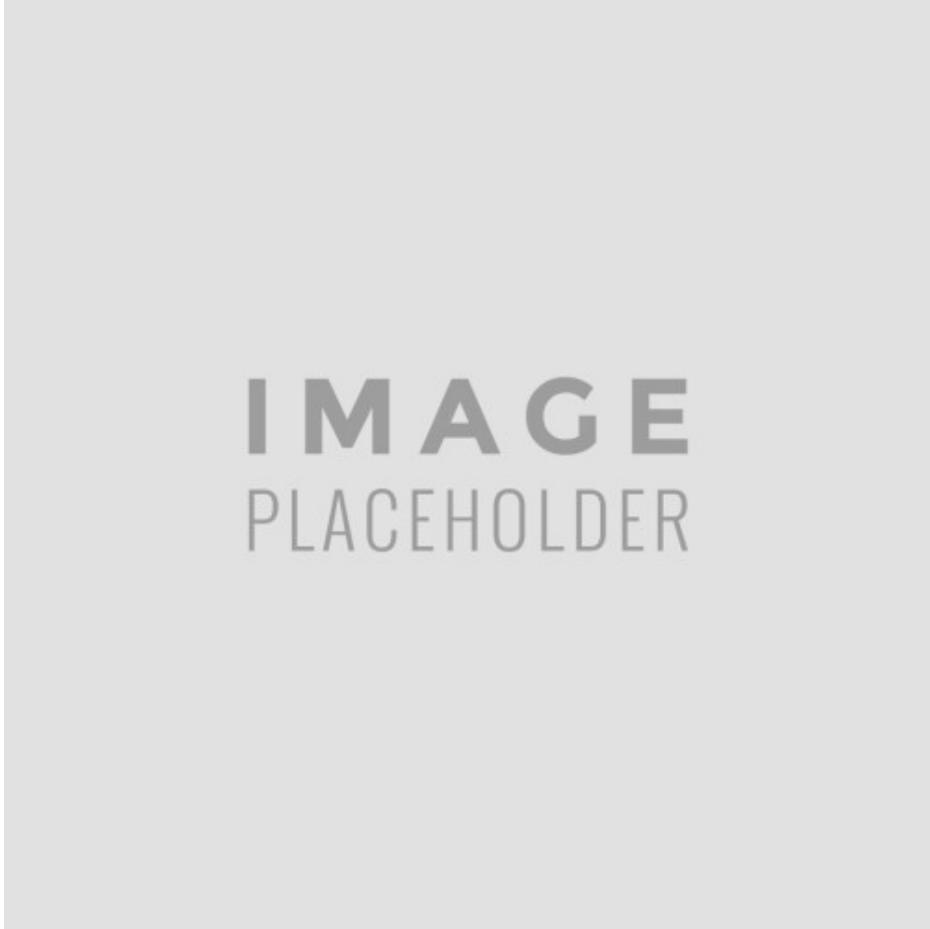


IMAGE
PLACEHOLDER

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Abstract

I present a review of the use of graphene in electronic devices, both in its shortfalls and exciting properties. The electronic structure is detailed, along with various scattering sources that affect electron transport and ultimately the goal of room temperature, electronic devices. Considering heterostructures and the use of other materials to enhance graphene, I discuss the potential use of hafnium dioxide, and other oxides, as an excellent gate dielectric material for potential use in graphene field-effect devices.

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Foreword

This thesis serves the purpose presenting the conclusions of my research into thin oxides on graphene. I will be arguing , and how that fits into a bigger picture of materials science and particular applications.

In chapter 1, I will outline what I hope to achieve in this project. I begin by discussing the theoretical properties of graphene and why it has attracted so much interest as an electronic material. I will also describe some challenges facing new computing technologies, including the use of dielectrics, and how my work contributes to realising solutions to new generations of this technology. I will outline a theoretical and experimental summary of the results to date seen in introducing dielectrics to graphene.

In chapter 2, I describe the various ways of producing and identifying graphene in lab use, and the characterisations I have conducted. This will include our use of atomic force microscopy (AFM), optical microscopy and Raman spectroscopy.

I will then describe the devices and measurements I have made in chapter 3. This will regard connections to devices, which allow the measurements I have perform, and the processes used to fabricate our devices. I have made graphene devices using lithography and evaporation methods, to create electrical contacts. I will also describe the oxides I have investigated in this chapter, and the methods I have used to transfer them.

In chapter 4 I will present the data and results from my measurements of the respective devices which will be placed on SiO_2 . The results to here will be compared alongside data after stamping the same devices with thin oxides in chapter 5.

Chapter 1

Introduction

1.1 Preface

The mechanical exfoliation of atomically thin materials in 2004 sparked a flurry of research into many materials with unique properties. Graphene, the first of these, rose to prominence in research and has begun finding applications in industrial contexts.

Materials that are two dimensional restrict the movement of electrons to a plane. Because of this, these materials exhibit unique electronic properties. A clear example of this is a hexagonal lattice of carbon atoms, or graphene, which gives rise to a 'dirac' point in the band structure (see section 1.3.1).

1.2 Transistors - the field effect

1.2.1 Conductivity in FETs

1.2.2 Mobility in FETs

1.3 Graphene

1.3.1 Electronic properties

Why is it a good conductor?

Hybridisation

Electronic dispersion

Charged puddling

1.4 Transport and scattering in graphene

1.4.1 Charged impurities

1.4.2 Phonon scattering

1.4.3 Dielectric screening

Charge screening

Fine structure constant

Tuning the fine structure constant

High κ materials

1.4.4 Remote phonon scattering

1.5

Chapter 2

Experimental techniques

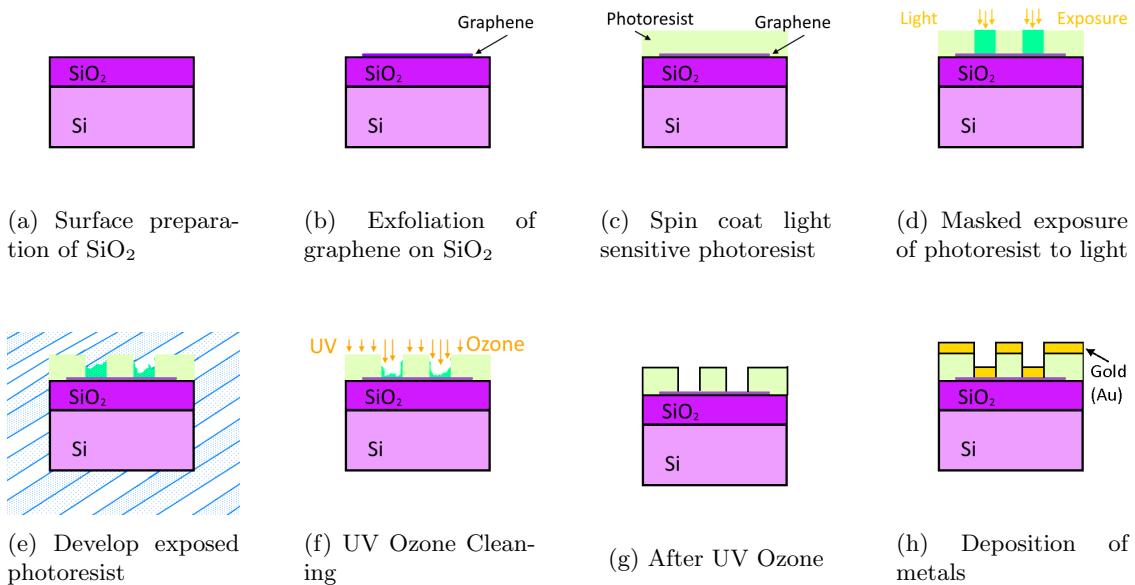
Two aspects are involved in performing electronic measurements of materials, namely fabrication and measurement techniques.

Physical devices containing graphene need to be fabricated allow measurements to take place. This primarily deals with the production of materials (graphene, oxides) and the processes to develop connectable devices. Some of the tools and techniques used include lithography, electron beam evaporation, and etching. The processes used in this project are detailed in section 2.1.

To measure the properties of graphene, particular experimental methods and procedures are required to control the environment and obtain useful data. Section 2.2 primarily deals with the operation of the experimental apparatus used to measure the electronic properties of graphene.

2.1 Fabrication

To create graphene devices where we can measure the electronic properties referenced in sections 1.2 and 1.3.1, a variety of steps need to be taken in order to probe electronic flow.



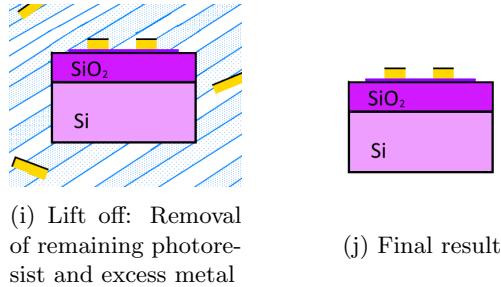


Figure 2.1: Device fabrication process
From exfoliated graphene to a FET.

2.1.1 Graphene

Since graphene's realisation in 2004^[1], much research has been focused to finding efficient ways of producing large amounts of graphene^[2]. Originally, the first samples ever created which have primarily been used for sensitive measurements have been conducted using a method of exfoliation (section 2.1.2). These samples typically exhibit better electronic properties than those produced by other methods. Since 2008/2009, CVD (?) of carbon to create graphene films has provided another prominent method to produce large films for industrial scale applications. In particular, growth of graphene on copper sheets^[3] has been a reliable way producing these large uniform sheets.

There are other methods not used in this thesis, such as epitaxial growth of graphene via SiC uses heating to boil off silicon atoms to form a layer of graphene on it's surface.

2.1.2 Exfoliation

Exfoliation in materials refers to the cleaving thin layers (or leaves) off a larger sample, and acquiring them onto the substrate. We exfoliate graphene onto Si/SiO₂ wafers. Generally exfoliation involves pressing tape/surfaces against a bulk crystal (such as highly orientated pyrolytic graphite (HOPG), Kish graphite, natural graphite, or graphenium). Due to van der Waals interactions, layers of graphite are transferred to the desired surface. By repeated peeling of the same tape, a thin coverage can be obtained and then transferred onto substrates, such as SiO₂. Exfoliation can take a variety of forms, from Geim's method^[4], to directly applying scotch tape to HOPG and then pressing against SiO₂, before peeling the tape off.

Huang *et al* investigated a reliable method of exfoliation to produce large area and high quality samples^[5], which has been widely cited. Tape with graphite flakes is brought into contact with a silicon dioxide wafer, and an annealing process of heating the tape and wafer for 2-5m at ~ 100°C on a conventional lab hot plate is used. After allowing cooling to room temperature, the tape is removed. They find under optical microscopy that graphene flakes with uniform thickness routinely range from ~ 20μm to above 100μm. In this context, annealing is expected to increase traction due to the removal of gas molecules trapped between SiO₂ and graphite.

The following steps make up the process of exfoliation we optimised:

1. (Optional) Use a plasma ashing/etcher with an argon/oxygen plasma to the clean surface of SiO₂. This can increase the adhesion between graphene and the surface by removing organic adsorbates^[5]. Alternatively, clean wafers of Si/SiO₂ in acetone, tilted in an ultrasonic bath for 30s. Repeat the same in isopropanol, before rinsing in ethanol and drying with N₂ gas.
2. Cleave a layer of HOPG graphite by using scotch tape to peel off a thick film.
3. Use a secondary piece of scotch tape to exfoliate a thinner layer off master tape. Ensure good coverage by reattaching a couple times.

4. Attach Si/SiO₂ wafers to graphite covered areas of secondary tape. The SiO₂ face should be contacting the graphite.
5. Attach the tape and wafers firmly to a glass slide, before using a tissue/cotton-bud to press the surface of the tape into the wafer.
6. Place glass slide on a hotplate at 100°C for two minutes, before removing and cooling for two minutes.
7. Slowly peel tape at an acute angle from the glass slide, roughly at 6s per cm over the wafer.

We found success can depend on HOPG crystal, given we tried cleavage using ZYA and ZYB quality crystals and had repeated failure. Changing to a new ZYA crystal provided immediate results using the same process.

2.1.3 Lithography

Lithography can be used to create polymer structures that allow the deposition of desired material in 2D geometries. This is used to create electrical contacts onto graphene. This process and the adjustments made for fabricating our devices are described in this section.

Lithography typically consists of three main steps.

1. Spin coating - covering a sample with a uniform layer of polymer, and baking it on.
2. Exposure - The polymer undergoes chemical changes to its properties when exposed to particular wavelengths of light. This differentiates exposed areas to those unexposed.
3. Developer solution - developer solution removes intended areas of photoresist to create structures.

Spin coating photoresists

A spin coater is used to deposit thin films of materials. A vacuum holds a sample on the spinner, before drops of photoresist are introduced to the sample, which is then spun over sometime to achieve a uniform thickness of photoresist. Baking on a hotplate follows to set the photoresist layer on the sample.

Photoresists vary in their spinning thickness, but also their exposure rates. Positive photoresists dissolve in particular developer solutions when exposed to light, while negative photoresists dissolve if not exposed to light. We have only used positive photoresists, as we have primarily been creating structures for deposition, and not etching material where you want the bulk of the wafer exposed.

HMDS & AZ-1512HS Initially devices were fabricated using the AZ-1512HS polymer, with the additional use of hexamethyldisilazane (HMDS) as an adhesion promoter between SiO₂ and AZ-1512HS. Devices were spun initially for 10 s at 1000 rpm, before being spun between 2000 and 3000 rpm for 30 s, per resist layer. This leaves a thickness of 1.7 μm to 1.39 μm^[6]. Devices were then baked at 100 °C for 1 minute.

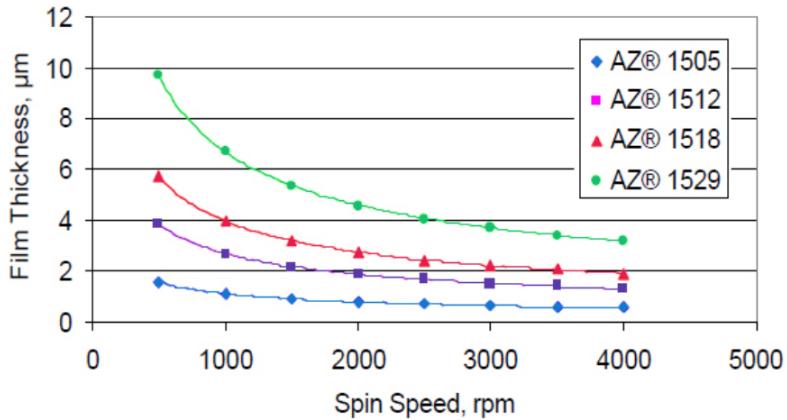


Figure 2.2: Spin curve of AZ-1512HS (Source: EMD Performance Materials^[7])

Skin issues with HMDS When using HMDS and AZ-1512HS in conjunction, significant amounts of deposition remenants were found on samples as seen in fig. 2.3.

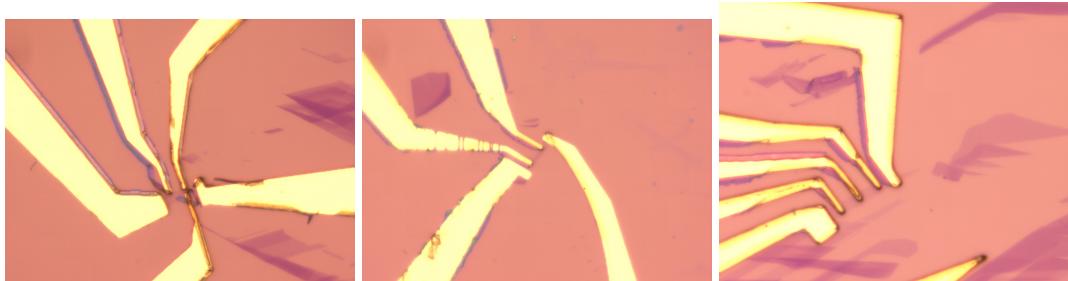


Figure 2.3: Material remanants from lithography. Gold edges exhibit a bluish remnant edge.

This is likely due to metal deposition (ie, Chromium, see section 2.1.5) forming layers on the sides of lithography wells, as the skins have very similar geometry to that of either the wells or the edges. The spinning speeds give resist heights (ie, the well edge heights) roughly the same as feature width ($\approx 1\mu\text{m}$ minimum), matching the observed result.

Ultrasonication (see section 2.1.6) can be used to attempt to remove edges after lift off, however there is risk of damaging samples of graphene.

LOR-1A & AZ-1512HS The issue with a single layer photoresist processes, outlined above, is that well edges allow deposited materials to adhere, leaving 'skins'. One way to prevent this from happening is to use a multilayer process. Two resist layers are spun onto the sample, with the bottom film being more sensitive to the lithography process than the top (ie, develops faster, or is more sensitive to exposure). When developed, the bottom layer *undercuts* the top layer, stopping adhesion to edges of the well when material is deposited. This process is depicted in fig. 2.4.

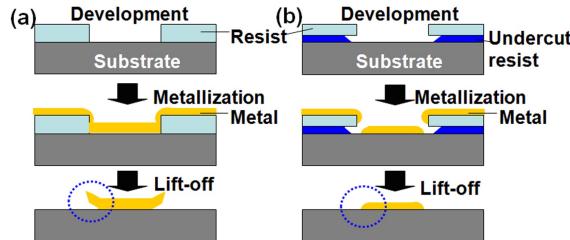


Figure 2.4: Bilayer lithography process (Source: Park *et al*^[8])

LOR-1A is an actinic lift off resist, responding to UV light from 240 nm to 290 nm^[9]. When the resist films are exposed to the developer, LOR-1A is removed below an overhanging AZ1512-HS layer due to additional development, leaving the desired undercut effect.

Exposure

After spinning, a mask writer tool is used to expose the wafer and resist films to UV light. A mask writer is composed of a mask, or a DMD (digital micro-mirror device) which allows filtering of pixel like squares, based on an input image. Actinic reactions occur from the UV light with the photoresist, forming desired pad structures in the resist. Prepared CAD files are used to generate masks used by the DMD as seen in fig. 2.5.

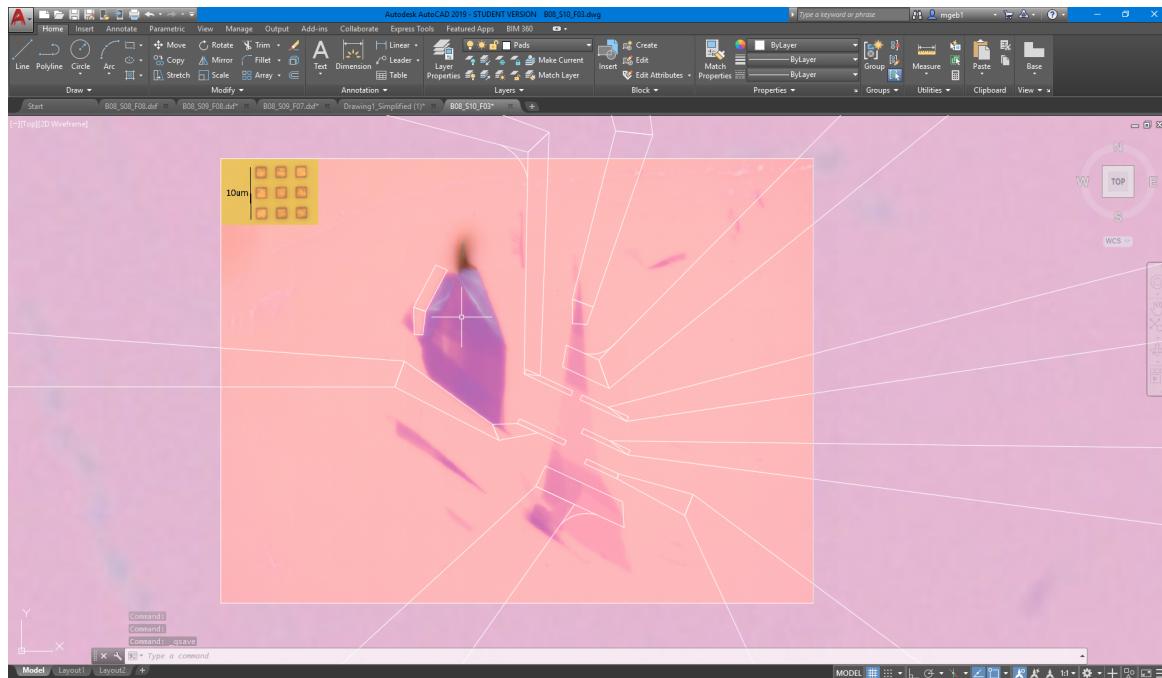


Figure 2.5: DMD masks created using Autocad™.

Additional structures are created to help position the mask when using a 20x lens, as graphene can be difficult to see in a mask writer tool.

An important parameter in the mask writing process is the exposure time, which affects the ability to develop fine structures. By using an array of different exposure times (fig. 2.6), the optimal feature result was found for a typical developing time.

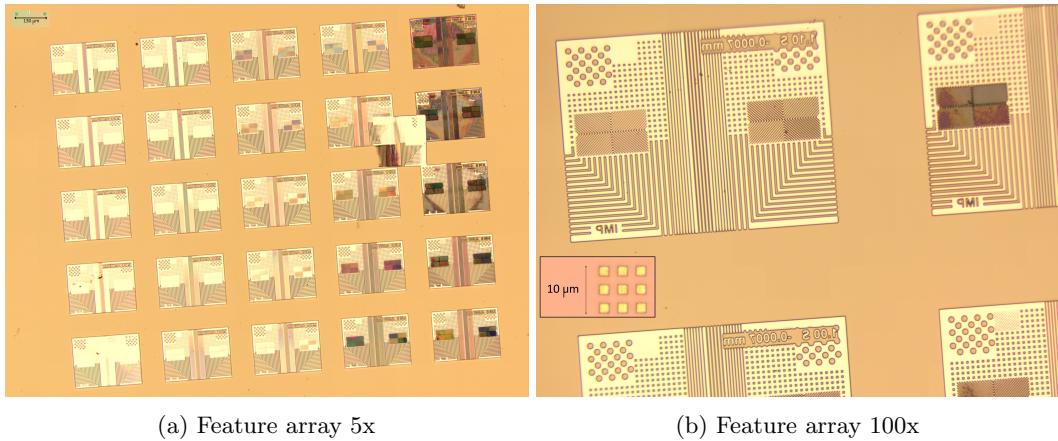


Figure 2.6: Developing an exposure array on SiO₂

Developers

Developers are used to dissolve exposed / unexposed areas of photoresist films. We use AZ-726 in conjunction with AZ-1512HS. Using a development time complementary to the exposure time is important to not overdevelop features, as material in proximity to exposed areas is at risk of some structural damage, and developers continue to react with the remaining structure over time.

2.1.4 UV Ozone surface preparation

Large resistances can occur when trying to make contact with graphene. This can be for a variety of reasons. Resist residues between the deposited pads and graphene can be insulating, perhaps non-metallic bonding occurs between deposited metals and graphene, or the oxidisation of metals being deposited (ie, chromium oxide) could occur.

Several studies by Li *et al*^[10] and Nath *et al*^[11;12] have shown the ability to reduce contact resistance of graphene by using UV ozone treatment, to less than 200 Ω , a small contact resistance.

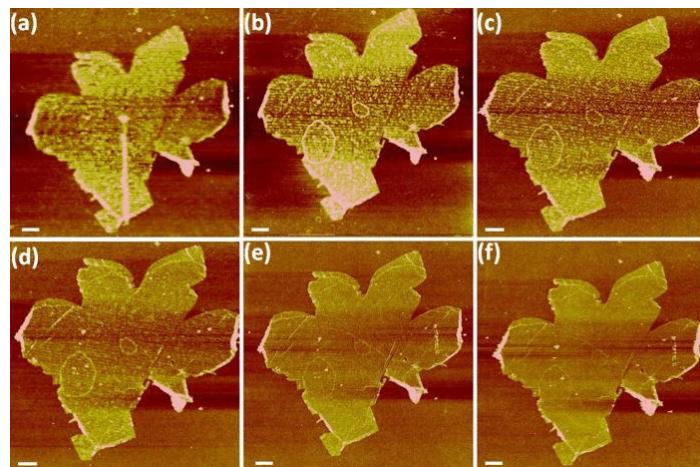


Figure 2.7: Cleaning of graphene using UV Ozone (Source: Li *et al.* [10])
 (a) Before transfer (b) After photolithography (c)→(f) UVO treatment for 5, 10, 16, 22min,
 respectively. Scale bar: 1μm.

UV Ozone treatment refers to the use of UV light to generate photochemical reactions on sample surfaces. 185nm light is used to generate ozone O_3 from bonding molecular (O_2) oxygen, while 254nm light is used to dissociate ozone to molecular and singlet oxygen (O_1), the latter of which is reactive with substrate surfaces. Increasing stage temperature also will increase the etching rate that occurs. UV Ozone is used in this context to clean the graphene exposed in our developed wells, as seen in fig. 2.7.

To determine an appropriate etching time for the particular tool used, two wafers with grapehe flakes at times of 5m and 15m were cleaned using UV Ozone. The 15m devices were etched away completely, however the 5m device provided the first low resistance contact observed, after many iterations of devices.

2.1.5 Deposition

Once a designed structure is built to make contacts with graphene and cleaned using UV Ozone, material can now be deposited onto the device. There are many different methods, including sputtering and thermal evaporation, however electron beam evaporation (fig. 2.8) was used for these devices, due to its uniformity, control of deposition rate, and the availability of various material crucibles.

50nm of Au (Gold) was originally deposited with a Cr (Chromium) adhesion layer of 5nm to promote contact to SiO_2 , however issues with metallic contact to graphene arose. In case of chromium oxidisation during deposition, creating an insulating layer to graphene, a thinner layer (2nm) of chromium was instead deposited. This is reasonable as pinhole effects resulting from a thin deposited Cr layer do not affect bulk transport.

Oxide Protection

In using metal liquids to cover devices with oxides, the gold reacted strongly to the liquid metallic environment, destroying pre-established pads. This is further described in chapter 5, however the result was to use additional layers, another layer of Cr 2nm and a layer of SiO_2 20nm. These additional layers do not prevent contact through contact probes and provide insulation from the bulk of metal liquid reactions.

2.1.6 Lift-off

To remove the remaining gold covered photoresist on the substrate, a solvent called PG remover is used to emerse samples at 80 °C. Using a pipette to generate soft fluid flow around the device, the excess gold is slowly removed.

Ultrasonication

After lift off, the presence of skin remenants (described in section 2.1.3) could sometimes be cleaned off through the use of ultrasonication (fig. 2.10), however this had a large risk of damaging the graphene, seen in fig. 2.11.

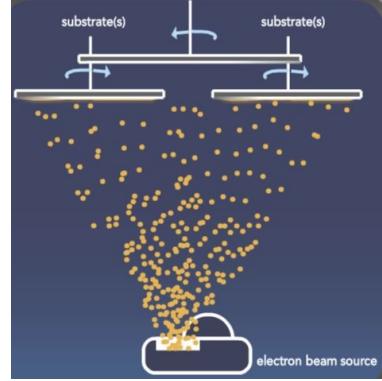
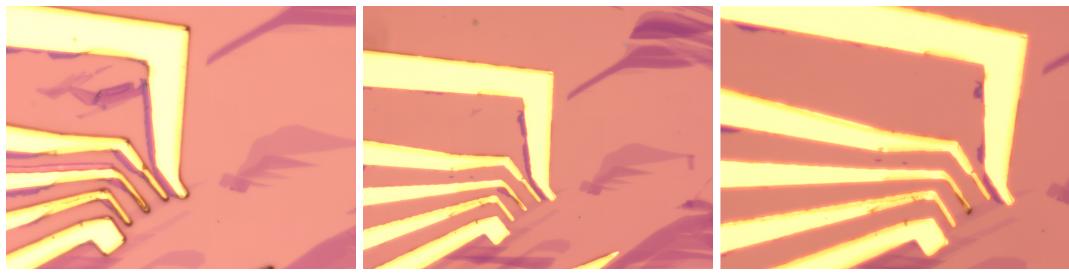


Figure 2.8: E-beam Evaporation
(Source: [13])



Figure 2.9: PG Remover liftoff



2.10: Ultrasonication used to remove material remanants from litho
Note the movement or loss of gold material on the middle probes



Figure 2.11: Ultrasonication that has broken graphene sample.

2.1.7 Oxide stamping

Zavabeti *et al*'s^[14] work on thin oxides synthesised by liquid metal introduces two methods to create such oxides. The first involves the exfoliation of oxide layers from the surface of metal droplets, and the second involves the suspension of oxide layers in water, created by injecting gas through the metal liquid. This section will only describe the former in detail, which is used in this project. Refer to chapter 5 for further optimisation and exploration of the liquid metal technique.

2.2 Measurement techniques

2.2.1 4 probe measurement

Limiting resistance

2.2.2 Probe station

Cooling

PID control

Vacuum

Cabling & Static Discharge

Chapter 3

Characterisation of graphene

Chapter 4

Electrical measurements of pristine graphene

4.1 CVD

4.2 Exfoliated

$$C_{\text{flake}} = \frac{G_{\text{SiO}_2} - G_{\text{flake}}}{G_{\text{SiO}_2}} \quad (4.1)$$

$$\partial R = \frac{\rho}{w} \partial L \quad (4.2)$$

$$R = \frac{V}{I} = \frac{V_a - V_b}{I_{in}} \quad (4.3)$$

$$\sigma = \sqrt{(N^* e \mu)^2 + \left(\rho_S + \frac{1}{N e \mu} \right)^{-2}} \quad (4.4)$$

$$N = \frac{C_g}{e} |V - V_G| \quad (4.5)$$

$$\rho[V_g, T] = \rho_0[V_g] + \rho_A[T] + \rho_B[Vg, T] \quad (4.6)$$

$$\rho_A[T] = \left(\frac{h}{e^2} \right) \frac{\pi 2 D a^2 k_B T}{2 h^2 \rho_S V_s^2 V_F^2} \quad (4.7)$$

$$\rho_B[V_G, T] = B \frac{h}{e^2} V_G^{-\alpha_1} \left(\frac{1}{\exp[(0.059 \text{ eV})/k_B T] - 1} + \frac{6.5}{\exp[(0.115 \text{ eV})/k_B T] - 1} \right) \quad (4.8)$$

4.2.1 hBN transfer

Chapter 5

Thin oxides

5.1 Printing

5.1.1 Al_2O_3

5.1.2 SnO

5.1.3 Bi_2O_3

5.2 Smearing

5.2.1 Ga_2O_3

Chapter 6

Conclusion

6.1 Future direction

6.2 Concluding remarks

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Appendices

Appendix A

Raman spectroscopy samples

Appendix B

Labview programs