9. Difficulties in the design occurred numerous times while creating the datapath. Routing wires was often difficult due to there being so many elements to work with. Even routing through multiple layers was difficult. Getting sizing right was also a tough thing for the MP. Even now, my design is still larger than it should be but it was even larger before I tried working with it. Debugging the design was also a pain, specifically for the layout. It became very hard to track things in the layout view.

10. a) The distance between *vdd* and *gnd* varies in the design due to smaller modules being made from different sizes. However, the median measurement between the signals was roughly 3um. I didn't really choose to have it as 3um however it is good to keep the length of the design small because the width will be VERY long (mostly due to the regfile and ALU). Along with that, we have to stack multiple bitslices on top of each other which only increases the height, so its important to minimize that distance.

b) Gates can be sized differently for a variety of reasons (as told in the question). One possible reason is to deal with race conditions with the signals. Changing the sizing of the transistors can allow two signals (one of which may be travelling slower than the other) to arrive at the same time. For example, if you have an AND gate with one input coming from metal1 but the other coming from metal3. Clearly we need the metal3 signal to come faster (or slow down the metal1 signal) to avoid problems. Resizing accomplishing this.