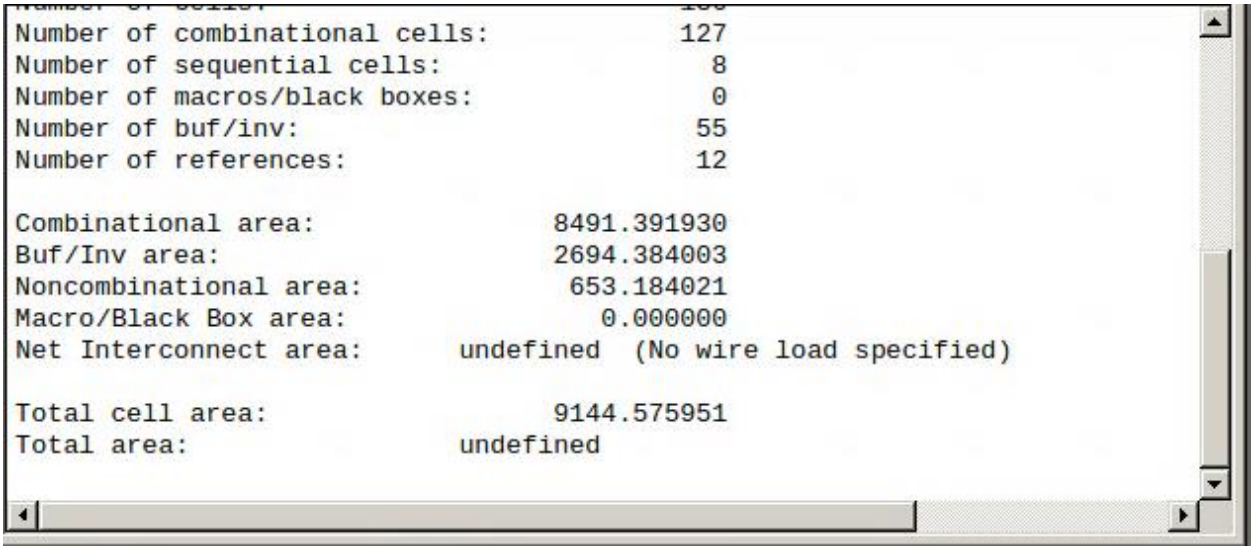
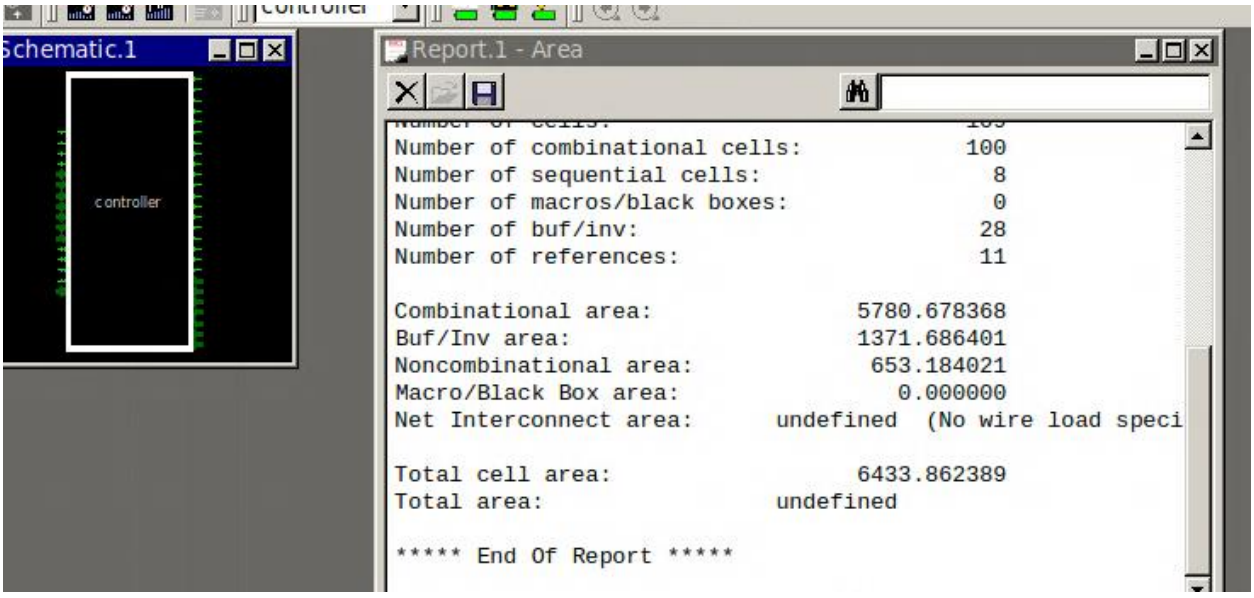
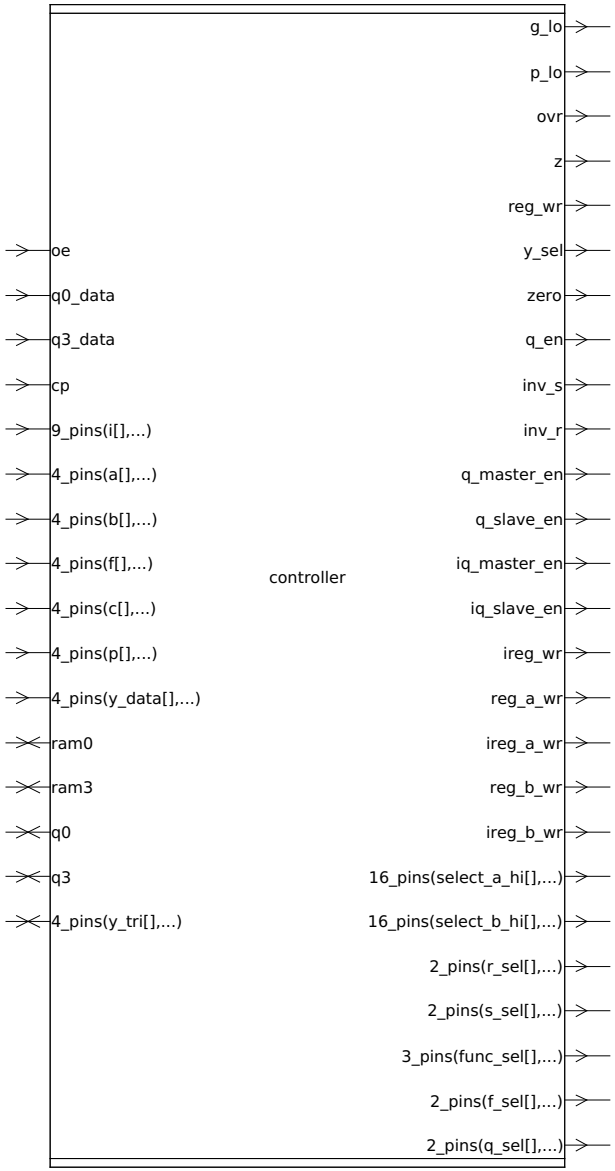
The total area of the am2901 layout is 338.4 * 108.72 = 36,790.85um^2.

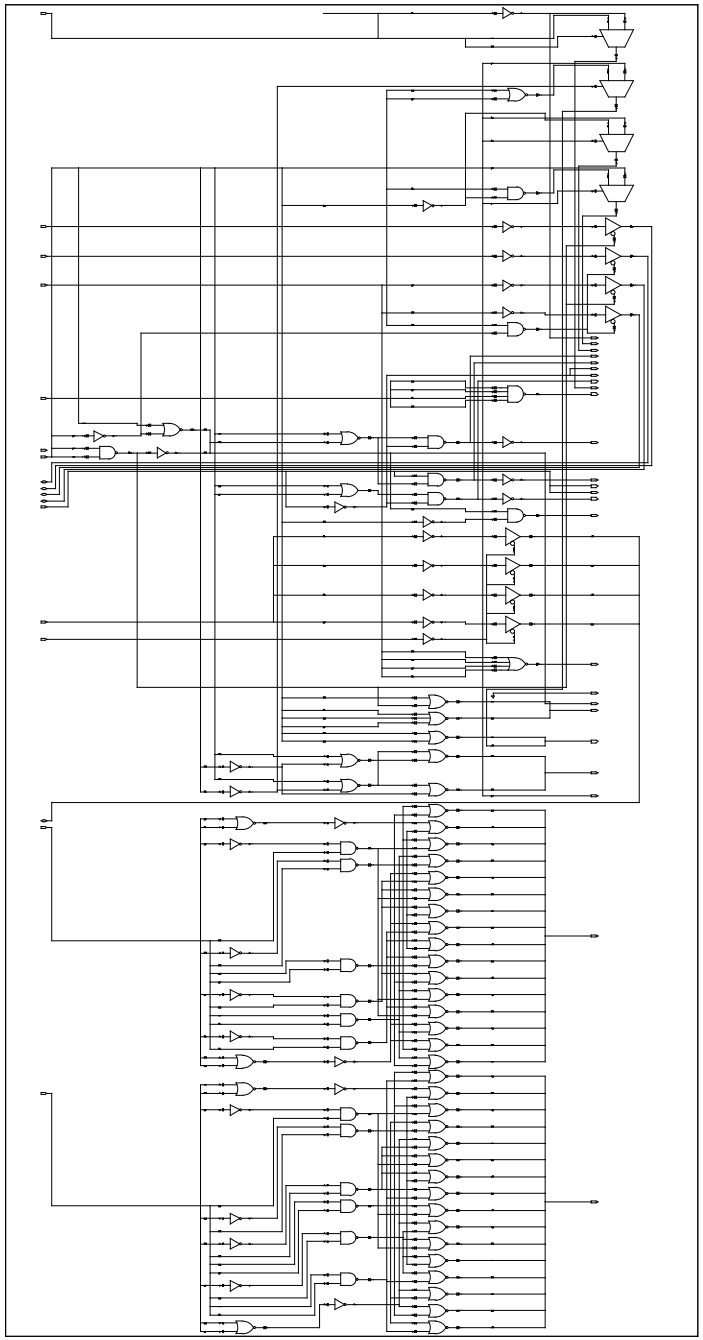
Area of Design With 275 Max Rise/Fall:



Area of Design With 325 Max Rise/Fall:




oe
q0_data
q3_data
cp
9_pins(i[],...)
4_pins(a[],...)
4_pins(b[],...)
4_pins(f[],...)
4_pins(c[],...)
4_pins(p[],...)
4_pins(y_data[],...)
ram0
ram3
q0
q3
4_pins(y_tri[],...)
controller
g_lo
p_lo
ovr
z
reg_wr
y_sel
zero
q_en
inv_s
inv_r
q_master_en
q_slave_en
iq_master_en
iq_slave_en
ireg_wr
reg_a_wr
ireg_a_wr
reg_b_wr
ireg_b_wr
16_pins(select_a_hi[],...)
16_pins(select_b_hi[],...)
2_pins(r_sel[],...)
2_pins(s_sel[],...)
3_pins(func_sel[],...)
2_pins(f_sel[],...)
2_pins(q_sel[],...)



```
#####################################################################
#  Generated by:      Cadence Encounter 14.28-s033_1
#  OS:                Linux x86_64(Host ID linux-06.ews.illinois.edu)
#  Generated on:      Thu May  2 17:37:56 2019
#  Design:            controller
#  Command:           summaryReport -noHtml -outfile summaryReport.rpt
#####################################################################


==============================
General Design Information
==============================
Design Status: Routed
Design Name: controller
# Instances: 112
# Hard Macros: 0
# Std Cells: 112
    ------------------------------
    Standard Cells in Netlist
    ------------------------------
              Cell Type   Instance Count  Area (um^2)
                  inv_1               20        979.7760
                  inv_2                6        293.9328
                  inv_4                6        293.9328
                invzp_1                8        653.1840
                 mux2_1                4        457.2288
                nand2_1                7        457.2288
                nand2_2               12        783.8208
                nand4_1                1         81.6480
                 nor2_1               33       1616.6304
                 nor2_2                8        391.9104
                 nor2_4                4        457.2288
                 nor3_1                1         65.3184
                 nor4_1                1         81.6480
                  or2_1                1         81.6480
# Pads: 0
# Net: 168
# Special Net: 2
# IO Pins:
    ------------------------------
    Issued IO Information
    ------------------------------
    # Unplaced IO Pin  0
    # Floating IO
        ------------------------------
        Floating IO
        ------------------------------
            Floating IO Name
                        q_en
                        zero
                        c[0]
                        c[1]  4
    # IO Connected to Non-IO Inst
        ------------------------------
        IO Connected to Non-IO Inst
        ------------------------------
                     IO Name      Non-IO Inst Name
                          cp                 U128
                    ireg_b_wr                U128
                     reg_b_wr                U128
                    ireg_a_wr                U128
                     reg_a_wr                U128
                      ireg_wr                U141
```

iq_slave_en	U151
iq_master_en	U149
q_slave_en	U152
q_master_en	U150
inv_r	U188
inv_s	U186
q_sel[0]	U183
q_sel[1]	U184
f_sel[0]	U147
f_sel[1]	U144
y_sel	U195
func_sel[0]	U188
func_sel[1]	U185
func_sel[2]	U186
s_sel[0]	U191
s_sel[1]	U193
r_sel[0]	U179
r_sel[1]	U182
reg_wr	U142
q3_data	U132
q0_data	U135
q3	drvqshl
q0	drvqshr
ram3	drvraml
ram0	drvramr
oe	U137
y_data[0]	U133
y_data[1]	U131
y_data[2]	U129
y_data[3]	U136
y_tri[0]	drvy0
y_tri[1]	drvy1
y_tri[2]	drvy2
y_tri[3]	drvy3
z	U139
ovr	U177
p_lo	U138
g_lo	U145
p[0]	U138
p[1]	U138
p[2]	U138
p[3]	U138
c[2]	U177
c[3]	U145
f[0]	U134
f[1]	U139
f[2]	U139
f[3]	U130
select_b_hi[0]	U114
select_b_hi[1]	U164
select_b_hi[2]	U168
select_b_hi[3]	U156
select_b_hi[4]	U116
select_b_hi[5]	U163
select_b_hi[6]	U167
select_b_hi[7]	U98
select_b_hi[8]	U115
select_b_hi[9]	U162
select_b_hi[10]	U166
select_b_hi[11]	U99
select_b_hi[12]	U122
select_b_hi[13]	U161
select_b_hi[14]	U100

```
             select_b_hi[15]                  U153
              select_a_hi[0]                  U117
              select_a_hi[1]                  U172
              select_a_hi[2]                  U176
              select_a_hi[3]                  U160
              select_a_hi[4]                  U119
              select_a_hi[5]                  U171
              select_a_hi[6]                  U175
              select_a_hi[7]                  U101
              select_a_hi[8]                  U118
              select_a_hi[9]                  U170
             select_a_hi[10]                  U174
             select_a_hi[11]                  U102
             select_a_hi[12]                  U123
             select_a_hi[13]                  U169
             select_a_hi[14]                  U103
             select_a_hi[15]                  U157
                        b[0]                   U92
                        b[1]                   U94
                        b[2]                  U104
                        b[3]                  U105
                        a[0]                   U93
                        a[1]                   U95
                        a[2]                  U106
                        a[3]                  U107
                        i[0]                  U180
                        i[1]                  U179
                        i[2]                  U179
                        i[3]                  U188
                        i[4]                  U185
                        i[5]                  U186
                        i[6]                  U148
                        i[7]                  U140
                        i[8]                  U140  103  107
# Pins:
    ------------------------------
    Correctness of Pin Connectivity for All Instances
    ------------------------------
    # Floating Terms  0
    # Output Term Marked Tie Hi/Lo  0
    # Output Term Shorted to PG Net  0  313
# PG Pins:
    ------------------------------
    Correctness of PG Pin Connectivity for All Instances
    ------------------------------
    # Instances that No Net Defined for Any PG Pin
        ------------------------------
        The Instances that No Net Defined for any PG Pin
        ------------------------------
               Instance Name
                        U196
                        U195
                        U194
                        U193
                        U192
                        U191
                        U190
                        U189
                        U188
                        U187
                        U186
                        U185
                        U184
```

U183
U182
U181
U180
U179
U177
U176
U175
U174
U173
U172
U171
U170
U169
U168
U167
U166
U165
U164
U163
U162
U161
U160
U159
U158
U157
U156
U155
U154
U153
U152
U151
U150
U149
U148
U147
U146
U145
U144
U143
U142
U141
U140
U139
U138
U137
U136
U135
U134
U133
U132
U131
U130
U129
U128
U127
U126
U125
U124
U123
U122
U121
U120

```
                        U119
                        U118
                        U117
                        U116
                        U115
                        U114
                        U113
                        U112
                        U111
                        U110
                        U109
                        U108
                        U107
                        U106
                        U105
                        U104
                        U103
                        U102
                        U101
                        U100
                         U99
                         U98
                         U97
                         U96
                         U95
                         U94
                         U93
                         U92
                    drvraml
                    drvqshl
                    drvramr
                    drvqshr
                      drvy3
                      drvy2
                      drvy1
                      drvy0  112
    # Floating PG Terms  0
    # PG Pins Connect to Non-PG Net  0
    # Power Pins Connect Ground Net  0
    # Ground Pins Connect Power Net  0  224
Average Pins Per Net(Signal): 1.863

==============================
General Library Information
==============================
# Routing Layers: 5
# Masterslice Layers: 12
# Pin Layers:
    General Caution:
        1) Library have metal1, metal2, metal3, metal4 and metal5 pins, you should setP
reRouteAsObs {1 2 3}                                    to ensure these pins are accessibl
e after placement

    ------------------------------
    Pin Layers
    ------------------------------
    metal5
    metal4
    metal3
    metal2
    metal1  5
# Layers:
    ------------------------------
```

```
    Layer metal5 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  2.160 um
    Wire Pitch Y  2.160 um
    Wire Width  0.480 um
    Spacing  0.480 um
    ------------------------------
    Layer via4 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via4
        ------------------------------
                Vias in via4  Default
                        M5_M4      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal4 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via3 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via3
        ------------------------------
                Vias in via3  Default
                        M4_M3      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal3 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via2 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via2
        ------------------------------
                Vias in via2  Default
                        M3_M2      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal2 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
```

```
    Spacing  0.480 um
    ------------------------------
    Layer via Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via
        ------------------------------
                 Vias in via  Default
                       M2_M1      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal1 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.360 um
    ------------------------------
    Layer cc Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer cc
        ------------------------------
                  Vias in cc  Default
                     M1_POLY       No
                        NTAP       No
                        M1_N       No
                        M1_P       No  For complete list click here
    ------------------------------
    Layer nodrc Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer metalcap Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer cap_id Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer res_id Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer text Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer sblock Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer pad Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer glass Information
```

```
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer poly Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer pactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nwell Information
    ------------------------------
    Type  Masterslice  22
# Pins without Physical Port: 0
# Pins in Library without Timing Lib:
    ------------------------------
    Pins in Library without timing lib
    ------------------------------
               Cell Name      List of Pin Name
                  ABnorC                   ip1
                  ABnorC                   ip2
                  ABnorC                   ip3
                  ABnorC                    op
                   ABorC                   ip1
                   ABorC                   ip2
                   ABorC                   ip3
                   ABorC                    op
           ab_or_c_or_d                    ip1
           ab_or_c_or_d                    ip2
           ab_or_c_or_d                    ip3
           ab_or_c_or_d                    ip4
           ab_or_c_or_d                     op
                 and2_1                    ip1
                 and2_1                    ip2
                 and2_1                     op
                 and2_2                    ip1
                 and2_2                    ip2
                 and2_2                     op
                 and2_4                    ip1
                 and2_4                    ip2
                 and2_4                     op
                 and3_1                    ip1
                 and3_1                    ip2
                 and3_1                    ip3
                 and3_1                     op
                 and3_2                    ip1
                 and3_2                    ip2
                 and3_2                    ip3
                 and3_2                     op
                 and3_4                    ip1
                 and3_4                    ip2
                 and3_4                    ip3
                 and3_4                     op
                 and4_1                    ip1
                 and4_1                    ip2
                 and4_1                    ip3
                 and4_1                    ip4
                 and4_1                     op
```

and4_2	ip1
and4_2	ip2
and4_2	ip3
and4_2	ip4
and4_2	op
and4_4	ip1
and4_4	ip2
and4_4	ip3
and4_4	ip4
and4_4	op
buf_1	ip
buf_1	op
buf_2	ip
buf_2	op
buf_4	ip
buf_4	op
bufzp_2	c
bufzp_2	ip
bufzp_2	op
cd_12	ip
cd_12	op
cd_16	ip
cd_16	op
cd_8	ip
cd_8	op
dksp_1	ck
dksp_1	ip
dksp_1	q
dksp_1	qb
dksp_1	sb
dp_1	ck
dp_1	ip
dp_1	q
dp_2	ck
dp_2	ip
dp_2	q
dp_4	ck
dp_4	ip
dp_4	q
drp_1	ck
drp_1	ip
drp_1	q
drp_1	rb
drp_2	ck
drp_2	ip
drp_2	q
drp_2	rb
drp_4	ck
drp_4	ip
drp_4	q
drp_4	rb
drsp_1	ck
drsp_1	ip
drsp_1	q
drsp_1	rb
drsp_1	s
drsp_2	ck
drsp_2	ip
drsp_2	q
drsp_2	rb
drsp_2	s
drsp_4	ck
drsp_4	ip

drsp_4	q
drsp_4	rb
drsp_4	s
dtrsp_2	ck
dtrsp_2	ip
dtrsp_2	q
dtrsp_2	rb
dtrsp_2	s
dtrsp_2	sip
dtrsp_2	sm
fulladder	a
fulladder	b
fulladder	ci
fulladder	co
fulladder	s
inv_1	ip
inv_1	op
inv_2	ip
inv_2	op
inv_4	ip
inv_4	op
invzp_1	c
invzp_1	ip
invzp_1	op
invzp_2	c
invzp_2	ip
invzp_2	op
invzp_4	c
invzp_4	ip
invzp_4	op
jkrp_2	ck
jkrp_2	j
jkrp_2	k
jkrp_2	q
jkrp_2	qb
jkrp_2	rb
lp_1	ck
lp_1	ip
lp_1	q
lp_2	ck
lp_2	ip
lp_2	q
lrp_1	ck
lrp_1	ip
lrp_1	q
lrp_1	rb
lrp_2	ck
lrp_2	ip
lrp_2	q
lrp_2	rb
lrp_4	ck
lrp_4	ip
lrp_4	q
lrp_4	rb
lrsp_1	ck
lrsp_1	ip
lrsp_1	q
lrsp_1	rb
lrsp_1	s
lrsp_2	ck
lrsp_2	ip
lrsp_2	q
lrsp_2	rb

lrsp_2	s
lrsp_4	ck
lrsp_4	ip
lrsp_4	q
lrsp_4	rb
lrsp_4	s
mux2_1	ip1
mux2_1	ip2
mux2_1	op
mux2_1	s
mux2_2	ip1
mux2_2	ip2
mux2_2	op
mux2_2	s
mux2_4	ip1
mux2_4	ip2
mux2_4	op
mux2_4	s
mux3_2	ip1
mux3_2	ip2
mux3_2	ip3
mux3_2	op
mux3_2	s0
mux3_2	s1
mux4_2	ip1
mux4_2	ip2
mux4_2	ip3
mux4_2	ip4
mux4_2	op
mux4_2	s0
mux4_2	s1
nand2_1	ip1
nand2_1	ip2
nand2_1	op
nand2_2	ip1
nand2_2	ip2
nand2_2	op
nand2_4	ip1
nand2_4	ip2
nand2_4	op
nand3_1	ip1
nand3_1	ip2
nand3_1	ip3
nand3_1	op
nand3_2	ip1
nand3_2	ip2
nand3_2	ip3
nand3_2	op
nand3_4	ip1
nand3_4	ip2
nand3_4	ip3
nand3_4	op
nand4_1	ip1
nand4_1	ip2
nand4_1	ip3
nand4_1	ip4
nand4_1	op
nand4_2	ip1
nand4_2	ip2
nand4_2	ip3
nand4_2	ip4
nand4_2	op
nand4_4	ip1

nand4_4	ip2
nand4_4	ip3
nand4_4	ip4
nand4_4	op
nor2_1	ip1
nor2_1	ip2
nor2_1	op
nor2_2	ip1
nor2_2	ip2
nor2_2	op
nor2_4	ip1
nor2_4	ip2
nor2_4	op
nor3_1	ip1
nor3_1	ip2
nor3_1	ip3
nor3_1	op
nor3_2	ip1
nor3_2	ip2
nor3_2	ip3
nor3_2	op
nor3_4	ip1
nor3_4	ip2
nor3_4	ip3
nor3_4	op
nor4_1	ip1
nor4_1	ip2
nor4_1	ip3
nor4_1	ip4
nor4_1	op
nor4_2	ip1
nor4_2	ip2
nor4_2	ip3
nor4_2	ip4
nor4_2	op
nor4_4	ip1
nor4_4	ip2
nor4_4	ip3
nor4_4	ip4
nor4_4	op
not_ab_or_c_or_d	ip1
not_ab_or_c_or_d	ip2
not_ab_or_c_or_d	ip3
not_ab_or_c_or_d	ip4
not_ab_or_c_or_d	op
or2_1	ip1
or2_1	ip2
or2_1	op
or2_2	ip1
or2_2	ip2
or2_2	op
or2_4	ip1
or2_4	ip2
or2_4	op
or3_1	ip1
or3_1	ip2
or3_1	ip3
or3_1	op
or3_2	ip1
or3_2	ip2
or3_2	ip3
or3_2	op
or3_4	ip1

```
                  or3_4                   ip2
                  or3_4                   ip3
                  or3_4                    op
                  or4_1                   ip1
                  or4_1                   ip2
                  or4_1                   ip3
                  or4_1                   ip4
                  or4_1                    op
                  or4_2                   ip1
                  or4_2                   ip2
                  or4_2                   ip3
                  or4_2                   ip4
                  or4_2                    op
                  or4_4                   ip1
                  or4_4                   ip2
                  or4_4                   ip3
                  or4_4                   ip4
                  or4_4                    op
                xnor2_1                   ip1
                xnor2_1                   ip2
                xnor2_1                    op
                xnor2_2                   ip1
                xnor2_2                   ip2
                xnor2_2                    op
                 xor2_1                   ip1
                 xor2_1                   ip2
                 xor2_1                    op
                 xor2_2                   ip1
                 xor2_2                   ip2
                 xor2_2                    op
                 padgnd                  pad
          padbidirhe_025                  di
          padbidirhe_025                 dib
          padbidirhe_025                  do
          padbidirhe_025                 oeb
          padbidirhe_025                 pad
                 padinc                   di
                 padinc                  dib
                 padinc                  pad
                  padio                 data
                  padio                  pad
                 padout                   di
                 padout                  dib
                 padout                   do
                 padout                  pad
                 padvdd                  pad
             padnoconnect                pad  338
# Pins Missing Direction: 0
Antenna Summary Report:
    General Caution:
        1) All Antenna Constructs are absent for the layer section of LEF.
        2) All Antenna Constructs are absent for the macro section of LEF.For more info
rmation click here
# Cells Missing LEF Info: 0
# Cells with Dimension Errors: 0

==============================
Netlist Information
==============================
# HFO (>200) Nets: 0
# No-driven Nets: 16
    General Caution:
        1) TODO
```

```
    No-driven Nets
    N35
    N34
    N33
    N25
    N24
    N23
    i_0
    i_1
    i_2
    ireg_b_wr
    reg_b_wr
    reg_a_wr
    q_en
    i[3]
    i[4]
    i[5]
# Multi-driven Nets: 0
# Assign Statements: 16
    General Caution:
        1) The assignment statements can impact CTS and IPO.
        2) You can use "setDoAssign" properly to slove the problem.

    Verilog File Name: controller_synth.v
    Module Name: controller
    ireg_b_wr = ireg_a_wr
    q_sel[1] = N35
    q_sel[0] = N34
    f_sel[0] = N33
    r_sel[1] = N25
    r_sel[0] = N24
    f_sel[1] = N23
    reg_a_wr = cp
    reg_b_wr = reg_a_wr
    func_sel[0] = i[3]
    func_sel[1] = i[4]
    func_sel[2] = i[5]
    i_0 = i[0]
    i_1 = i[1]
    i_2 = i[2]
    zero = 1'b0
Is Design Uniquified: YES
# Pins in Netlist without timing lib:
    ------------------------------
    Pins in Netlist without timing lib
    ------------------------------
    Cell Name  List of Pin Name
    inv_1  ip
    inv_1  op
    inv_2  ip
    inv_2  op
    inv_4  ip
    inv_4  op
    invzp_1  c
    invzp_1  ip
    invzp_1  op
    mux2_1  ip1
    mux2_1  ip2
    mux2_1  op
    mux2_1  s
    nand2_1  ip1
    nand2_1  ip2
    nand2_1  op
```

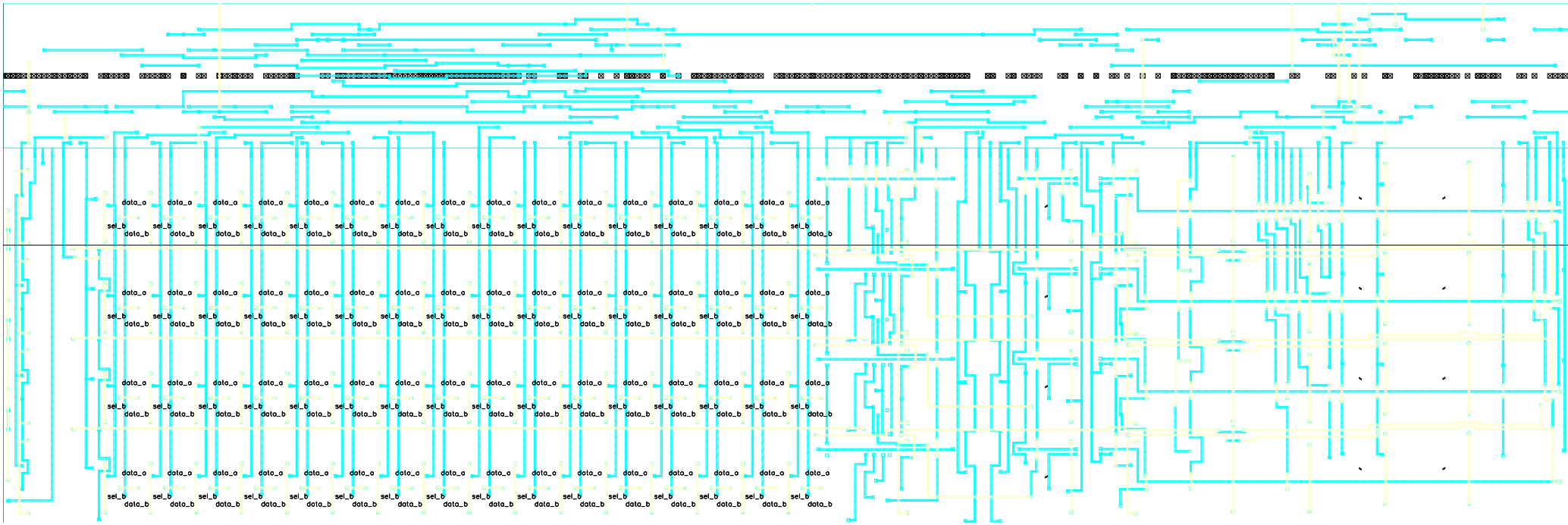
```
    nand2_2  ip1
    nand2_2  ip2
    nand2_2  op
    nand4_1  ip1
    nand4_1  ip2
    nand4_1  ip3
    nand4_1  ip4
    nand4_1  op
    nor2_1  ip1
    nor2_1  ip2
    nor2_1  op
    nor2_2  ip1
    nor2_2  ip2
    nor2_2  op
    nor2_4  ip1
    nor2_4  ip2
    nor2_4  op
    nor3_1  ip1
    nor3_1  ip2
    nor3_1  ip3
    nor3_1  op
    nor4_1  ip1
    nor4_1  ip2
    nor4_1  ip3
    nor4_1  ip4
    nor4_1  op
    or2_1  ip1
    or2_1  ip2
    or2_1  op  45

==============================

==============================
: Internal  External
No of Nets:        147           0
No of Connections:        269           0
Total Net Length (X): 3.2539e+03  0.0000e+00
Total Net Length (Y): 1.9172e+03  0.0000e+00
Total Net Length: 5.1711e+03  0.0000e+00

==============================
Timing Information
==============================
# Clocks in design: 0
# Generated clocks: 0
# "dont_use" cells from .libs: 0
# "dont_touch" cells from .libs: 0
# Cells in .lib with max_tran: 0
# Cells in .lib with max_cap: 0
# Cells in .lib with max_fanout: 0
SDC max_cap: N/A
SDC max_tran: N/A
SDC max_fanout: N/A
Default Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

==============================
Floorplan/Placement Information
==============================
Total area of Standard cells: 6695.136 um^2
Total area of Standard cells(Subtracting Physical Cells): 6695.136 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
```

Total area of Pad cells: 0.000 um^2
Total area of Core: 10233.216 um^2
Total area of Chip: 10233.216 um^2
Effective Utilization: 6.8562e-01
Number of Cell Rows: 2
% Pure Gate Density #1 (Subtracting BLOCKAGES): 65.426%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 65.426%
% Pure Gate Density #3 (Subtracting MACROS): 65.426%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 65.426%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 65.426%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES and Physical Cells): 65.426%
% Core Density (Counting Std Cells and MACROs): 65.426%
% Core Density #2(Subtracting Physical Cells): 65.426%
% Chip Density (Counting Std Cells and MACROs and IOs): 65.426%
% Chip Density #2(Subtracting Physical Cells): 65.426%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

==============================
Wire Length Distribution
==============================
Total metal1 wire length: 355.6800 um
Total metal2 wire length: 1630.3200 um
Total metal3 wire length: 2634.9000 um
Total metal4 wire length: 186.6600 um
Total metal5 wire length: 476.2800 um
Total wire length: 5283.8400 um
Average wire length/net: 31.4514 um
Area of Power Net Distribution:

Area of Power Net Distribution			
Layer Name	Area of Power Net	Routable Area	Percentage
metal1	892.4256	10233.2160	8.7209%
metal2	130.6368	10233.2160	1.2766%
metal3	0.0000	10233.2160	0.0000%
metal4	0.0000	10233.2160	0.0000%
metal5	0.0000	10233.2160	0.0000%

For more information click here


data_a
sel_b
data_b