Networked Embedded Systems Lab
Prof. Marco Zimmerling

Introduction to Embedded Systems – WS 2022/23

Sample Solution to Exercise 1: SPI, I/O, Polling, and Interrupts

Task 1: Memory Map

Task 1.1: Memory Addresses

Answer the following questions for the MSP432 processor, as used as an example in the lecture:

(a) How many different addresses are available for peripherals?

(b) How many different addresses are available for ports?

(c) Suppose an LED is connected to Pin 5 of Port 2. Determine the memory address of Port 2, and the value which has to be written to this address to turn the LED on.

(d) How many bytes can be written in the ROM region?
How many 32-bit words can be written in the ROM region?

Solution to Task 1.1:

Using the MSP432 data sheet, we find the following:

1. Section 6.3 "Memory Map" presents Figure 6-1 "Device Memory Zones". Here, we see peripherals have the address range: [0x4000_0000, 0x5FFF_FFFF]. The number of total addressable locations is thus

   $$0x5FFF\_FFFF - 0x4000\_0000 + 1 = 0x2000\_0000,$$

   or 2^{29} addresses.

2. Section 6.3.3 "Peripheral Zone Memory Map" presents Figure 6-4 of the same name, where we see there exists a "Peripheral Region". In Section 6.3.3.1 "Peripheral Region" we see Table 6-1 "Peripheral Address Offsets" which further partitions the region. In this table we find the "Port Module", and it has the address range: [0x4000_4C00, 0x4000_4FFF]. The number of total addressable locations is thus

   $$0x4000\_4FFF - 0x4000\_4C00 + 1 = 0x0400,$$

   or 2^{10} addresses.

3. Table 6-1 refers to Table 6-21 for details of the "Port Module". Table 6-21 "Port Registers" tells that the base address of this region is 0x4000_4C00, and "Port 2 Output" has an address offset of 003h[1]. Together, this means that Port 2's output address is

   $$0x4000\_4C00 + 0x0003 = 0x4000\_4C03.$$

   Pin 5 is the sixth least significant bit (LSB) of Port 2. This can be seen in the MSP-432 schematic. This means the following value should be written to this address: 0b0010_0000, or 0x0020.

[1] 003h is an alternative way to wite 0x0003

4. Figure 6-1 "Device Memory Zones" shows that there is a "Code" zone. Figure 6-2 "Code Zone Memory Map" tells us that there exists a ROM region, and it has an address range: [0x0200_0000, 0x020F_FFFF]. The number of total addressable locations in this region is thus

   $$\text{0x020F\_FFFF - 0x0200\_0000} + 1 = \text{0x0010\_0000},$$

   which is 2^{20} addresses. In the MSP432, each address location corresponds to one byte. Therefore, the addressable memory space is 2^{20} Byte or 1 MByte. The number of 4-byte words is a quarter of that, which is 2^{18} words or 256 kilo words.

   Note that Section 6.4.3 "ROM" states that the MSP432P401x MCUs supports 32KB of ROM, and the rest of the 1MByte ROM region is reserved for future upgrades. Also note that the developer can not write to these addresses, only the manufacturer can.

Task 1.2: SRAM Design

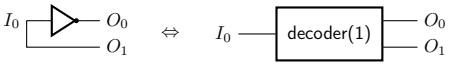
Determine the optimal partitioning of SRAM address bits into row select bits, used to select word lines, and column select bits, used to select bit lines. The objective is to minimize the area of the SRAM. Use the following data for your computations:

- Row select bits, to select a word line: u
- Column select bits, to select a bit line: w
- The address is 8-bit: $u + w = 8$
- Area of a memory cell: $A_{\text{mem}} = 6$
- Area of a 2-to-1 multiplexer: $A_{\text{mux}} = 4$
- Area of a 2-input AND gate: $A_{\text{AND}} = 1$
- Area of a NOT gate: $A_{\text{NOT}} = 1$
- Area of a wire: $A_{\text{wire}} = 0$
- Area of a sense amplifier: $A_{\text{sense}} = 5$

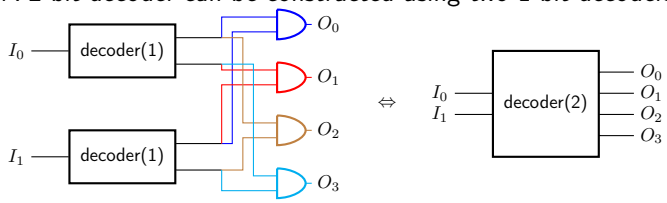
It is assumed that the multiplexer is dual channel, meaning a single multiplexer can be used to select both BL and $\overline{\text{BL}}$.

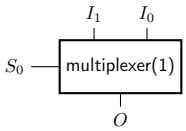
Hint: Use recursive construction to build decoders from smaller decoders and 2-input AND gates. Use a recursive tree-like construction to build large multiplexers from smaller ones. An example of these constructions is given below.

A 1-bit decoder can be constructed using a NOT gate:



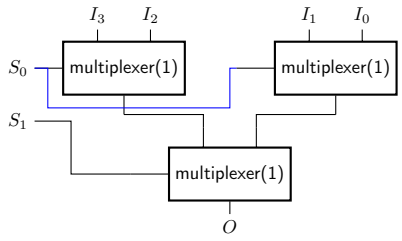
A 2-bit decoder can be constructed using two 1-bit decoders and four 2-input AND gates:





The area of a 2-to-1 multiplexer is given, and we can represent it using:

A 4-to-1 multiplexer can be constructed using three 2-to-1 multiplexers:



Solution to Task 1.2:

To build the SRAM with u row select bits and w column select bits, we need (a) $2^{(u+w)}$ memory cells, (b) one u-bit decoder, (c) one 2^w-to-1 multiplexer, and (d) 2^w sense amplifiers.

(a) For a 8-bit address, we need 2^8 memory cells. The area C occupied by memory cells is thus

$$C = 2^8 \cdot A_{\text{mem}} = 1536.$$

(b) For activating one of the 2^u word lines, we need a u-bit decoder. In general, we can construct a k-bit decoder using using two smaller decoders and 2^k 2-input AND gates. The smaller decoders should be of size $k/2$ is k is even, or of sizes $(k+1)/2$ and $(k-1)/2$ if k is odd. Therefore, the area $D(k)$ of a k-bit decoder is given by

$$D(k) = \begin{cases} A_{\text{NOT}} & \text{if } k = 1 \\ 2 \cdot D(\frac{k}{2}) + A_{\text{AND}} \cdot 2^k & \text{if } k > 1 \text{ and } k \text{ is even} \\ D(\frac{k-1}{2}) + D(\frac{k+1}{2}) + A_{\text{AND}} \cdot 2^k & \text{if } k > 1 \text{ and } k \text{ is odd} \end{cases}$$

(c) For selecting one of the 2^w bit lines, we need a 2^w-to-1 multiplexer. In general, we can construct a 2^k-to-1 multiplexer for any k using two 2^{k-1}-to-1 multiplexers and one 2-to-1 multiplexer. Therefore, the area $M(k)$ of a multiplexer with k select pins is given by

$$M(k) = \begin{cases} A_{\text{mux}} & \text{if } k = 1 \\ 2 \cdot M(k-1) + A_{\text{mux}} & \text{otherwise} \end{cases}$$

(d) We need a single sense amplifier for each column bit line. Therefore, for w column bit lines, the area of all sense amplifiers is

$$S(w) = 2^w \cdot A_{\text{sense}}$$

There are eight possible solutions or design points for u and w. The area of the control circuit, i.e. the area excluding the memory cells $D(u) + M(w) + S(w)$, is given in Table 1 for different design points. We see from

u	w	Decoder $D(u)$	Multiplexer $M(w)$	Sense Amp $S(w)$	Total
0	8	0	1020	1280	2300
1	7	1	508	640	1149
2	6	6	252	320	578
3	5	15	124	160	299
4	4	28	60	80	168
5	3	53	28	40	121
6	2	94	12	20	126
7	1	171	4	10	185
8	0	312	0	5	317

Table 1: Design points for the SRAM

the table that $u = 5$ and $w = 3$ is the optimal design point. The total area of SRAM is thus in this case:

$$C + D(u = 5) + M(w = 3) + S(w = 3) = 1536 + 53 + 28 + 40 = 1657$$

Task 2: Communication

Suppose that a sender and a receiver exchange data via UART with the following configuration:

- The baudrate is 115200 bits/s
- UART is set up with 1 start bit, 2 stop bits, 8 data bits, and 1 parity bit
- 16 clock periods are used for sampling 1 bit

Answer the following questions:

(a) What is the required clock frequency?

(b) Suppose a 48 MHz clock. What is a suitable division factor?

(c) How long does it take to transfer 10 MBytes of data?

(d) Suppose that we use division factor as computed in part ((b)). The sender has a basic clock frequency of 48 MHz. What is the range of clock frequencies of the receiver such that:

- all symbols are correctly recognized, and
- the signal is stable between one period before and one period after the sampling time.

Solution to Task 2:

(a) It takes 16 clock ticks to sample 1 bit, and the baud rate is 115200 bits/s. Therefore, the required clock frequency is:

$$115200\,\text{bits/s} \cdot 16\,\text{/bits} = 1.8432\,\text{MHz}$$

(b) The ratio between the given and the required clock is:

$$\frac{48\,\text{MHz}}{1.8432\,\text{MHz}} = 26.04167$$

Thus, a 26 division factor can be used.

(c) To send 1 Byte (8 bits) of data via UART, we need to transmit a total of $1 + 2 + 8 + 1 = 12$ bits of data and overhead. We will call these data and overhead bits 'symbols' to differentiate from data bits. The total payload for transmission is

$$10 \cdot 2^{20} \cdot 8 \cdot 12/8\,\text{symbols}$$

The time taken to transmit this payload is

$$T = \frac{10 \cdot 2^{20} \cdot 8 \cdot 12/8\,\text{symbols}}{115200\,\text{symbols/s}} = 1092.27\,\text{s}$$

(d) We'll call the sender's data transmission rate r_s, and the receiver's data reception rate r_r. From part (b) we know the division factor, so we have the following:

$$r_s = \frac{48 \cdot 10^6}{16 \cdot 26}\,\text{Hz}, \qquad r_r = \frac{F_r}{16 \cdot 26},$$

where F_r is the unknown clock frequency. Let the communication start at time 0. The sender transmits the kth symbol during time

$$\left(\frac{(k-1)}{r_s}, \frac{k}{r_s}\right),$$

and the receiver samples the kth symbol at time

$$\frac{k-0.5}{r_r}.$$

For correct reception of the kth symbol, it has to be constant for a clock cycle before and after the sample time:

$$\left(\frac{k-0.5}{r_r}+\frac{1}{r_r\cdot 16}, \frac{k-0.5}{r_r}-\frac{1}{r_r\cdot 16}\right).$$

We now have two extreme situations:

1. If receiver is *slower* than the sender, the second stop bit is 'critical'. To be sampled correctly, it has to be sampled before the second stop bit ends. Thus we have

$$\begin{aligned}\frac{12-0.5}{r_r}+\frac{1}{r_r\cdot 16} &\leq \frac{12}{r_s}\\ r_r &\geq \frac{11.5\cdot 16+1}{12\cdot 16}\cdot r_s = \frac{46.25\,\mathrm{MHz}}{16\cdot 26}\end{aligned}$$

2. If receiver is *faster* than the sender, the first stop is 'critical'. To be sampled correctly, it has to be sampled after the start of the first stop bit. Thus we have

$$\begin{aligned}\frac{10+0.5}{r_r}-\frac{1}{r_r\cdot 16} &\geq \frac{10}{r_s}\\ r_r &\leq \frac{10.5\cdot 16-1}{10\cdot 16}\cdot r_s = \frac{50.1\,\mathrm{MHz}}{16\cdot 26}\end{aligned}$$

Combining these two inequalities, we get the valid range of clock frequencies for the receiver:

$$46.25\,\mathrm{MHz} \leq F_r \leq 50.1\,\mathrm{MHz}$$

Task 3: Interrupts and Polling

An external event is sensed using polling, with a period P. It takes 100 cycles to process the event. The processor frequency is 48 MHz. Before starting a new period, the previous polling task should have finished. The relative deadline for processing an event is 10μs.

(a) Determine the range of feasible polling periods P.

(b) Suppose now that an unrelated interrupt may occur, and the interrupt has a higher priority than the processing of the polling event. Including all overheads, it takes 40 cycles to process the interrupt. The minimum time between two subsequent interrupts is T. Suppose that T is larger than 140 cycles. Determine the range of feasible polling periods P.

(c) Find the minimum time between two interrupts T, and the corresponding polling period P, such that the polling period is feasible.

Solution to Task 3:

(a) The computation time C of the polling event can be calculated using the processor frequency:

$$C = \frac{100}{48\cdot 10^6\,\mathrm{Hz}} = 2.0833\,\mu\mathrm{s}$$

The maximum response time of the event is $P+C$, and this response time must not exceed the deadline:

$$P + 2.0833\,\mu\mathrm{s} \leq 10\,\mu\mathrm{s}$$

The polling period must not be less than the computation time:

$$P \geq 2.0833\,\mu\text{s}$$

Combining these conditions, we get the range for $P \in [2.0833\,\mu\text{s}, 7.9167\,\mu\text{s}]$.

(b) The time taken to process one interrupt is:

$$\frac{40}{48 \cdot 10^6\,\text{Hz}} = 0.833\,\mu\text{s}$$

If the minimum time between two interrupts is not less than 140 cycles, then there can be at most one interrupt within the processing of one polling event. Therefore, we can make the worst-case assumption that while a polling event is processed, an additional 40 cycles are spent in interrupt processing. Then the range for P is:

$$\begin{aligned} 2.0833\,\mu\text{s} + 0.8333\,\mu\text{s} + P &\leq 10\,\mu\text{s} \\ P &\geq 2.08\,\mu\text{s} + 0.8333\,\mu\text{s} \\ \Rightarrow \quad 2.9167\,\mu\text{s} \leq P &\leq 7.0833\,\mu\text{s} \end{aligned}$$

(c) Let E be the total computations done within one polling period, and let the number of interrupts during the processing of one event be k. We have that

$$E = 100 + 40 \cdot k$$

The conditions for (a) no deadline miss and (b) the polling task finishes before the start of a new period are

$$\begin{aligned} \frac{E}{48 \cdot 10^6\,\text{Hz}} + P &\leq 10\,\mu\text{s} \\ P &\geq \frac{E}{48 \cdot 10^6\,\text{Hz}} \end{aligned}$$

If we minimize T, we maximize k. k is in turn maximizes E, and E is bounded by $P \cdot 48 \cdot 10^6$ Hz. Therefore, we have that

$$2 \cdot \frac{E}{48 \cdot 10^6\,\text{Hz}} \leq 10\mu\text{s} \quad \Rightarrow \quad E \leq 240\ [\text{cycles}]$$

Assuming the largest feasible value of E, we have

$$k = \frac{240 - 100}{40} = 3.5.$$

This means at most 3 interrupts can be processed fully during the processing of one event. The time taken for processing one event and three interrupts is

$$\frac{100 + 40 \cdot 3}{48 \cdot 10^6\,\text{Hz}} = 4.583\,\mu\text{s}$$

The minimum feasible time between two interrupts is $T = 4.583\,\mu\text{s}/3 = 1.528\,\mu\text{s}$.

The feasible range for the polling period is $P \in [4.583\,\mu\text{s}, 5.417\,\mu\text{s}]$.