Embedded Systems Exercise 1 - HS 2020

7./9.10.2020

Stefan Draskovic

Exercise structure

- **Goal of today's exercise:**
  - A bit of everything to get you started
- **Agenda:**
  - Wednesday 16:15 - 17:00 Introduction and solving a sample question (recorded)
  - Friday 16:15 - 17:00 Solutions (recorded)
- **Available assistants:**
  - Stefan Drašković
  - Francesca Marsicano

Exercise structure

- **Interactions:**
  - **Exercise Zoom:** Questions can be asked throughout the exercise in this room by raising your hand. Please feel free to write in the chat in case we oversee your question.
  - **Help Zoom:** Student assistants are available throughout the session for 1-on-1 meetings under the Zoom Meeting ID 917 6971 5701.
  - **Matrix Chatroom:** Questions that are relevant for everyone can be asked in the Matrix chatroom where the responsible assistants can answer as quickly as possible.

Content of today's exercise

Memory Addresses, SRAM Design, UART Communication, Interrupt & Polling

Task 1.1: Memory Addresses

Learn to use the MSP-432 datasheet

Note difference between *address* and *memory*

(a) How many different addresses are available for peripherals?

(b) How many different addresses are available for ports?

(c) Suppose an LED is connected to Pin 5 of Port 2. Determine the memory address of Port 2, and the value which has to be written to this address to turn the LED on.

(d) How many bytes can be written in the ROM region?
How many 32-bit words can be written in the ROM region?

Task 1.1 Solution

(a) Peripherals addresses have the following range **[0x4000_0000, 0x5FFF_FFFF]**.
Total addressable locations = 0x5FFF_FFFF - 0x4000_0000 + 1 = **0x2000_0000** or 2^{29}.

(b) Port addresses have the following range **[0x4000_4C00, 0x4000_4FFF]**. Total addressable locations = 0x4000_4FFF - 0x4000_4C00 + 1 = **0x0400** or 2^{10}.

(c) Port 2 address = **0x4000_4C00 + 0x0003 = 0x4000_4C03**
Following binary value should be written to this address: $\mathbf{00100000_2}$.

(d) ROM addresses have the following range **[0x0200_0000, 0x020F_FFFF]**. Total addressable locations = 0x020F_FFFF - 0x0200_0000 + 1 = **0x010_0000** or 2^{20} Bytes $\rightarrow$ 1 Mega byte.
Number of 4 Byte words: $2^{20}/4$ words = **256 kilo words**.

Task 1.2: SRAM Design

Determine the optimal partitioning of SRAM address bits into row select (used to select word lines) and column select (used to select bit lines) bits. The objective is to minimize the area of the SRAM. Use the follow data for your computations:

u: Number of bits to select a word line

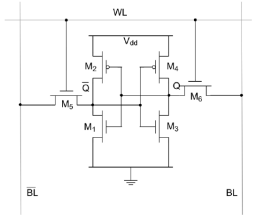
w: Number of bits to select a bit line

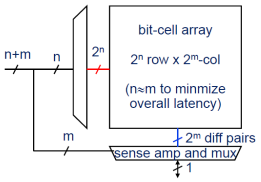
- Rows u + Columns w = 8
- Area of 1 memory cell: $A_{\text{mem}} = 6$
- Area of 2-1 mux: $A_{\text{mux}} = 4$
- Area of 2-input AND gate: $A_{\text{AND}} = 1$
- Area of Invetrer: $A_{\text{NOT}} = 1$
- $A_{\text{wires}} = 0$
- Area 1 bit sense-amp: $A_{\text{sense}} = 5$

SRAM Architecture

Components that contribute to area of memory:

- Area of memory cells.
- Area of decoder for activating word lines.
- Area of multiplexer for selecting bit-lines.
- Area of sense amplifiers.





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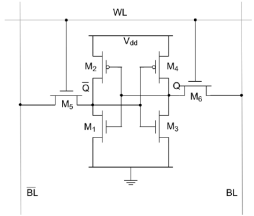
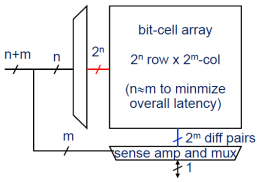
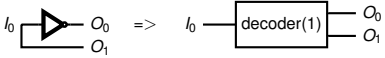




Decoder construction



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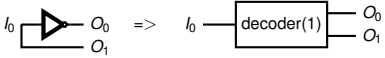
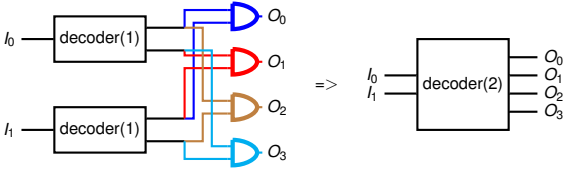
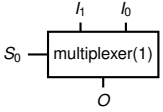


2-bit decoder can be constructed using two 1-Bit decoders and 4 AND gates:



Multiplexer construction

2-to-1 multiplexer is represented using:



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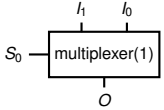
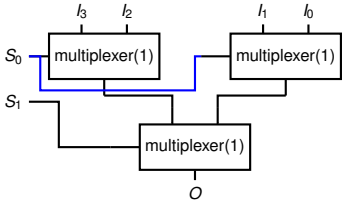


4-to-1 multiplexer can be constructed using 3x 2-to-1 multiplexers:



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- k bit decoder can be constructed using:
  - 2 Decoders of sizes:
  - $\{\frac{k}{2}, \frac{k}{2}\}$ if k is even.
  - $\{\frac{k-1}{2}, \frac{k+1}{2}\}$ if k is odd.
  - 2^k 2-Input AND gates.

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$$D(k) = \begin{cases} A_{\text{NOT}} & \text{if } k = 1 \\ 2 \cdot D(\frac{k}{2}) + A_{\text{AND}} \cdot 2^k & \text{if } k > 1 \text{ and } k \text{ is even} \\ D(\frac{k-1}{2}) + D(\frac{k+1}{2}) + A_{\text{AND}} \cdot 2^k & \text{if } k > 1 \text{ and } k \text{ is odd} \end{cases}$$

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- 2^l-to-1 multiplexer can be constructed using:
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  - One 2-to-1 multiplexer.

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$$M(k) = \begin{cases} A_{\text{mux}} = 4 & \text{if } k = 1 \\ 2 \cdot M(k-1) + A_{\text{mux}} & \text{otherwise} \end{cases}$$

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u	w	Decoder	Multiplexer	Sense Amp	Total
0	8	0	1020	1280	2300
1	7	1	508	640	1149
2	6	6	252	320	578
3	5	15	124	160	299
4	4	28	60	80	168
5	3	53	28	40	121
6	2	94	12	20	126
7	1	171	4	10	223
8	0	312	0	5	317

Task 2: Communication

Suppose that a sender and a receiver exchange data via UART with following configuration: Baudrate = 115200 bits/s; 1 start bit, 2 stop bits, 8 data bits, 1 parity bit; 16 clock periods used for sampling 1 bit

Answer the following questions:

(a) What is the required clock frequency?

(b) Suppose a 48 MHz clock. What is a suitable division factor?

(c) How long does it take to transfer 10 MBytes of data?

(d) Suppose that we use division factor as computed in part b. The sender has a basic clock frequency of 48 MHz. What is the range of clock frequencies of the receiver such that:

- all symbols are correctly recognized.
- signal is stable between 1 period before and after the sampling time.

Task 2 Solution

(a) The clock frequency is: $115200 \cdot 16 = 1.8432\text{MHz}$.

(b) The division factor is: $\frac{48 \times 10^6}{1.8432 \times 10^6 \text{Hz}} = 26.04167 \Rightarrow 26$

(c) 1 byte uses $1 + 2 + 8 + 1 = 12$ symbols. The total payload is $10 \times 10^6 \times 12$ symbols. The time taken to transmit the payload is:

$$T = \frac{10 \times 10^6 \cdot 12 \text{ symbols}}{115200 \text{ symbols}/\text{s}} = 1041.67\text{s}$$

Task 2 Solution

(d) Sender's transmission rate: $r_s = \frac{48 \times 10^6 \text{Hz}}{26}$.
Receiver's reception rate: $r_r = \frac{F_r}{26}$. F_r =?.

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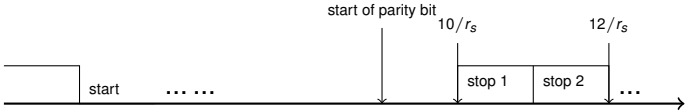

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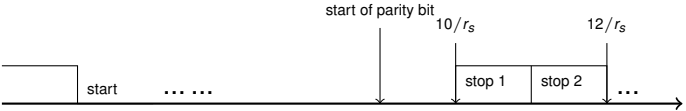

For correct reception of all bits, we have the following two conditions:

- If receiver is *slower*, the second stop bit must be sampled no later than $\frac{12}{r_s} - \frac{1}{r_r \cdot 16}$.
- If receiver is *faster*, the first stop bit must be sampled no earlier than $\frac{10}{r_s} + \frac{1}{r_r \cdot 16}$.

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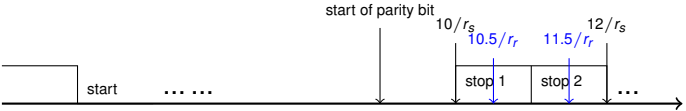

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The time when receiver samples the first and second stop bit is $\frac{10.5}{r_r}$, $\frac{11.5}{r_r}$, respectively. Therefore: $\frac{11.5}{r_r} \leq \frac{12}{r_s} - \frac{1}{r_r \cdot 16} \Rightarrow F_r \geq 46.25\text{MHz}$.
$\frac{10.5}{r_r} \geq \frac{10}{r_s} + \frac{1}{r_r \cdot 16} \Rightarrow F_r \leq 50.1\text{MHz}$.

$$46.25\text{MHz} \leq F_r \leq 50.1\text{MHz}$$

Task 3: Interrupt and Polling

An external event is sensed using polling with period P. It takes 100 cycles to process the event. Processor frequency is 48 MHz. Before starting a new period, the previous polling task should have finished. The relative deadline for processing an event is $10\mu s$.

(a) Determine the range of feasible polling periods.
(b) Suppose now that an unrelated interrupt may occur and the interrupt has higher priority than the code for processing the polling event. Including all overhead, it takes 40 cycles to process the interrupt. The minimum time between two subsequent interrupts is T. Suppose that T is larger than 140 cycles. Determine the range of feasible polling periods.
(c) What is the minimum feasible time between two interrupts T, and the corresponding feasible polling period P?

Task 3(a) Solution

Computation time is: $C = \frac{100}{48 \times 10^6 \text{Hz}} = 2.0833 \mu\text{s}$

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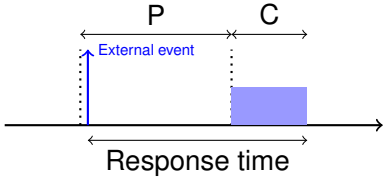

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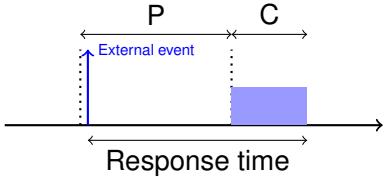

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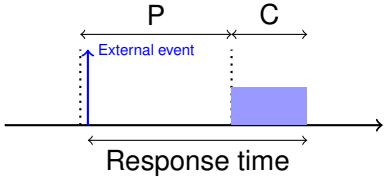

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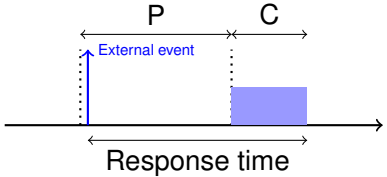

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Polling period must not be less than computation time: $P \geq 2.0833\mu\text{s}$

Therefore: $2.0833\mu\text{s} \leq P \leq 7.9167\mu\text{s}$

Task 3(b) Solution

Time taken for processing one interrupt: $\frac{40}{48 \times 10^6} = 0.833\mu s$.
There can be at-most one interrupt within the processing of one polling request (because of 140 cycles between subsequent interrupts).
Making worst-case assumption that whenever a polling request is processed, 40 cycles are spent in interrupt processing.
$2.0833\mu s + 0.8333\mu s + P \leq 10\mu s$
$P \geq 2.08\mu s + 0.8333\mu s$
Therefore: $2.9167 \leq P \leq 7.0833\mu s$

Task 3(c) Solution

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E = Total computations in one polling period, k= the maximum number of interrupts within one polling period.

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Maximizing E to maximize k: $E = P \cdot 48 \times 10^6$ (inequality (b)). Therefore:

$2 \cdot \frac{E}{48 \times 10^6} \leq 10\mu s \quad => \quad E \leq 240$ cycles

$k \leq \frac{240-100}{40} = \lfloor 3.5 \rfloor \; k \leq 3.$

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Time taken for processing one event and three interrupts: $\frac{100+40 \cdot 3}{48 \times 10^6} = 4.583\mu s$.

Minimum feasible value of $T = \frac{4.583}{3} = 1.528\mu s$

Feasible range for polling period: $4.583\mu s \leq P \leq 5.417\mu s$

Further reading

- **Lecture slides:**
  - Lecture slide Chapter 3

Questions?

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