Embedded Systems Exercise 1 - HS 2020

7./9.10.2020

Stefan Draskovic

Exercise structure

- **Goal of today's exercise:**
  - A bit of everything to get you started
- **Agenda:**
  - Wednesday 16:15 - 17:00 Introduction and solving a sample question (recorded)
  - Friday 16:15 - 17:00 Solutions (recorded)
- **Available assistants:**
  - Stefan Drašković
  - Francesca Marsicano

Exercise structure

- **Interactions:**
  - **Exercise Zoom:** Questions can be asked throughout the exercise in this room by raising your hand. Please feel free to write in the chat in case we oversee your question.
  - **Help Zoom:** Student assistants are available throughout the session for 1-on-1 meetings under the Zoom Meeting ID 917 6971 5701.
  - **Matrix Chatroom:** Questions that are relevant for everyone can be asked in the Matrix chatroom where the responsible assistants can answer as quickly as possible.

Content of today's exercise

Memory Addresses, SRAM Design, UART Communication, Interrupt & Polling

Introductory questions - Question 1

In the MSP432, how many different addresses are available for peripherals?

- ☐ 2^{20}
- ☐ 2^{24}
- ☐ 2^{29}
- ☐ 2^{30}

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Introductory questions - Question 2

In the MSP432, how many different addresses are available for ports?

- ☐ 2^{10}
- ☐ 2^{12}
- ☐ 2^{14}
- ☐ 2^{16}

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Task 1.1: Memory Addresses

Learn to use the MSP-432 datasheet

Note difference between *address* and *memory*

(a) How many different addresses are available for peripherals?

(b) How many different addresses are available for ports?

(c) Suppose an LED is connected to Pin 5 of Port 2. Determine the memory address of Port 2, and the value which has to be written to this address to turn the LED on.

(d) How many bytes can be written in the ROM region?
How many 32-bit words can be written in the ROM region?

Task 1.2: SRAM Design

Determine the optimal partitioning of SRAM address bits into row select (used to select word lines) and column select (used to select bit lines) bits. The objective is to minimize the area of the SRAM. Use the follow data for your computations:

u: Number of bits to select a word line

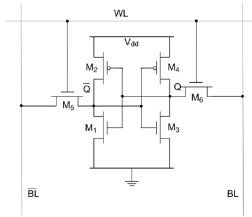
w: Number of bits to select a bit line

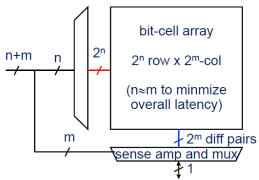
- Rows u + Columns w = 8
- Area of 1 memory cell: $A_{\text{mem}} = 6$
- Area of 2-1 mux: $A_{\text{mux}} = 4$
- Area of 2-input AND gate: $A_{\text{AND}} = 1$
- Area of Invetrer: $A_{\text{NOT}} = 1$
- $A_{\text{wires}} = 0$
- Area 1 bit sense-amp: $A_{\text{sense}} = 5$

SRAM Architecture

Components that contribute to area of memory:

- Area of memory cells.
- Area of decoder for activating word lines.
- Area of multiplexer for selecting bit-lines.
- Area of sense amplifiers.





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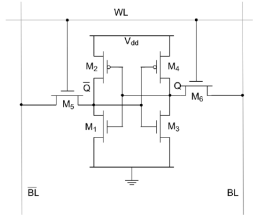
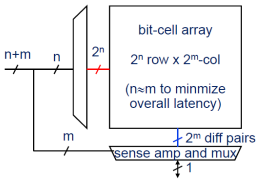
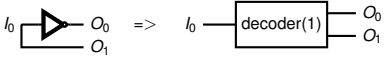




Decoder construction



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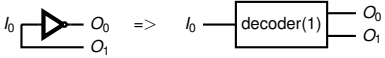
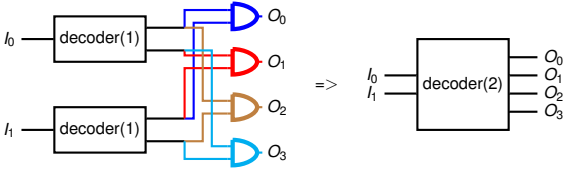
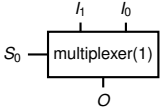


2-bit decoder can be constructed using two 1-Bit decoders and 4 AND gates:



Multiplexer construction

2-to-1 multiplexer is represented using:



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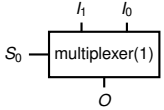
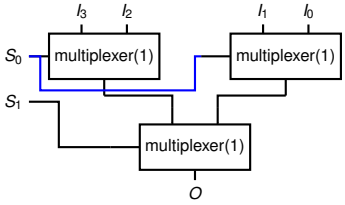


4-to-1 multiplexer can be constructed using 3x 2-to-1 multiplexers:



Task 2: Communication

Suppose that a sender and a receiver exchange data via UART with following configuration: Baudrate = 115200 bits/s; 1 start bit, 2 stop bits, 8 data bits, 1 parity bit; 16 clock periods used for sampling 1 bit

Answer the following questions:

(a) What is the required clock frequency?

(b) Suppose a 48 MHz clock. What is a suitable division factor?

(c) How long does it take to transfer 10 MBytes of data?

(d) Suppose that we use division factor as computed in part b. The sender has a basic clock frequency of 48 MHz. What is the range of clock frequencies of the receiver such that:

- all symbols are correctly recognized.
- signal is stable between 1 period before and after the sampling time.

Task 3: Interrupt and Polling

An external event is sensed using polling with period P. It takes 100 cycles to process the event. Processor frequency is 48 MHz. Before starting a new period, the previous polling task should have finished. The relative deadline for processing an event is $10\mu s$.

(a) Determine the range of feasible polling periods.
(b) Suppose now that an unrelated interrupt may occur and the interrupt has higher priority than the code for processing the polling event. Including all overhead, it takes 40 cycles to process the interrupt. The minimum time between two subsequent interrupts is T. Suppose that T is larger than 140 cycles. Determine the range of feasible polling periods.
(c) What is the minimum feasible time between two interrupts T, and the corresponding feasible polling period P?

Task 3(a) Solution

Computation time is: $C = \frac{100}{48 \times 10^6 \text{Hz}} = 2.0833 \mu\text{s}$

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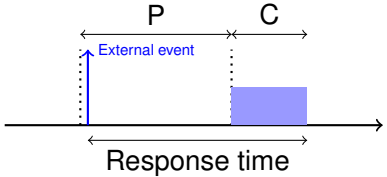
Maximum response time:



Worst-case response time is: $P + C$

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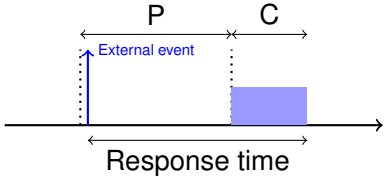

Worst-case response time is: $P + C$

Response time must not exceed deadline: $P + 2.0833\mu\text{s} \leq 10\mu\text{s}$

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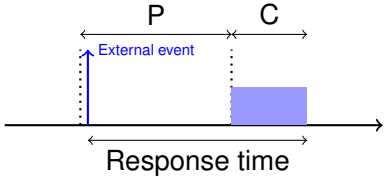

Worst-case response time is: $P + C$

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Polling period must not be less than computation time: $P \geq 2.0833\mu\text{s}$

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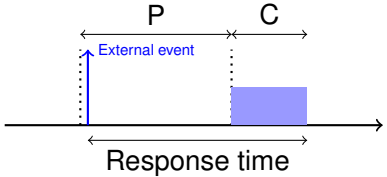

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Therefore: $2.0833\mu\text{s} \leq P \leq 7.9167\mu\text{s}$

Further reading

- **Lecture slides:**
  - Lecture slide Chapter 3

Questions?

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