Networked Embedded Systems Lab
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Introduction to Embedded Systems – WS 2022/23

Exercise 1: SPI, I/O, Polling, and Interrupts

Task 1: Memory Map

Task 1.1: Memory Addresses

Answer the following questions for the MSP432 processor, as used as an example in the lecture:

(a) How many different addresses are available for peripherals?

(b) How many different addresses are available for ports?

(c) Suppose an LED is connected to Pin 5 of Port 2. Determine the memory address of Port 2, and the value which has to be written to this address to turn the LED on.

(d) How many bytes can be written in the ROM region?
How many 32-bit words can be written in the ROM region?

Task 1.2: SRAM Design

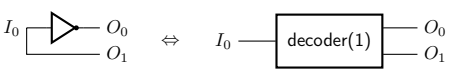
Determine the optimal partitioning of SRAM address bits into row select bits, used to select word lines, and column select bits, used to select bit lines. The objective is to minimize the area of the SRAM. Use the following data for your computations:

- Row select bits, to select a word line: u
- Column select bits, to select a bit line: w
- The address is 8-bit: $u + w = 8$
- Area of a memory cell: $A_{\text{mem}} = 6$
- Area of a 2-to-1 multiplexer: $A_{\text{mux}} = 4$
- Area of a 2-input AND gate: $A_{\text{AND}} = 1$
- Area of a NOT gate: $A_{\text{NOT}} = 1$
- Area of a wire: $A_{\text{wire}} = 0$
- Area of a sense amplifier: $A_{\text{sense}} = 5$

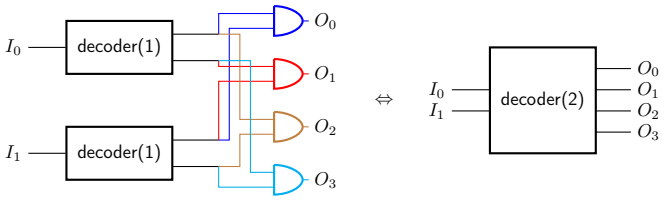
It is assumed that the multiplexer is dual channel, meaning a single multiplexer can be used to select both BL and $\overline{\text{BL}}$.

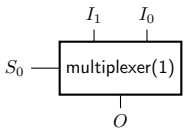
Hint: Use recursive construction to build decoders from smaller decoders and 2-input AND gates. Use a recursive tree-like construction to build large multiplexers from smaller ones. An example of these constructions is given below.

A 1-bit decoder can be constructed using a NOT gate:

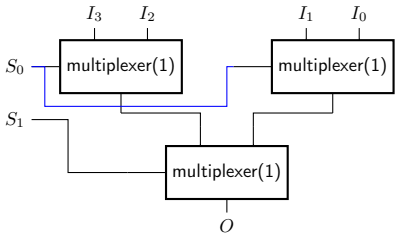


A 2-bit decoder can be constructed using two 1-bit decoders and four 2-input AND gates:





The area of a 2-to-1 multiplexer is given, and we can represent it using:
A 4-to-1 multiplexer can be constructed using three 2-to-1 multiplexers:



Task 2: Communication

Suppose that a sender and a receiver exchange data via UART with the following configuration:

- The baudrate is 115200 bits/s
- UART is set up with 1 start bit, 2 stop bits, 8 data bits, and 1 parity bit
- 16 clock periods are used for sampling 1 bit

Answer the following questions:

(a) What is the required clock frequency?

(b) Suppose a 48 MHz clock. What is a suitable division factor?

(c) How long does it take to transfer 10 MBytes of data?

(d) Suppose that we use division factor as computed in part ((b)). The sender has a basic clock frequency of 48 MHz. What is the range of clock frequencies of the receiver such that:

- all symbols are correctly recognized, and
- the signal is stable between one period before and one period after the sampling time.

Task 3: Interrupts and Polling

An external event is sensed using polling, with a period P. It takes 100 cycles to process the event. The processor frequency is 48 MHz. Before starting a new period, the previous polling task should have finished. The relative deadline for processing an event is 10μs.

(a) Determine the range of feasible polling periods P.

(b) Suppose now that an unrelated interrupt may occur, and the interrupt has a higher priority than the processing of the polling event. Including all overheads, it takes 40 cycles to process the interrupt. The minimum time between two subsequent interrupts is T. Suppose that T is larger than 140 cycles. Determine the range of feasible polling periods P.

(c) Find the minimum time between two interrupts T, and the corresponding polling period P, such that the polling period is feasible.