Image Masking Accelerator Conceptual Design

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***Abstract*—This report serves as a conceptual design for the Image Masking Accelerator (IMA) project proposed for the 2020 High Performance Embedded Systems course at the University of Cape Town. Contained within this report is a high level conceptual design, time and role management plans, as well as a report on progress made thus far. All designs and proposed plans contained within this report are subject to change.**

I. Conceptual Design

In preparation for this project, we had to narrow down the functionality of the IMA in order break down the accelerator into separately implementable and testable modules. The functionality specifications for this conceptual design can be found under Plan A of our project proposal. [1]

Figure 1 shows the conceptual design, which splits the IMA into three core modules. Essential to the IMA will be the user control over which images are selected as masks, and which images are to be used for overlaying. This control is afforded to the user by means of buttons (with integrated debounce modules) and an SD-card slot on the FPGA. These will serve as inputs to our memory controller module, which will implement the needed communication protocol with the SD-card to retrieve the needed images, and store them in BRAM. Potential inspiration for memory controller can be found at ZipCPU's SD-card controller [2]

The acquired images will then be processed from BRAM according to Figure 3 of our project proposal [1] and will occur in the following order, with steps one and two taking place concurrently and i representing the bit value:

1) $II_1^{[i]} = (Image\ 1^{[i]} \oplus Mask^{[i]}).(Image\ 1^{[i]})$
2) $II_2^{[i]} = (Image\ 1^{[i]} \oplus !Mask^{[i]}).(Image\ 1^{[i]})$
3) $Overlaid\ Image^{[i]} = II_1^{[i]} \oplus II_2^{[i]}$

Intermediary results (II_1 & II_2) will be stored back into BRAM at the location previously holding the original images. This will be done to conserve limited resources on the FPGA.

The final result will then be fed to a VGA interface which will display the masked and overlaid image to a monitor at a resolution of 640x480. This resolution was selected as it is an integer multiple of the original image resolutions (320x240) which made for convenient calculations when implementing timing requirements and multiplexing logic.

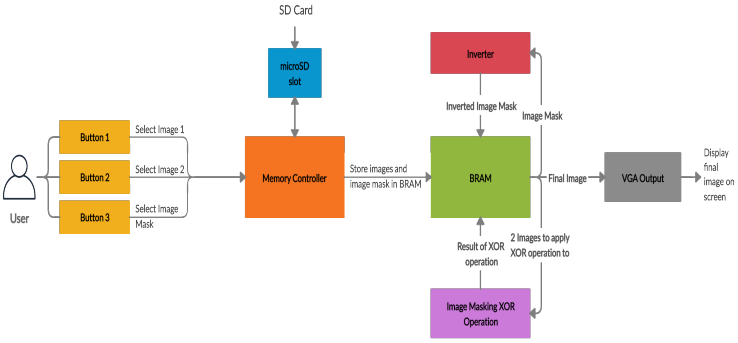

Fig. 1: High Level Conceptual Design

II. Time and Role Management

This project consists of 6 milestones, which spans across 7 weeks. Therefore, it was necessary to allocate appropriate roles and tasks for each member to undertake according to skills and individual time availability in order to work as efficiently as possible.

A. Time Management

With the above in mind, a Gantt Chart, which can be found in the Appendix, was created to track the life cycle of the project up to its completion. The Gantt Chart was used for the time allocation of the milestones of the project to ensure completion.

B. Role Management

With the aforementioned allocation in mind, it was not only important to allocate roles for each team member according to their skills and time availability, but also the resources available to them. Only two team members have access to the Nexys FPGA, and will have to be assigned roles that involve extensive hardware testing. Furthermore, the general roles assigned to each group member can be seen below in Table I where roles have been allocated according to members' strengths. The tasks assigned to each team member can be found in Table II.

III. Progress Update

As a proof of concept, we set out to implement a golden measure c++ script to emulate the core functionality of the IMA. The purpose behind this golden measure was to prove to ourselves that we understand what needs to occur at the bit

TABLE I: Role Allocation

Name	Roles
Matthew Lock	• Team Leader • Chief Hardware Tester
Luca Barbas	• Editor • Researcher • Human Resources Officer
Mahmoodah Jaffer	• Documentations Manager • Simulations Manager • Quality Assurance Manager
Lawrence Godfrey	• Blogger • Repository Manager • Software Expert

level of the IMA, as well as provide a measure against which the IMA's performance can be compared.

The first step of implementation of the golden measure was to find images that were of the correct format and resolution, namely raw 12-bit RGB colour 320x240 images. These were not readily available on the internet so we instead opted to create scripts which could down sample 24-bit RGB colour 320x240 images of varying formats. The OpenCV library was used to do this. The result of this script can be seen in Figure 2 where the original image is the 24-bit RGB colour 320x240 image, and the opposite image is the downsampled 12-bit RGB colour 320x240 image.

Fig. 2: Result of image downsampling

We then created a script which would emulate image masking at a bit level. **Take note that this script only performs one XOR image masking, and does not perform all the requirements of the IMA outlined in Plan A of the project proposal [1]. To get the expected golden measure for Plan A, we will need to multiply the run time of this golden measure by three as image overlaying requires three separate XOR maskings of the images**. The results of the golden measure can be found in Table III. No comment can be made about these results as they are the baseline results against which we will compare the IMA.

TABLE II: Division of Labour

Name	Tasks
Matthew Lock	Design and Implementation: • VGA module implementation • XOR module implementation Draft Report: • Results and conclusion • Experimentation and results summary script Final Report and Demonstration • Final compilation • Final review before submission • Reviewing the final vlog script • Reviewing and amending criticism of the Results and Conclusion
Luca Barbas	Design and Implementation: • High and low level schematics design • Design of memory controller module Draft Report: • Drafting the Abstract, Introduction and Background • Writing the summary script for the Introduction, Problem Description Final Report and Demonstration • Compiling and editing vlogs • Reviewing and amending criticism of the Abstract, Introduction and background
Mahmoodah Jaffer	Design and Implementation: • High and low level schematics design • Design of memory controller module Simulations: • Exhaustive module simulation Draft Report: • Drafting the Design section • Compiling the references • Summary script for the design section Final Report and Demonstration • Compiling and editing the vlogs • Final adjustments to the design write-up
Lawrence Godfrey	Design and Implementation: • XOR module implementation • Golden measure implementation Simulations: • Preliminary simulations Draft Report: • Proposed Development Strategy (follow-up to the methodology) • Methodology and Planned experimentation (follow-up to the methodology) • Summary script of the Methodology and conclusions summary Final Report and Demonstration • Summary script of methodology and conclusions summary • Finalizing changes of methodology, results and conclusions
All Members	• Compilation of the milestone 3 deliverable) • Recording the vlogs

Code for both the down sampling and masking scripts can found in our git repository [3].

TABLE III: Golden Measure Results

	Run Number	Run Time (ms)
XOR Image Masking	1	0.46
	2	0.48
	3	0.48
	4	0.42
	5	0.45
	(Average)	0.458

The next task we took upon ourselves was to get an image displaying using the VGA interface found on the Nexys A7 100T. To do this we implemented a VGA adapter inspired by the works of Ben Eater [4] using the timing requirements needed for an output display of 640x480.

Figure 3 shows Baby Yoda displayed to a screen using the working implementation of the VGA adapter. This is a rudimentary implementation with the image being initialised into BRAM using a coe file created from the downsampled image. A script for converting PPM images to coe initialization files, and for the working display adapter, along with simulations for timing requirements, can once again be found in our git repository [3].

Fig. 3: Baby Yoda displayed via FPGA VGA display port

REFERENCES

[1] L. G. Luca Barbas and M. Jaffer", "Ima project proposal," May 2012. [Online]. Available: https://github.com/matthew-william-lock/Image-Masking-Accelerator/tree/master/proposal

[2] ZipCPU, "Sd-card controller, using a shared spi interface," Sep 2017. [Online]. Available: https://github.com/ZipCPU/sdspi

[3] L. G. Luca Barbas and M. Jaffer", "Ima repository," May 2012. [Online]. Available: https://github.com/matthew-william-lock/Image-Masking-Accelerator

[4] B. Eater, "The world's worst video card?" Jul 2018. [Online]. Available: https://www.youtube.com/watch?v=l7rce6IQDWs

Appendix A: Item 1

Image Masking Accelerator
Matthew Locke as Project Lead
Mahmoodah Jaffer
Lawrence Godfrey
Luca Barbas

Project Start Date: **2020/05/23**

Legend: On Track | Low Risk | Med Risk | High Risk | Unassigned

Milestone Description	Category	Responsibilities Assigned To	Progress	Start	No. Days
Milestone 3: Status Update					
Snippets of Code	Med Risk	Matthew Locke	0%	2020/05/23	10
Initial Simulation	Med Risk	Lawrence Godfrey	0%	2020/05/25	10
Block diagram	On Track	Mahmoodah Jaffar	50%	2020/06/02	3
Schematics	Low Risk	Luca Barbas	0%	2020/06/02	3
Compilation of Deliverable	Low Risk	Everyone	0%	2020/06/07	1
Milestone 4: Drafting YODA Paper					
Abstract, Introduction and background	Low Risk	Luca Barbas	0%	2020/06/09	4
Methodology and Planned Experimentation	Low Risk	Lawrence Godfrey	0%	2020/06/09	3
Design	Low Risk	Mahmoodah Jaffar	0%	2020/06/09	3
Proposed Development Strategy	Med Risk	Lawrence Godfrey	0%	2020/06/11	1
Results and Conclusion	Low Risk	Matthew Locke	0%	2020/06/09	4
References	Low Risk	Mahmoodah Jaffar	0%	2020/06/13	1
Compilation and review	Low Risk	Matthew Locke	0%	2020/06/13	1
Milestone 5: Conference Presentation					
Introduction + Problem Description summary	Low Risk	Luca Barbas	0%	2020/06/16	3
Methodology/ Approach Taken summary script	Med Risk	Lawrence Godfrey	0%	2020/06/16	3
Design summary script	Med Risk	Mahmoodah Jaffar	0%	2020/06/16	3
Experimentation and Results summary script	Med Risk	Matthew Locke	0%	2020/06/16	3
Conclusions and any possible questions	Low Risk	Lawrence Godfrey	0%	2020/06/19	2
Check Script	Med Risk	Matthew Locke	0%	2020/06/19	1
Record vlog	Med Risk	Everyone	0%	2020/06/20	1
Compilation and Editing vlog	Low Risk	Luca Barbas	0%	2020/06/21	1
Milestone 6: Final Hand-in					
Abstract, Introduction and background	Low Risk	Luca Barbas	0%	2020/06/22	2
Methodology and Planned Experimentation	Low Risk	Lawrence Godfrey	0%	2020/06/22	2
Design	Low Risk	Mahmoodah Jaffar	0%	2020/06/22	2
Proposed Development	Low Risk	Lawrence Godfrey	0%	2020/06/22	2
Results and Conclusion	Low Risk	Matthew Locke	0%	2020/06/22	2
References	Low Risk	Mahmoodah Jaffar	0%	2020/06/24	1
Compilation and review	Low Risk	Matthew Locke	0%	2020/06/24	1

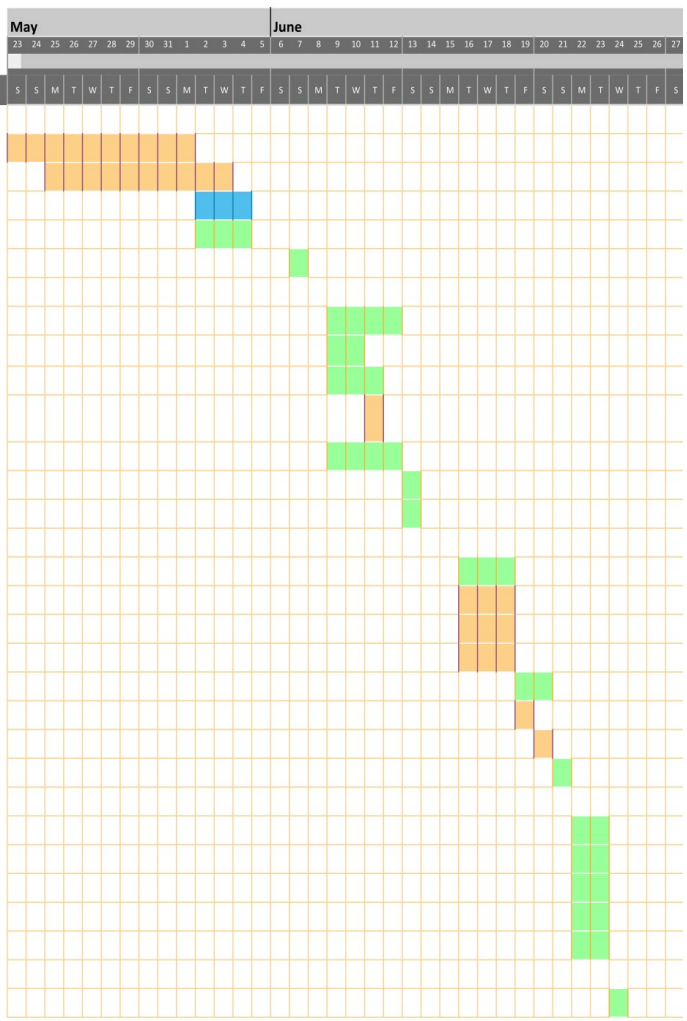

Fig. 4: Gantt Chart