MATTHEW BARONDEAU

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EDUCATION

Ph.D. in Electrical and Computer Engineering Spring 2026
University of Texas at Austin
Advisor: Dr. Andreas Gerstlauer

M.S. in Electrical and Computer Engineering Fall 2022
University of Texas at Austin; GPA 3.86/4.00

B.S. in Electrical and Computer Engineering Spring 2020
University of Texas at Austin; GPA 3.79/4.00

WORK EXPERIENCE

UT ECE – Graduate Research Assistant August 2020 – Present
- Investigating efficient thread-level parallelism for irregular memory bound workloads

Nvidia – GPU Architecture Intern May 2022 – August 2022
- Modeled multi-slice multi-partition L2 traffic into system-level cache
- Created and tuned prefetcher for irregular L2 data accesses

Tactical Computing Laboratory – Research Engineer I May 2021 – August 2021
- Profiled communication overhead in SST
- Created asynchronous execution framework for accelerator network

ARM – CPU Performance Intern May 2020 – August 2020
- Correlated MMU and L2 transactions in RTL and performance model on ARM microprocessors

UT ECE Department –Teaching Assistant August 2017 – May 2020, May 2022
- Instructed students in embedded systems and real-time operating systems courses

Lockheed Martin Missiles and Fire Control – Electrical Engineering Intern June 2019 – August 2019
- Designed fiber-optic communication and power controller interfaces

Applied Research Laboratories – Student Technician May 2018 – August 2018
- Created and tested Verilog RTL designs for GPS processing Xilinx Virtex system

Reynolds and Reynolds – IT Operations Intern Summer 2014 – 2017
- Repaired computers and installed security infrastructure at College Station office

PROJECTS

Analysis of Prefetcher Interaction with Run-ahead Execution Spring 2022
- Compared precise runahead execution against prefetcher combinations using SCARAB simulator

TinyYolo Acceleration Fall 2021
- Optimized TinyYolo on Ultra96 using code transformations and hardware accelerator,
- Resulted in 40x inference speedup over baseline

Parallelization of the Barnes-Hut Algorithm Spring 2021
- Parallelized Barnes-Hut using openMP and GPU giving 11x speedup over CPU baseline

Self-Monitor Stress Device Fall 2019 – Spring 2020
- Read physiological data to detect stress through sensors, processed using analog filters, and sent to ML model
- Awarded 2nd place in honors senior-design project category

RTOS Autonomous Racing Car Spring 2019
- Wrote real-time operating system for TI TM4C including file system, process loader, and priority scheduler
- Interfaced IR and laser sensors and tuned PID control algorithm to navigate racetrack

RELEVANT COURSEWORK

- ECE460N Computer Architecture
- ECE445M Real-Time Operating Systems
- ECE382N Advanced Embedded MCU
- ECE382M VLSI I
- CS380C Compilers
- ECE382N Parallelism & Locality
- ECE382V Semiconductor Memories
- ECE382M System on Chip Design
- CS395T Prediction Mechanisms in Computer Architecture
- ECE382N Parallel Computer Architecture

SERVICE ACTIVITIES

UT First Year Program – Fig Facilitator — Fall 2021- Present
Eta Kappa Nu Psi Chapter– Member — Fall 2019 – Spring 2021
UT First Year Program – Fig Mentor — August 2017 – December 2019

SKILLS

- **Programming Languages:** Assembly, C, C++, CUDA, Python, Verilog
- **Tools and frameworks:** LLVM, Vivado, gem5

HONORS

- Virginia & Ernest Cockrell Jr. Fellowship in Engineering