MATTHEW BARONDEAU

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https://matthewbarondeau.github.io/

EDUCATION

Ph.D. Electrical and Computer Engineering 05/2027
The University of Texas at Austin; Advisor: Andreas Gerstlauer

M.S. Electrical and Computer Engineering 12/2022
The University of Texas at Austin; GPA 3.88

B.S. Electrical and Computer Engineering 05/2020
The University of Texas at Austin; GPA 3.75

WORK EXPERIENCE

The University of Texas at Austin 08/2020 - Present
Graduate Research Assistant Austin, TX
- Investigated light-weight multithreading microarchitecture for memory-intensive workloads
- Developed dataset for ML-based proactive management for heterogeneous MPSoCs

Nvidia 05/2024 - 08/2024
Reliability and Safety Architecture Intern Santa Clara, CA
- Performed analysis and injected faults to improve data center resiliency and automotive safety
- Automated process to be chip agnostic for future exploration

Nvidia 05/2022 - 08/2022
GPU Architecture Intern Austin, TX
- Enhanced the L2 standalone simulator to simulate inter-slice communication
- Designed and optimized a GPU L2 metadata prefetcher

Tactical Computing Labs 05/2021 - 08/2021
Research Engineer I Austin, TX
- Quantified the component overhead in SST and developed a performance monitoring tool
- Implemented locality optimization for accelerator thread migration, leading to a data movement reduction

Arm 05/2020 - 08/2020
CPU Performance Intern Austin, TX
- Established a correlation between RTL and performance simulator replacement policy behavior
- Detected and rectified bugs related to the eviction process of the cache replacement policy

Lockheed Martin Missiles & Fire Control 06/2019 - 08/2019
Electrical Engineering Intern Grand Prairie, TX
- Engineered a high-current power supply controller
- Conducted comprehensive testing and characterization of a fiber communication circuit

Applied Research Labs 05/2018 - 08/2018
Student Technician Austin, TX
- Wrote RTL module to enable DMA playback of GPS data on Xilinx Virtex 7 FPGA
- Replicated analog front-end attenuation experiment to characterize system noise

SKILLS

Languages: C/C++, Python, Perl, CUDA, SystemVerilog, Assembly, HTML, CSS
Software: Git, Gem5, SST, Perf, Verilator, Intel PIN, Vivado, LLVM
Topics: Parallel computer architecture, Memory system design, Resilient computing

AWARDS

Texas ECE Graduate Leadership Award 2024
Qualcomm Innovation Fellowship 2023 - 2024
Virginia & Ernest Cockrell Jr. Fellowship in Engineering 2020 - 2024