MATTHEW BARONDEAU

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https://matthewbarondeau.github.io/

EDUCATION

Ph.D. Electrical and Computer Engineering 05/2027
The University of Texas at Austin; Advisor: Dr. Andreas Gerstlauer

M.S. Electrical and Computer Engineering 12/2022
The University of Texas at Austin; GPA 3.88

B.S. Electrical and Computer Engineering 05/2020
The University of Texas at Austin; GPA 3.75

WORK EXPERIENCE

The University of Texas at Austin, *Graduate Research Assistant* 08/2020 - Present
- Examining lightweight multithreading microarchitecture tailored for memory-intensive workloads
- Developing a proactive runtime manager for heterogeneous MPSoCs to enhance power efficiency

Nvidia, *GPU Architecture Intern* 05/2022 - 08/2022
- Enhanced the L2 standalone simulator to simulate inter-slice communication
- Designed and optimized a GPU L2 metadata prefetcher

Tactical Computing Labs, *Research Engineer I* 05/2021 - 08/2021
- Quantified the execution overhead of components in SST and developed a tool for performance monitoring
- Implemented locality optimization for accelerator thread migration, leading to a reduction in data movement costs

Arm, *CPU Performance Intern* 05/2020 - 08/2020
- Performed annotation of MMU and L2 transactions within a CPU performance simulator
- Detected and rectified bugs related to the eviction process of the cache replacement policy

Lockheed Martin Missiles & Fire Control, *Electrical Engineering Intern* 06/2019 - 08/2019
- Conducted comprehensive testing and characterization of a fiber communication circuit
- Obtained U.S. Secret security clearance

PROJECTS

Virtual Register Context Architecture 08/2020 - 11/2023
- Developed a register cache to hold partial contexts, reducing multiprocessing overhead on near-memory processors
- Crafted a register replacement policy that achieves a hit-rate within 2% of the optimal policy

Optimizing Producer-Consumer Traffic in Multi-Core Coherent Systems 08/2022 - 12/2022
- Modeled MESI coherence changes to reduce producer-consumer overheads by 2.5x

Evaluating Runahead Execution with Data Prefetching 01/2022 - 05/2022
- Evaluated precise runahead execution in concert with data prefetchers to improve prefetcher timeliness

CNN Hardware Accelerator 08/2021 - 12/2021
- Achieved 40x speedup on darknet inference on ultra96 board using SIMD and FPGA accelerator

Parallel Implementation of the Barnes-Hut Algorithm 01/2021 - 05/2021
- Wrote openMP and GPU versions of Barnes-Hut algorithm resulting in 10x speedup

SERVICE

Graduate Student Peer Mentor, ECE Partner Program, UT Austin 2021 - Present
First-Year Facilitator, First Year Experience Office, UT Austin 2021 - Present
First-Year Mentor, First Year Experience Office, UT Austin 2017 - 2020

AWARDS

Qualcomm Innovation Fellowship 2023 - 2024
Virginia & Ernest Cockrell Jr. Fellowship in Engineering 2020 - 2024

SKILLS

Languages: C/C++, Python, CUDA, System Verilog, Assembly, Java
Software: VIM, Git, Gem5, SST, CACTI, Verilator, Intel PIN, Vivado, Keil, LLVM