CS 219: Homework #7

Due on October 19th, 2016 at 4:00pm

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Problem 12

12.6) Compare zero-, one-, two-, and three-address machines by writing programs to compute $X = \frac{(A+B\times C)}{(D-E\times F)}$ for each of the four machines. The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOVE(X ← Y)	MOVE(X ← Y)
POP M	STORE M	ADD(X ← X + Y)	ADD(X ← Y + Z)
ADD	ADD M	SUB(X ← X - Y)	ADD(X ← Y - Z)
SUB	SUB M	MUL(X ← X × Y)	MUL(X ← Y × Z)
MUL	MUL M	DIV(X ← $\frac{X}{Y}$)	DIV(X ← $\frac{Y}{Z}$)
DIV	DIV M		

Solution:

0 Address	1 Address	2 Address	3 Address
PUSH B	LOAD F	MUL B,C	MUL B,C
PUSH C	MUL E	ADD A,B	ADD X,A,B
MUL	STORE X	MUL E,F	MUL E,F
PUSH A	LOAD D	SUB D,E	SUB D,E
ADD	SUB X	DIV A,D	DIV X,D
PUSH D	STORE X		
PUSH E	LOAD C		
PUSH F	MUL B		
MUL	ADD A		
SUB	DIV X		
DIV			
POP X			

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12.7) Consider a hypothetical computer with an instruction set of only two n-bit instructions. The first bit specifies the opcode, and the remaining bits specify one of the 2n-1 n-bit words of main memory. The two instructions are as follows:

- **SUBS X** = Subtract the contents of location X from the accumulator, and store the result in location X and the accumulator.
- **JUMP X** = Place address X in the program counter.

A word in main memory may contain either an instruction or a binary number in twos complement notation. Demonstrate that this instruction repertoire is reasonably complete by specifying how the following operations can be programmed. Pick any two from a.) to e.).

a) Data transfer: Location X to accumulator, accumulator to location X.

b) Addition: Add contents of location X to accumulator.

c) Conditional branch.

d) Logical OR.

e) I/O Operations.

Solution:

a.) **Data Transfer:** Location X to accumulator, accumulator to location X. Y,Z are used as scratch space left at zero. X is moved to the accumulator using:

1.) subs Z
2.) subs Z
3.) subs X
4.) subs Z
5.) subs Z
6.) subs X

and the accumulator to X using:

1.) subs Z
2.) subs X
3.) subs X
4.) subs Z
5.) subs X
6.) subs Z
7.) subs Z
8.) subs X

b.) **Addition:** Add contents of location X to accumulator. Addition will be equivalent to the negative accumulator minus X.

1.) subs Y
2.) subs Z
3.) subs Z
4.) subs X
5.) subs Y
6.) subs Z
7.) subs Z
8.) subs X
9.) subs Z
10.) subs Z
11.) subs Y

Problem 13

13.1) Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator?

Word 20 contains 40.
Word 30 contains 50.
Word 40 contains 60.
Word 50 contains 70.

a.) LOAD IMMEDIATE 20
b.) LOAD DIRECT 20
c.) LOAD INDIRECT 20
d.) LOAD IMMEDIATE 30
e.) LOAD DIRECT 30
f.) LOAD INDIRECT 30

Solution:

a.) 20
b.) 40
c.) 60
d.) 30
e.) 50
f.) 70

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13.3) An address field in an instruction contains decimal value 14. Where is the corresponding operand located for:

- immediate addressing?
- direct addressing?
- indirect addressing?
- register addressing?
- register indirect addressing?

Solution:

- The address field
- Memory location 14
- The memory location whose address is in the memory location 14
- Register 14
- The memory location whose address is in register 14

13.5) A PC-relative mode branch instruction is 3-bytes long. The address of the instruction, in decimal, is 256028. Determine the branch target address if the signed displacement in the instruction is -31.

Solution:

The next instruction is at $\underline{256031}$ and the branch is $\underline{-31}$, so the next address is $256031 - 31 = \underline{\mathbf{256000}}$.

13.7) How many times does the processor need to refer to memory when it fetches and executes an indirect-address-mode instruction is:

a) A computation requiring a single operand

b) A branch

Solution:

a) Fetch instruction, Fetch effective address, Fetch operand. **3 memory references**

b) Fetch instruction, Fetch effective address and transfer to PC. **2 memory references**

13.11) Consider a processor that includes a base with indexing addressing mode. Suppose an instruction is encountered that employs this addressing mode and specifies a displacement of 1970, in decimal. Currently the base and index register contain the decimal numbers 48,022 and 8, respectively. What is the address of the operand?

Solution:

Base + index + signed displacement $= 48,022 + 8 + 1970 = 50,000_{10} = \underline{\mathbf{0xC350}}$