# CS 219: Homework #5

Due on October 5th, 2016 at 4:00pm

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# Problem 1

**Review Questions**

1.1.) What general categories of functions are specified by computer instructions?
**Answer:** The categories are processor I/O, processor memory, data processing, and c control.

1.2.) List and briefly define the possible states that define an instruction execution?
**Answer:**

- **IAC - Instruction Address Calculation** - Determine the address of the next instruction to be executed
- **IF - Instruction Fetch** - Read instruction from its memory location into the processor.
- **OAC - Operand Address Calculation** - If the operation references an operand stored in memory or one that is available via I/O, then determine its address.
- **OF - Operand Fetch** - Fetch the operand from memory or read it in from I/O.
- **Data Operation** - Perform the operation indicated in the instruction.
- **OS - Operand Store** - Write the result into memory or out to I/O.

1.3.) List and briefly define two approaches to dealing with multiple interrupts?
**Answer:**

- **ISR - Interrupt Service Routines** - Priorities are assigned to each different type of interrupt. ISR's with higher priorities can interrupt lower priority ISR's, resulting in the lower priority ISR being put on the stack until that ISR is completed.
- **Disabling Interrupts** - The processor can ignore specific interrupts and those will remain pending, only to be checked after the processor has enabled interrupts.

1.4.) What types of transfers must a computer's interconnection structure (e.g., bus) support?
**Answer:**

- Memory to processor and processor to memory
- I/O to processor and processor to I/O
- I/O to memory and memory to I/O

1.5.) List and briefly define the QPI protocol layers.
**Answer:**

- **Physical** - Wires that carry signals, circuitry, logic for other features required for transmitting and receiving binary data.
- **Link** - Responsible for flow control and reliable transmission.
- **Routing** Allows for direction of packets.
- **Protocol** - The high-level set of rules for exchanging packets of data between devices.

1.6.) List and briefly define the PCIe protocol layers.
**Answer:**

- **Physical** - Wires that carry signals, circuitry, logic for other features required for transmitting and receiving binary data.
- **Link** - Responsible for flow control and reliable transmission.
- **Transmission** - Generates and consumes data packets that are then used to implement load/store data transfer systems. Also handles flow control of the packets between various components on a link.

# Problem 2

2.1) The hypothetical machine of Figure 3.4 in the book also has two I/O instructions:

- 0011 = load AC from I/O
- 0111 = store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5
2. Add contents of memory location 940.
3. Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

**Answer:**

| Address | Memory |
|---|---|
| 300 | 3 0 0 5 |
| 301 | 5 9 4 0 |
| 302 | 7 0 0 6 |
| ... | ... |
| 940 | 0 0 0 2 |

The memory contains 300: 3005, 301: 5940, and 302:7006. This means the program instructions will have to do the following steps:

1. $3005 \rightarrow IR$
2. $3 \rightarrow AC$
3. $5940 \rightarrow IR$
4. $3 + 2 = 5 \rightarrow AC$
5. $7006 \rightarrow IR$
6. $AC \rightarrow Device\ 6$

Problem 2 continued on next page...

2.2) A combinational circuit is used to control a seven-segment display or decimal digits, as shown in Figure 11.35 in the book. The circuit has four inputs, which provide the four-bit code used in packed decimal representation ($0_10 = 000$, ... , $9_10 = 10001$). The seven outputs define which segments will be activated to display a given decimal digit. Note that some combinations of inputs and outputs are not needed.

a.) Develop a truth table for this circuit.

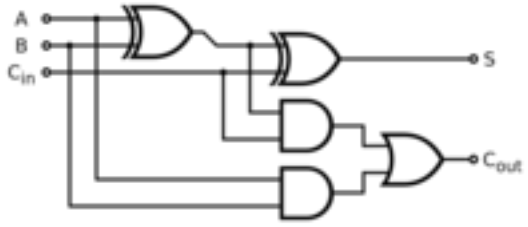
b.) Express the truth table in SOP form.

c.) Express the truth table in POS Form.

**Answer:**

N/A

2.3) Implement the full adder of Figure 11.20 with just five gates. (Hint: Some of the gates are XOR gates.)
**Answer:** From wikipedia:




2.4) Consider Figure 11.20 from the book. Assume that each gate produces a delay of 10 ns. Thus, the sum output is valid after 20 ns and the carry output after 20 ns. What is the total add time for a 32-bit adder

a.) Implemented without carry lookahead, as in Figure 11.19 in the book.

b.) Implemented with carry lookahead using 8-bit adders, as in Figure 11.21 from the book.

**Answer:**

N/A