LAB 4

Sampler Error Modeling and Correction

1. **First order model of a ZOH sampling circuit**
   Construct a model for a sampling circuit shown in Fig. 1.

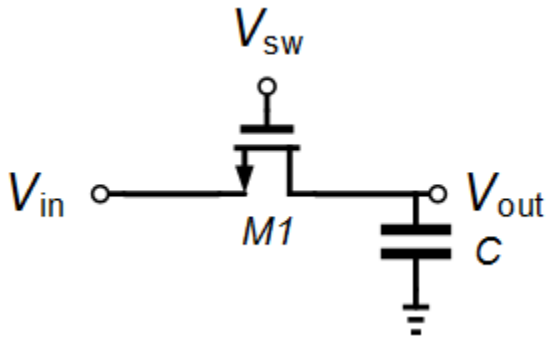

Figure 1: Sampling Circuit

When the NMOS switch M1 is ON (*V*sw = 1), the sampling circuit behaves as a series RC circuit and the input *V*in is sampled on the capacitor. When the switch turns OFF (*V*sw = 0), the voltage on the capacitor is held constant until the beginning of the next sampling phase. If the ON resistance of the switch is R, then the time constant of the sampler, τ, is R*C.

a. For an input sinusoidal signal of frequency 1 GHz, a sampling frequency of 10 GHz and time constant of 10 ps, plot the output of the sampling circuit.

2. **Sampling Error**
   Sampling error is the difference between an ideally sampled signal (delta train) and a signal sampled with a finite time constant sampling circuit.

   a. Assume a NRZ (Non Return to Zero) input of amplitude 0.5 V and data rate of 10 Gb/s. Sample the input signal once in the middle of every bit period. Assuming a 50% duty cycle for *V*sw in Fig. 1, what should the time constant be for the maximum sampling error to be less than 1 LSB for a 7-bit ADC with a full scale range of 1 V. Justify with an equation the obtained time constant value.

   b. Assume a multi-tone signal input with frequencies of 0.2 GHz, 0.58 GHz, 1 GHz, 1.7 GHz and 2.4 GHz and a sampling frequency of 10 GHz. What should the time constant be for the sampling error to be less than 1 LSB for a 7-bit ADC? Is it different from the time constant in 2.a? Why?

3. **Sampling Error Estimation**
   Construct an ADC model by adding an N-bit quantizer (N=7) at the output of the sampling circuit.

   a. Let the input to the ADC be the multitone signal generated in 2.b. At the ADC output, find the error, *E*, between the quantized signal sampled with a sampling circuit having the time constant derived 2.a and an ideally sampled signal. What is the variance of *E*? What is ratio of the variance of *E* to the variance of the uniform quantization noise?

   b. In this model, the ADC output at time instant *i* has both a sampling error and a quantization error. Using **least squares estimation**, construct an M-tap FIR filter that estimates the sampling error at the ADC output using M-1 previous ADC output values. Add the estimated error to the ADC output and compute the error signal, *E*, defined in 3.a. Plot the ratio of the variance of *E* to the variance of uniform quantization noise as M is varied from 2 to 10. What do you infer from this plot?

4. **Calibration of Errors in a Two-Channel TI-ADC**
   a. Construct a simulation of a 2-way TI-ADC that includes time, offset and bandwidth mismatches between the channels. Provide SNDR plots following the setup in 2(a) for the design of the input signal.
   b. Construct a calibration technique capable of compensating the time, offset and bandwidth mismatches between the channels following the techniques described in the references.

References

T.-H. Tsai, P. J. Hurst, and S. H. Lewis, "Bandwidth Mismatch and Its Correction in Time-Interleaved Analog-to-Digital Converters," IEEE Transactions on Circuits and Systems II, pp. 1133-1137, Oct., 2006.

N. Sitthimahachaikul, L. P. Rao, and P. J. Hurst, "Canceling the ISI Due to Finite S/H Bandwidth in a Circular Buffer Forward Equalizer", IEEE Transactions On Circuits And Systems—II: Express Briefs, Vol. 59, No. 3, March 2012

S. M. Jamal, D. Fu, M. P. Singh, P. J. Hurst, and S. H. Lewis, "Calibration of Sample-Time Error in a Two-Channel Time-Interleaved Analog-to-Digital Converter," IEEE Transactions on Circuits and Systems I, pp. 130-139, Jan., 2004

D. Fu, K. Dyer, S. Lewis, and P. Hurst, "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," IEEE Journal of Solid-State Circuits, pp. 1904-1911, Dec., 1998