(1) •	Msgs																
/ucat_tb/reset_TB	1																
/ucat_tb/clock_TB	1																
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S FETCH	1	S FETCH	2	S DECODE	0	S LDA IM	4 O	S LDA IM	M 1	S LDA IM	М 2	SF	TCH	0
I - /ucat_tb/port_out_00_TB	00	00															
→ /ucat_tb/port_out_01_TB	00	00															
→ /ucat_tb/port_out_06_TB	00	00															
+- /ucat_tb/port_out_07_TB	00	00															
→ /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	86	00					86										
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	01	00									01						
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	02	00			01								02				
I → /ucat_tb/DUT1/cpu_component/processing/reg_A/data	AA	00													AA		
I → /ucat_tb/DUT1/cpu_component/processing/reg_B/data	00	00															
	00	00															
			1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	#		
Now	2200000 ps	os			4000	0 ps			8000	0 ps			1200	00 ps			
© ✓ © Cursor 1	133845 ps														1338	45 ps	

Figure 1: Fetch-Decode States and LDA_IMM Execution

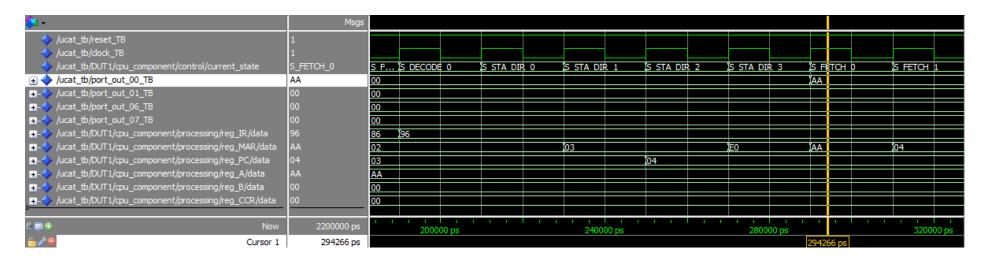


Figure 2: STA_DIR Execution

∳ 1 v	Msgs																
/ucat_tb/reset_TB	1																
/ucat_tb/clock_TB	1																
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S DECODE	0	S LDA DIF	₹ 0	S LDA DIF	1 1	S LDA DIF	₹ 2	S LDA DI	R 3	S LDA DIF	R 4	S F	TCH	0
	AA	AA															
+> /ucat_tb/port_out_01_TB	CC	CC															
→ /ucat_tb/port_out_06_TB	00	00															
→ /ucat_tb/port_out_07_TB	00	00															
/ucat_tb/DUT1/cpu_component/processing/reg_IR/data	87	96	87														
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	F1	08					09				F1						
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	0A	09							0A								
→ /ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	CC													11		
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_B/data	00	00															
+- /ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	00	00															
																	
[™] 🛒 💿 Now	2200000 ps	00 ps			6800	00 ps			72000	00 ps			7600	00 ps			
© ► Cursor 1	774117 ps														7741	17 ps	

Figure 3: LDA_DIR Execution

≨i •	Msgs														
/ucat_tb/reset_TB	1														
/ucat_tb/clock_TB	1														
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S DECODE	0	S LDB IM	M 0	S LDB IM	И 1	S LDB IM	12 S	FETCH	0	S FETCH	1	S FETCH 2
	AA	AA													
	CC	CC													
	11	11													
+ /ucat_tb/port_out_07_TB	00	00													
/ /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	88	96	88												
/ /ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	0D	0C					OD						0E		
	0E	0D							OE.						OF
	11	11													
→ /ucat_tb/DUT1/cpu_component/processing/reg_B/data	DD	00)D	D				
	00	00													
<u></u>			<u> </u>						<u> </u>			+	<u> </u>		
△ 💀 🕞 Now	2200000 ps		10000	000 ps			10400	000 ps			1080	0000 ps			1120000 ps
€ 1 Cursor 1	1074222 ps		1074222 ps												

Figure 4: LDB_IMM Execution

(1) →	Msgs																
<pre>// /ucat_tb/reset_TB</pre>	1												T				
/ucat_tb/dock_TB	1												1				
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	s	S DECODE	0	s stb dir	0	S STB DIF	1	s stb dif	2	s stb dif	3	FET	сн о)	S FETCH	1
→ /ucat_tb/port_out_00_TB	AA	AA															
+> /ucat_tb/port_out_01_TB	CC	CC															
+> /ucat_tb/port_out_06_TB	11	11															
→ /ucat_tb/port_out_07_TB	DD	00)	DD				
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	97	88	97														
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	BA	0E					0F				E7)	3A			10	
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_PC/data	10	0F							10								
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	11															
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_B/data		DD															
+- /ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	00	00															
		-							<u> </u>					_			
△ 🛒 ⊙ Now	2200000 ps		1160000 ps 1200000 ps									1	1240000 ps				
© ✓ ⊖ Cursor 1	1233520 ps	1233520 ps															

Figure 5: STB_DIR Execution

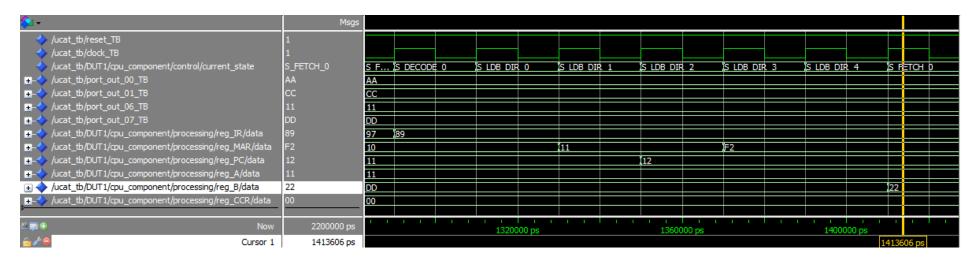


Figure 6: LDB_DIR Execution

≨ iv	Msgs														
/ucat_tb/reset_TB	1								i						
/ucat_tb/clock_TB	1								1						
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S DECODE	0	S BEQ 0		S BEQ 1	S	FETCH	0	S FETCH	1	S FETCH :	2	S DECODE 0
	AA	AA													
→ /ucat_tb/port_out_01_TB	CC	CC													
→ /ucat_tb/port_out_06_TB	11	11													
+- /vcat_tb/port_out_07_TB	22	22													
/ucat_tb/DUT1/cpu_component/processing/reg_IR/data	21	97	21												86
II → /ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	15	14					15				16				
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_PC/data	16	15						16					17		
<u>+</u> → /ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	11													
	22	22							ļ						
	00	00													
Now	2200000 ps	1 1	16400	000 ps	1 1	1 1	16800	00 ps	1	1 1	17200	00 ps	1 1	1 1	1760000 ps
© Cursor 1	1694197 ps		1694197 ps												

Figure 7: BEQ Execution

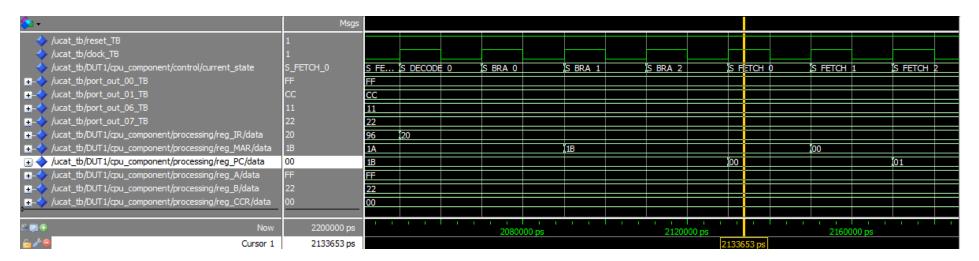


Figure 8: BRA Execution