<b>(1)</b> •	Msgs																
/ucat_tb/reset_TB	1																
/ucat_tb/clock_TB	1																
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S FETCH	1	S FETCH	2	S DECODE	0	S LDA IM	4 O	S LDA IM	М 1	S LDA IM	М 2	SF	TCH	0
<b>I</b> - /ucat_tb/port_out_00_TB	00	00															
→ /ucat_tb/port_out_01_TB	00	00															
→ /ucat_tb/port_out_06_TB	00	00															
+- /ucat_tb/port_out_07_TB	00	00															
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	86	00					86										
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	01	00									01						
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	02	00			01								02				
<b>I</b> → /ucat_tb/DUT1/cpu_component/processing/reg_A/data	AA	00													AA		
<b>I</b> → /ucat_tb/DUT1/cpu_component/processing/reg_B/data	00	00															
	00	00															
		1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	弄		
Now	2200000 ps	os			4000	0 ps			8000	0 ps			1200	00 ps			
© ✓ © Cursor 1	133845 ps														13384	45 ps	

Figure 1: Fetch-Decode States and LDA\_IMM Execution

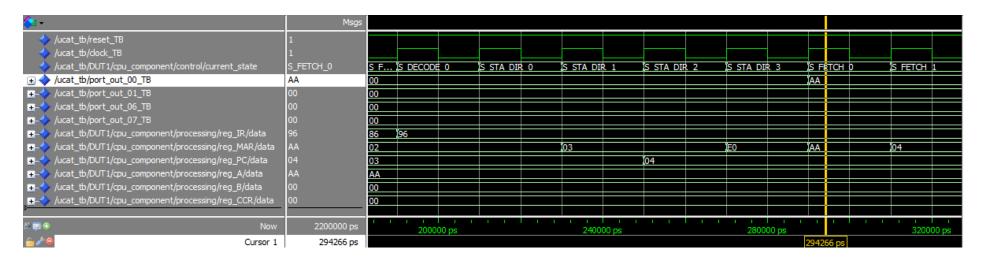


Figure 2: STA\_DIR Execution

<b>(1)</b> ▼	Msgs															
<pre>// /ucat_tb/reset_TB</pre>	1															
/ucat_tb/dock_TB	1														_	
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S DECODE	0	S LDA DIF	0 9	S LDA DI	R 1	S LDA DI	₹ 2	S LDA DI	₹ 3	S LDA DI	R 4	S FET	CH 0
	AA	AA														
+> /ucat_tb/port_out_01_TB	CC	CC														
/ucat_tb/port_out_06_TB	00	00														
→ /ucat_tb/port_out_07_TB	00	00														
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	87	96	87													
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	F1	08					09				F1					
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	0A	09							0A							
→ /ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	CC													11	
	00	00														
+- / /ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	00	00														
		1 1	1 1	1 1	1 1	1 1	<u> </u>	1 1	1 1	1 1	<u> </u>	1 1	<del></del>	1 1		
Now	2200000 ps	00 ps			6800	00 ps			7200	00 ps			7600	00 ps		
6 ≠ 6 Cursor 1	774117 ps														774117	7 ps

Figure 3: LDA\_DIR Execution

<b>≨i</b> +	Msgs														
/ucat_tb/reset_TB	1														
/ucat_tb/clock_TB	1														
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	S DECODE	0	S LDB IM	И О	S LDB IM	И 1	S LDB IM	И2 S	FETCH	0	S FETCH	1	S FETCH 2
+ /ucat_tb/port_out_00_TB	AA	AA													
+ /ucat_tb/port_out_01_TB	CC	CC													
+ /ucat_tb/port_out_06_TB	11	11													
+- /ucat_tb/port_out_07_TB	00	00													
	88	96	88												
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	0D	0C					OD						0E		
/ /ucat_tb/DUT1/cpu_component/processing/reg_PC/data	0E	0D							0E						0F
	11	11													
	DD	00								<u> </u>	D				
/ /ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	00	00													
Now	2200000 ps		10000	00 ps			10400	000 ps			108	0000 ps			1120000 ps
© Lursor 1	1074222 ps									10	74222 p	s			

Figure 4: LDB\_IMM Execution

<b>ૄ</b>	Msgs															
/ucat_tb/reset_TB	1															
/ucat_tb/clock_TB	1															
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	s	S DECODE	0	s stb dir	0	S STB DIF	1	s stb dif	2	S STB DIF	1 3	S FET	CH D	S FETCH	1
+- /ucat_tb/port_out_00_TB	AA	AA														
	CC	CC														
→ /ucat_tb/port_out_06_TB	11	11														
→ /ucat_tb/port_out_07_TB	DD	00											DD			
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	97	88	97													
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	BA	0E					OF				E7		BA		10	
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	10	0F							10							
/ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	11														
<b>I</b> → /ucat_tb/DUT1/cpu_component/processing/reg_B/data	DD	DD														
	00	00														
			1 1								<del></del>					
Now	2200000 ps				11600	00 ps			12000	00 ps			12	240000 ps		
© / © Cursor 1	1233520 ps											13	233520	ps		

Figure 5: STB\_DIR Execution

<b>≨i</b> •	Msgs																
/ucat_tb/reset_TB	1														Ħ		
/ucat_tb/clock_TB	1														ļΠ		
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S F	S DECODE	0	S LDB DIR	. 0	S LDB DI	R 1	S LDB DIF	. 2	S LDB DIF	3	S LDB DIF	<b>1</b> 4	S F	TCH 0	
	AA	AA													П		
	CC	CC													П		
	11	11													Ħ		
	DD	DD															
/ucat_tb/DUT1/cpu_component/processing/reg_IR/data	89	97	89														
/ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	F2	10					11				F2						
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	12	11							12								
/ucat_tb/DUT1/cpu_component/processing/reg_A/data	11	11															
	22	DD													22		
	00	00															
			<u> </u>						<u> </u>		<u> </u>		<u> </u>		-		=
Now	2200000 ps				13200	00 ps			13600	00 ps			14000	00 ps			
© Lursor 1	1413606 ps													1	41360	6 ps	

Figure 6: LDB\_DIR Execution

<b>(</b> 1) ▼	Msgs																		
<pre>// /ucat_tb/reset_TB</pre>	1																		
/ucat_tb/clock_TB	1																		
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FE	S DECODE	0	S BRA 0		S BRA 1		S BRA 2	s	FETCH	0	S FETCH	1	S FETCH :	2			
/> /ucat_tb/port_out_00_TB	FF	FF									1								
/> /ucat_tb/port_out_01_TB	CC	CC									1								
	11	11																	
+> /ucat_tb/port_out_07_TB	22	22																	
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	20	96	20																
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	1B	1A					1B						00						
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_PC/data	00	1B								(0)	)				01				
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_A/data	FF	FF																	
<u>→</u> /ucat_tb/DUT1/cpu_component/processing/reg_B/data	22	22																	
+- /vcat_tb/DUT1/cpu_component/processing/reg_CCR/data	00	00																	
△ ■ • Now	2200000 ps				20800			21600	00 ps										
© ✓ ⊖ Cursor 1	2133653 ps	2133653 ps											53 ps						

Figure 7: BRA Execution

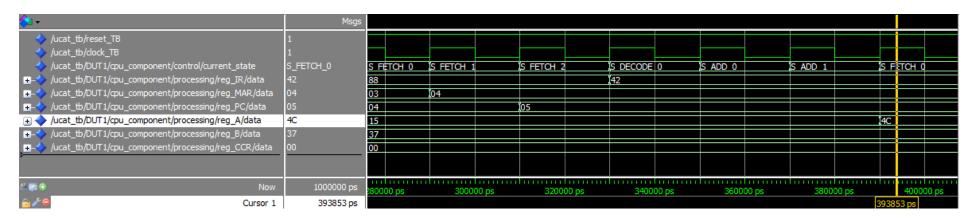


Figure 8: ADD\_AB Execution

<b>€</b> 1 •	Msgs															
/ucat_tb/reset_TB	1															
/ucat_tb/clock_TB	1															
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FET	CH 1	S FETCH 2		S DECODE	0	S SUB 0		S SUB 1		S F	TCH 0		S FETCH 1	
/ /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	43	88				43										
/ /ucat_tb/DUT1/cpu_component/processing/reg_MAR/data	04	04													05	
/ucat_tb/DUT1/cpu_component/processing/reg_PC/data	05	04		05												
→ /ucat_tb/DUT1/cpu_component/processing/reg_A/data	DE	15										DE				
<u>I</u> → /ucat_tb/DUT1/cpu_component/processing/reg_B/data	37	37														
/ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	09	00										09				
 △ ■ ● Now	1000000 ps											1111	11111			11111
		30000	)0 ps	32000	00 ps	34000	00 ps	3600	00 ps	3800	00 ps		40000	00 ps	42000	)0 ps
©   Cursor 1	393853 ps										3	3938	53 ps			

Figure 9: SUB\_AB Execution

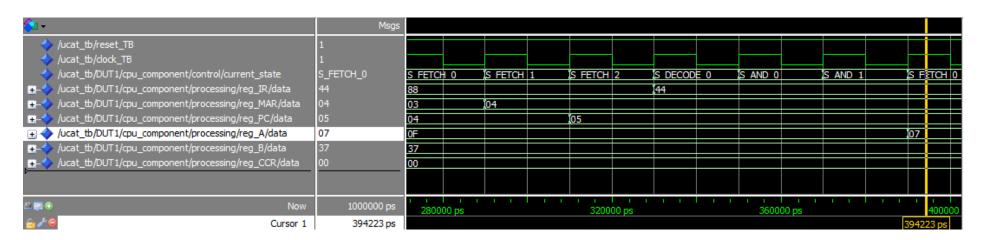


Figure 10: AND\_AB Execution

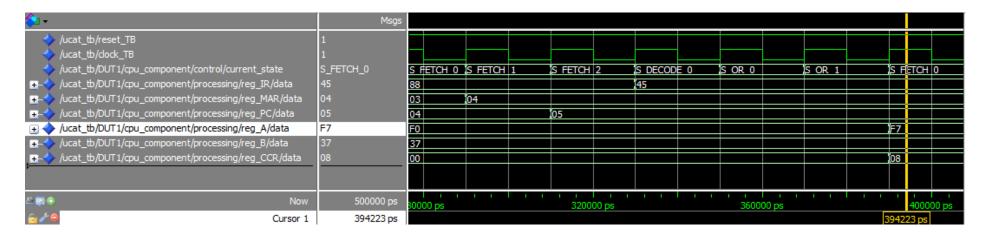


Figure 11: OR\_AB Execution

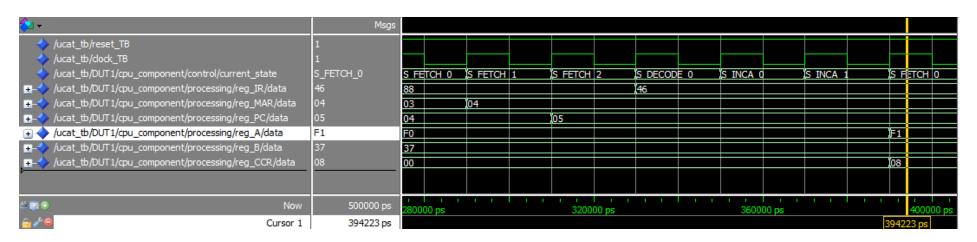


Figure 12: INCA Execution

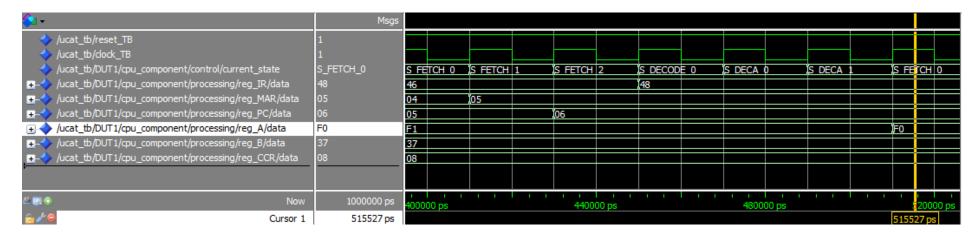


Figure 13: DECA Execution

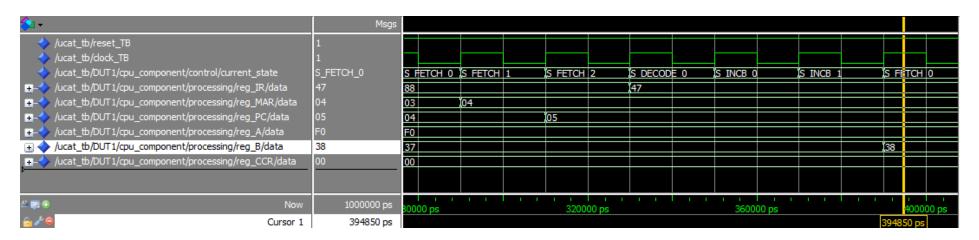


Figure 14: INCB Execution

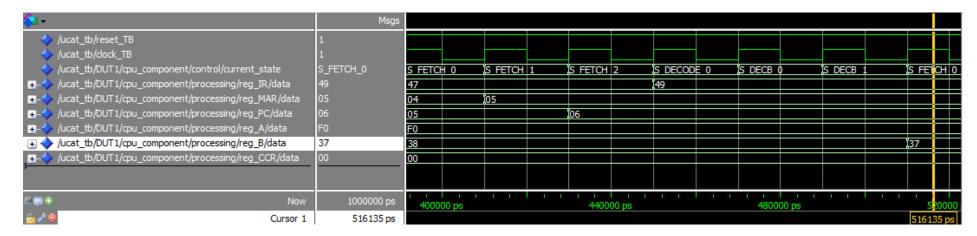


Figure 15: DECB Execution

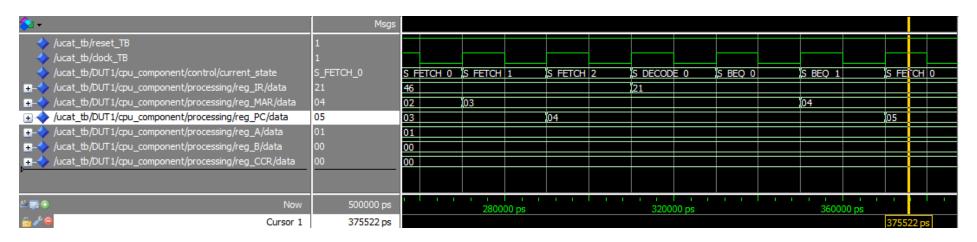


Figure 16: BEQ Execution 1

<b>(</b> 1) ▼	Msgs														
/ucat_tb/reset_TB	1														
/ucat_tb/clock_TB	1														
/ucat_tb/DUT1/cpu_component/control/current_state	S_FETCH_0	S FETCH 1	S FETCH	2	S DECOD	E 0	S BEQ 0		S BEQ 1		S BEQ 2		S FE	TCH 0	
/ /ucat_tb/DUT1/cpu_component/processing/reg_IR/data	21	48			21										
————————————————————————————————————	04	03							04						
→ /ucat_tb/DUT1/cpu_component/processing/reg_PC/data	00	03	04								05		00		
/ /ucat_tb/DUT1/cpu_component/processing/reg_A/data	00	00													
	00	00													
/ucat_tb/DUT1/cpu_component/processing/reg_CCR/data	04	04													
N == 4		1 1	1 1 1	1 1	<del>                                     </del>	1 1	1 1	1 1	1 1	1 1	1 1	1 1	_		╗
Now	500000 ps	280000 ps			3200	00 ps			3600	00 ps				100000 p	os
© Lursor 1	394847 ps												3948	17 ps	

Figure 17: BEQ Execution 2