EELE 466 Class Project

Task #4 Assignment

Due Wed May 6, 2015

You now need to take all the VHDL code that was generated from all the Matlab functions found in *Madgwick_segments.m* and create a top level VHDL file that implements the entire Madgwick Matlab code in VHDL.

```
function [q0, q1, q2, q3] = Madgwick_segments(q0, q1, q2, q3, gx, gy, gz, ax, ay, az, mx, my, mz)
```

You also need to verify this code using the Matlab HDL Verification Toolbox and compare it to the output of the original Matlab Madgwick code. This will be similar to what you did for lab 3.

Task #4 Deliverables

Upload to D2L the following files:

1. All the VHDL code necessary to implement your overall Madgwick function.
2. **A final report** that includes the following:
    a. The FPGA resources required for all the VHDL code.
    b. The maximum frequency that the design can run as reported by the timing report (targeting the Cyclone II on the DE2 board in the lab).
    c. Your test and verification results.