**Matthew L. Liu**

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**Objective**

Third year Computer Engineer Student at Georgia Tech with industry experience in hardware engineering specializing in pre-silicon validation within an SoC. Adaptable, resourceful, and adept at working in focused and collaborative environments, debugging problems during testing, and creating or finding solutions. Successful in climate research and other multi-disciplinary internships. Actively looking for hardware design engineering internships and co-ops Spring and Summer 2020.

**Education**

**Georgia Institute of Technology | Atlanta, GA** *January 2017 – Present*

Bachelor of Science in Computer Engineering, GPA 3.3 Expected Graduation, May 2021

* Faculty Honors and Dean’s List (all semesters except Fall 2018)

**Skills**

**Programming:** System Verilog, Verilog, VHDL, OVM/UVM, C,C++, Java, MATLAB, MIPS Assembly, VPython, Python, Perl, HTML/CSS/JS, GrADs script, Fortran, Linux, Unix, MacOS X

**Operating Systems:** Linux, Unix, MacOS X, FreeBSD, Windows 10

**Hardware:** Raspberry Pi, ARM mbed microcontroller, FPGAs, oscilloscope, logic analyzer, logic probe, digital multimeter, function generator, FPGA, BeagleBoard, digital and analog circuit design, PLD, TTL devices

**Software and Project Development Environments:** Vim, Synopsys’ Verdi (for interactive debug), Git, Altera Quartus II, NI LabVIEW, GitHub, Microsoft Office Suite, Twitter API, Google API, Final Cut Pro, Adobe Photoshop, FL Studio

**Professional Organizations:** IEEE, Phi Sigma Pi (national honor fraternity)

**Communication:** Project and Conference Presentations, Research Posters, Design proposals, technical reports

**Languages:** English (fluent), Chinese (intermediate), Spanish (beginner)

**Work Experience**

**Intel | Fort Collins, CO** *May – August 2019*

***10nm Power Management Validation Intern***

* Contributed to development of new BFM within pre-silicon validation environment for modeling power management firmware responses by improving code modularity and resuse and minimized reliance on firmware to validate RTL
* For supported regression tests, the BFM reduces CPU model time by 27% and total cycles by 75%, enabling more efficient, more reliable, and timelier validation

**CIRA, NOAA Research Lab at CSU | Fort Collins, CO; Kunming, China** *May 2016 – August 2018*

***Climate Researcher and Research Assistant***

*CIRA is a nexus for multi-disciplinary cooperation between atmospheric and NOAA research scientists*

* Gathered NOAA weather station data, parsed and analyzed the data (CSV files), with Fortran models, MATLAB, and GrADs (atmospheric science visual data analysis tool) and presented at Third Pole Environmental Conference
* Worked with senior research scientist, Dr. Glen Liston to perform data analysis and modeling on regional conditional variations specifically within the Rocky Mountains, Alaska, and Greenland Ice sheets

**JDL International, Inc. | Fort Collins, CO; Munich, Germany; Jiangxi, China** *May 2018 – January 2019*

***Intern***

*Waste water treatment company that develops and designs modular, on-site bioreactor technology to treat contaminated water. The company works with public and private organizations, like the UN, whom are concerned with environmental protection*

* Contributed in a variety of different IT, engineering, and marketing roles
* Improved, fixed, and identified bugs on company website
* Procured and conducted data analysis of water quality before and after FMBR treatment
* Participated and observed an on-site installation of equipment
* Attended trade shows, conferences, and onsite trainings on environmental protection

**Projects**

**FPGA Controlled Autonomous “Wall Following Bot”** *Spring 2019*

***HW and SW Programmer, ECE Department, ECE2031***

*Collective effort of four computer engineering and science majors*

* Developed an algorithm for wall following with a team of four computer engineering students by programming a DE2 board modified amigo bot (used Intel Quartus CAD tool for design)
* Partially programmed the simple programmable computer (used by the amigobot) onto a FPGA with a processor, memory, and IO bus for interfacing with peripheral devices

**Arm Mbed Role-Playing Game** *December 2018*

***HW Design and Programmer, ECE Department, ECE2035***

* Independently developed a RPG, quest-based game using Mbed hardware.
* Constructed a gaming circuit, coded in C, hash table data structure, OOP, interface between hardware and software
* Demo: <https://www.youtube.com/watch?v=Wtsbtr2bRxA>

**Minesweeper Computer Generated Solution** *December 2018*

***SW Programmer, ECE Department, ECE2035***

* Developed a computer-generated solution to the Minesweeper game using square inferencing techniques coded in both C and MIPS assembly language. Seeding the program generates different a random map for itself to solve.
* Optimized memory, and reduced static and dynamic instructions

**Python Physics Simulations** *Spring and Fall 2018*

***SW Programmer, Physics Department, PHYS2211/2212***

* Modeled electro-magnetic fields, charged objects, electrons, spaceship trajectories, 3D motion, springs, etc.

**Finite State Machines** *April 2017*

***Circuit Designer, ECE Department, ECE2020***

* Using NI myDAQ instruments, breadboard/protoboard, decoders, inverters, flip-flops, etc. to create state transition diagrams and truth tables for engineering synchronous clocked finite state machine.

**Twitter API Sentiment Analysis** *Summer 2016*

***Programmer, Independent Project***

* Conducted sentiment analysis on Tweets with Python (made inferences from diction and semantics) + open source code

**Relevant Coursework at ECE Georgia Tech by Spring 2020**

**Hardware and Software Programming:** Instruction set architecture datapath and controller, memory (stack, heap, static), data abstractions (structs, arrays, linked lists, hash tables), File I/O, Embedded software, basic concurrency in multicore systems, assembly level programming, procedural abstraction (function calls, activation frames, etc.)

**Digital Design Laboratory:** implement simple computer within a PLD, VHDL (design, implement, simulate circuits), design with graphical CAD tools, machine language and assembly language programs for simple computer, FPGAs, HDL based simulation and synthesis with FPGAs, oscilloscope, logic analyzer, timing simulation, state machine implementation, design verification with logic analyzer, combinational design using primitive gates, schematic capture, and VHDL

**Circuit Analysis:** Voltage, Current, Power, Energy, Kirchoff, linearity, superposition, Thevenin, Norton, Op Amps, first and second order circuits, RLC circuits, forcing functions, sinusoidal steady-state analysis, resonance, phasors, impedance, power analysis (instantaneous and average power, complex power, max power transfer)

**Signal Processing:** Phasors, sinusoids, harmonics, spectrogram analysis, Fourier series synthesis and analysis, aliasing, folding, continuous vs discrete time domains, convolution, filters (low, high, bandpass), DFT, Z-transform for FIR, MATLAB, Image enhancement, Time frequency analysis, sound and music synthesis, sample reconstruction

**Math Foundations for Computer Engineering:** discrete math, proofs, computational complexity, Fast Fourier transform, error detection and correction codes (parity coding), data abstractions, graph theory (trees, lists, Prim’s, Dykstra’s algorithms, etc.), regular expressions, state minimization, algorithms (searching, sorting, closest path, recursion etc.)

**Physical Foundations for Computer Engineering:** Physical Implementation of a bit (barrier model), physics of CMOS based computation (semiconductor physics, MOSFET and device physics, switches as computing devices), physics of data communication via propagation through wire, alternative computing models (quantum computing)

**Computer Architecture, Systems, Concurrency and Energy in Computation:** instruction set architecture (mutli-cycle data path and control, controller implementation), CPU pipeline (hazards and solutions, branch prediction), Memory Systems (caches, main memory, virtual memory basics, OS level algorithms), Concurrency (threads, ILP, DLP, TLP), Energy and Power dissipation (microarchitecture-level, power virus, kernel benchmarks), I/O architecture and operating system support, CPU scheduling

**Leadership, Volunteering, and Activities**

**Clubs, Georgia Institute of Technology** *2017 – present*

**•** Phi Sigma Pi, Piano Club, Chess Club, Student Alumni Association, Navigators

**Family Leadership Training Institute** *2016 – 2017*

**Concert Pianist** *2006 – present*

• International Keyboard Odyssiad and Festival (silver medalist), symphonic, tower, and chamber orchestra

**Activities:** Basketball, Volleyball, Swimming, Tennis, Track