

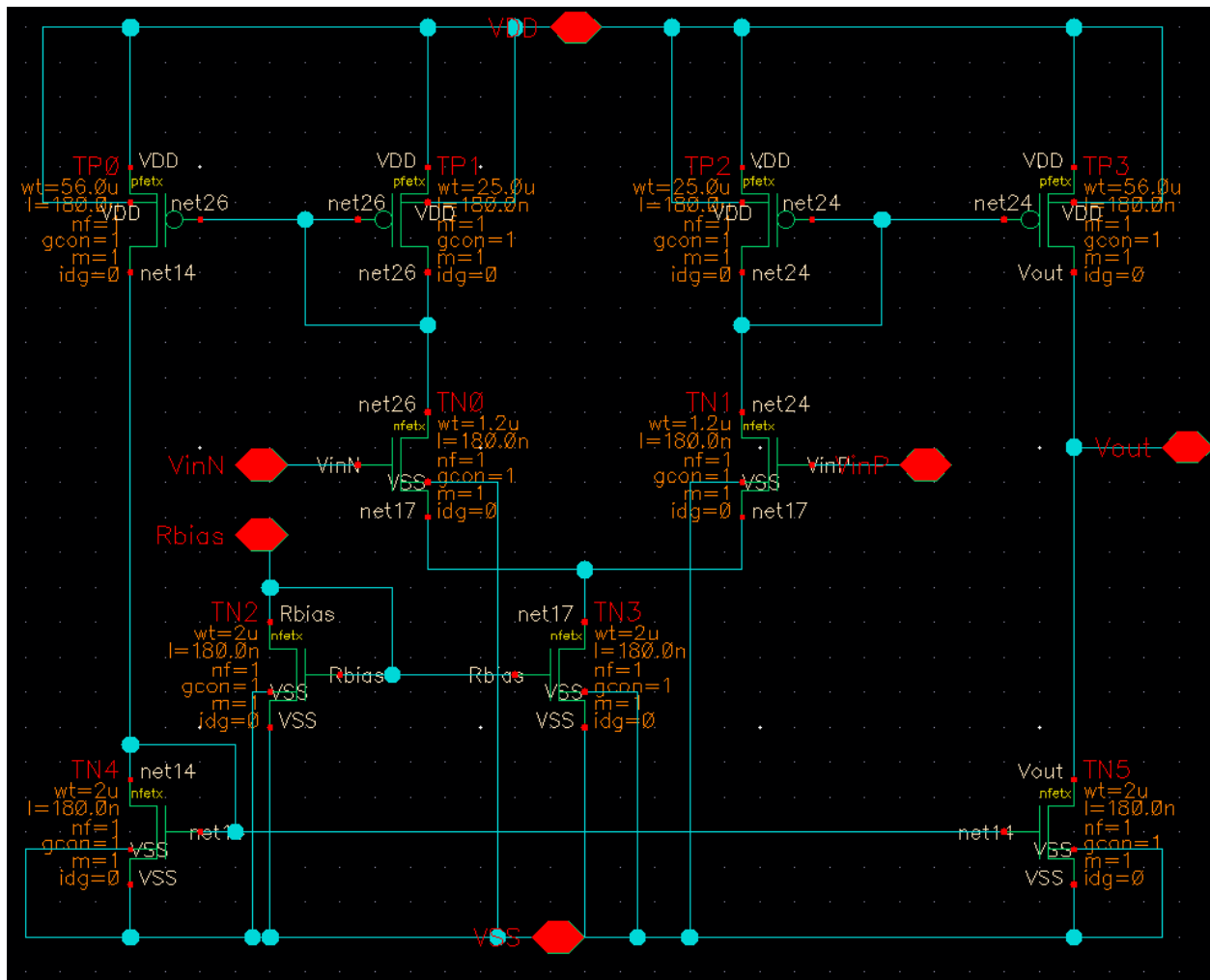
Matthew Loden

ECEN 474

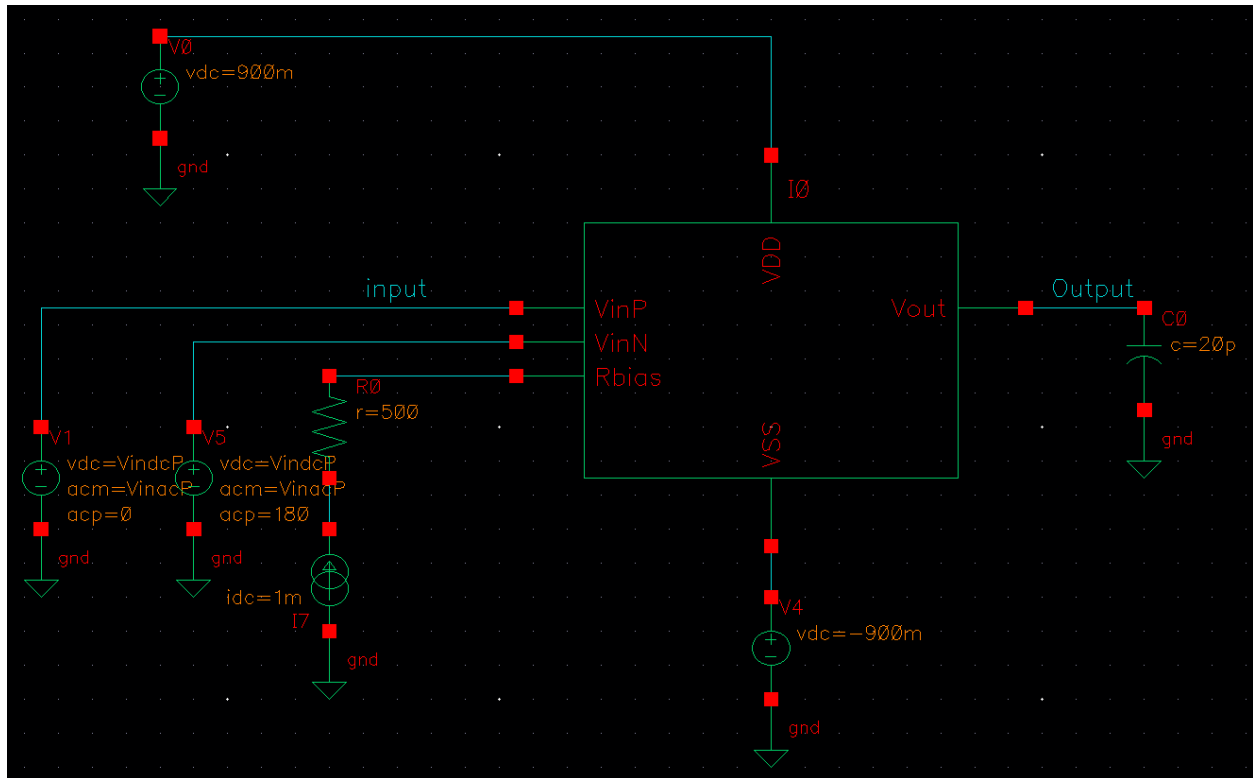
Lab 08 – Operational Transconductance Amplifier

Schematic and Pre-lab Simulations:

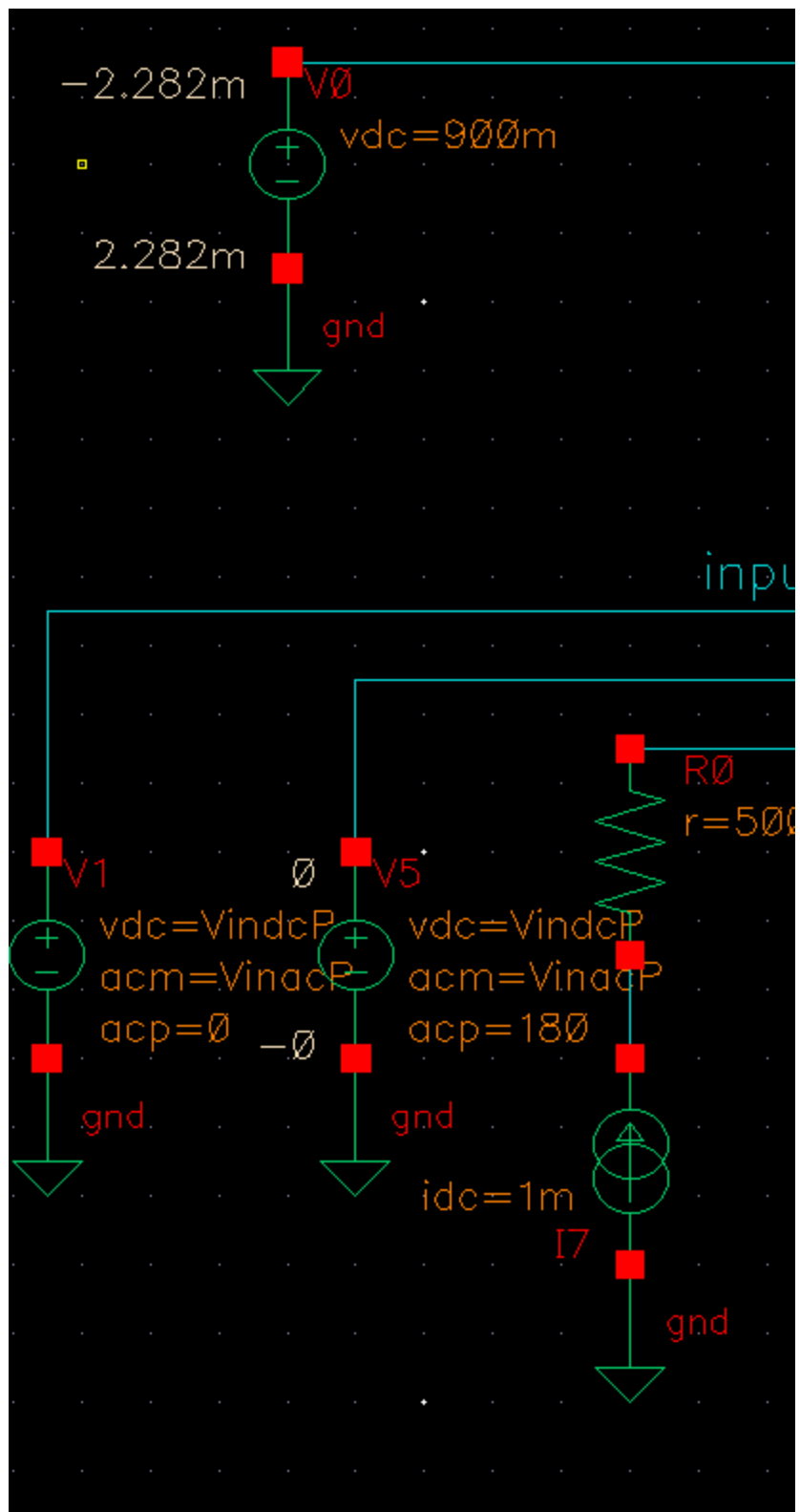
Schematic:



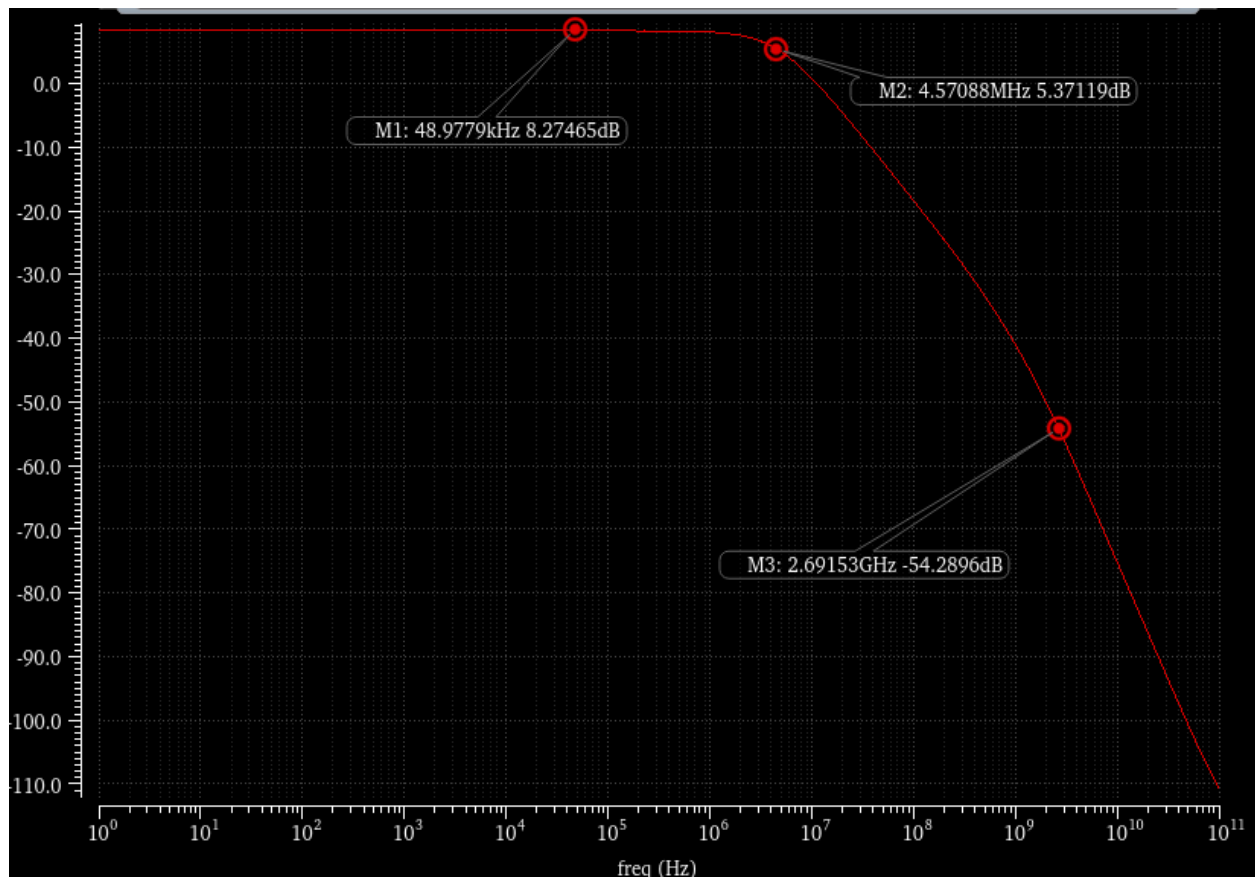
Test Bench:



Power Draw from Voltage Sources Not Including Current Source:

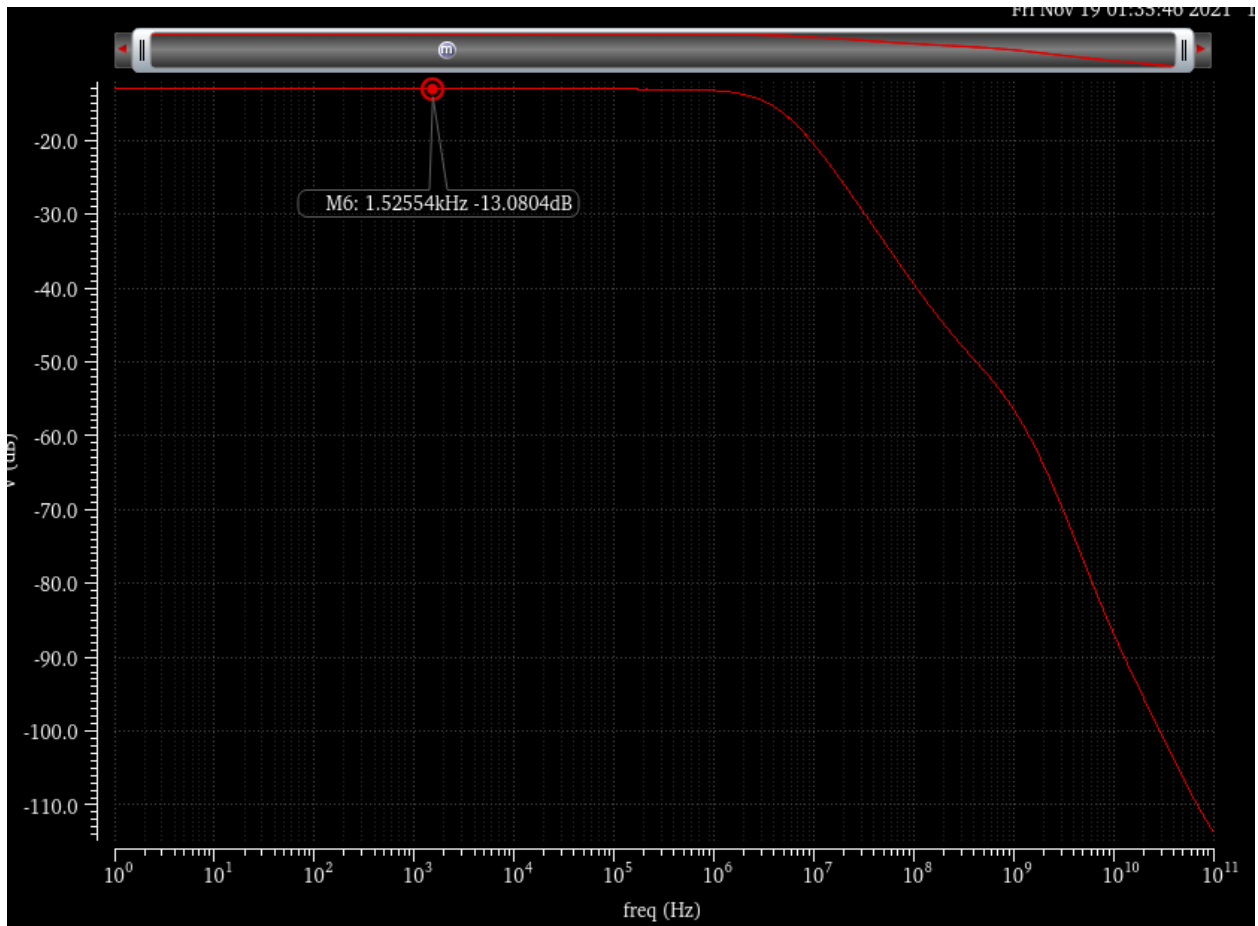


$$\text{Power} = (2.282-1)mA * 1.8v = 2.307mW$$

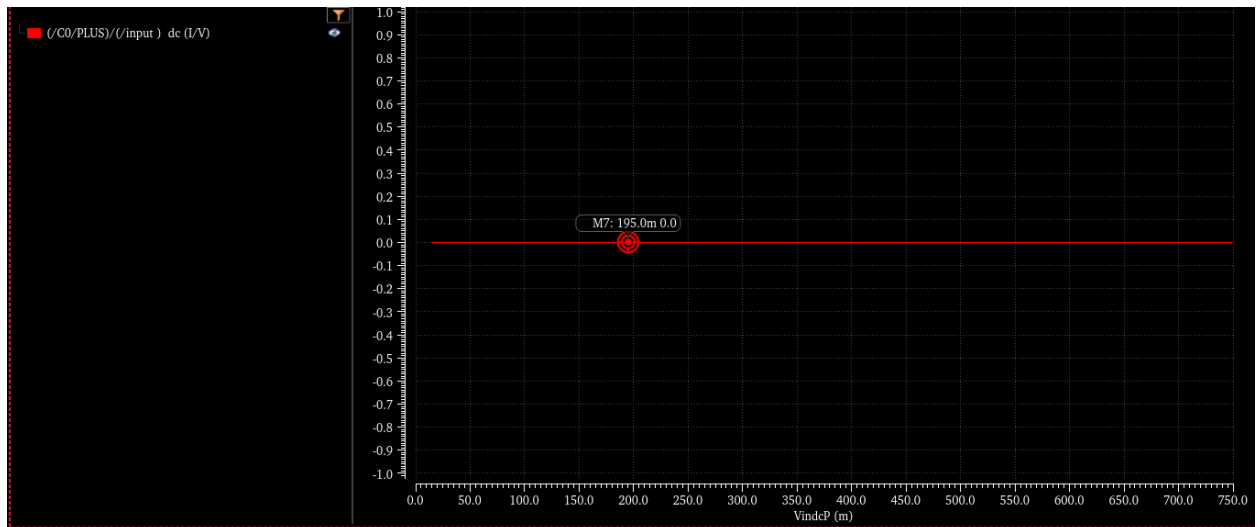


$A_{dm} = 8.27\text{dB}$, Dominant Pole = 4.57MHz , Phase margin ensured > 60 due to second pole occurring at 2.69GHz which is much larger than three times the pole one frequency.

$$GBW = A_{dm} * P1 = 11.84\text{MHz}$$

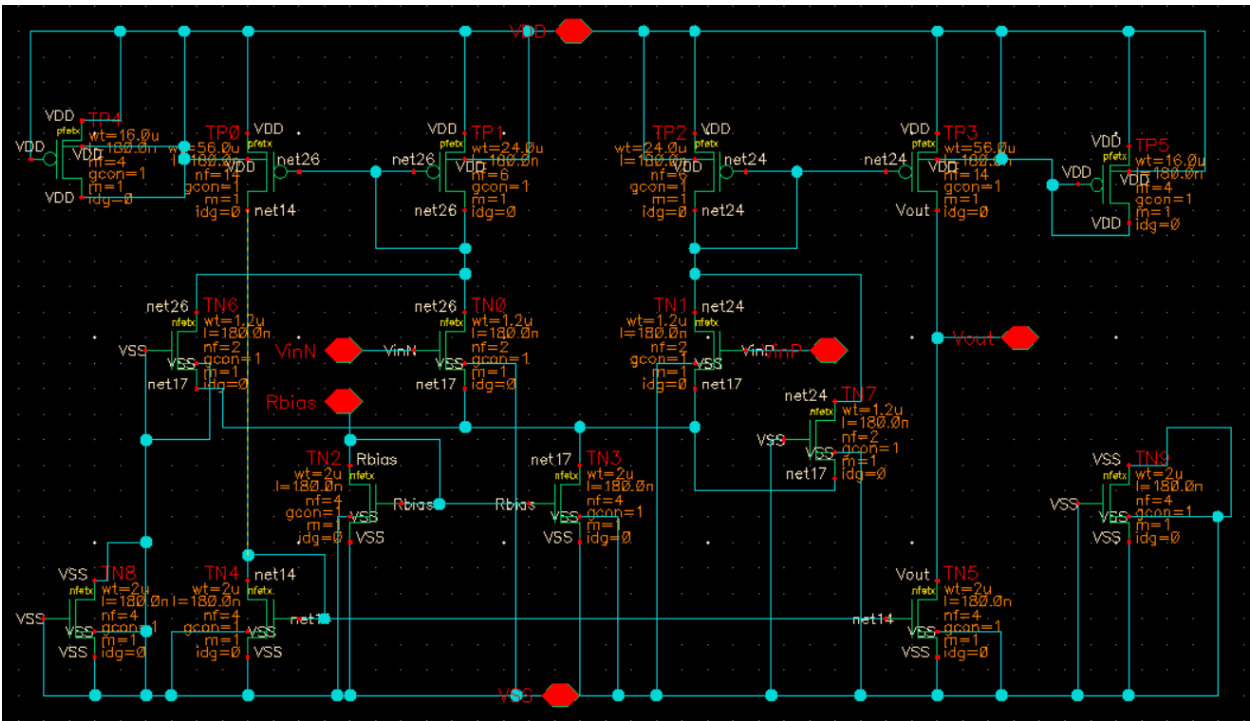


Acm

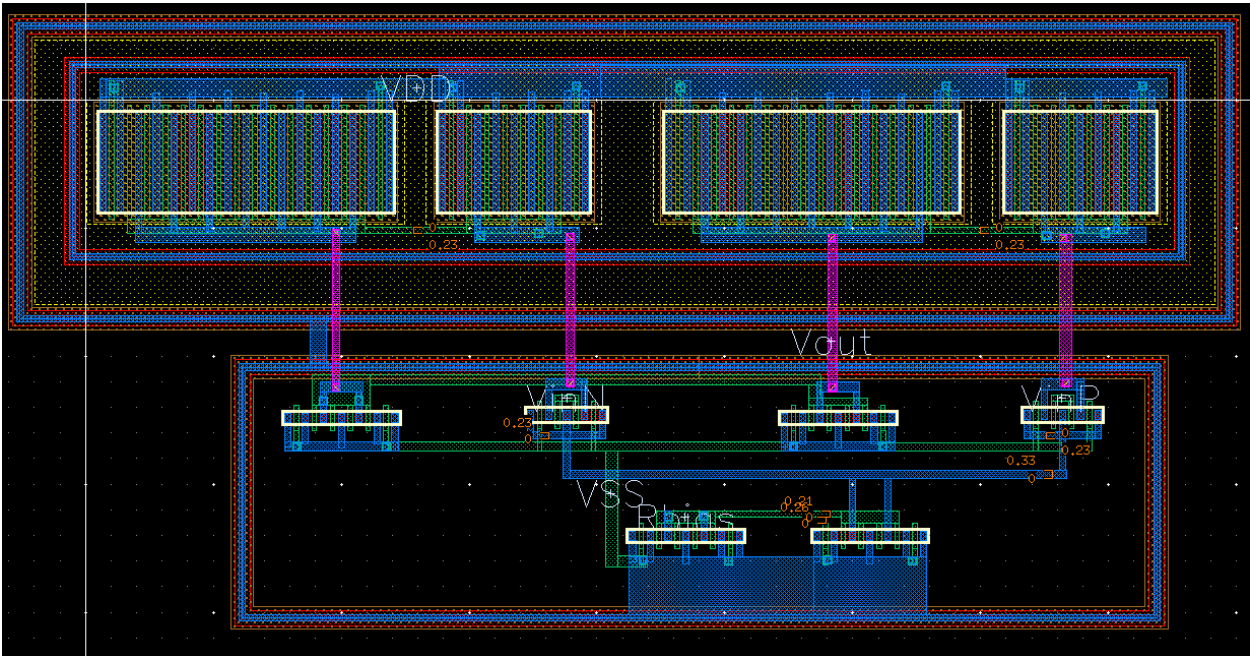


Transconductance

Layout Schematic:



Layout:



LVS:

```

REPORT FILE NAME:      OTA.lvs.report
LAYOUT NAME:          /home/ugrads/m/matthewloden/CAL/OTA.sp ('OTA')
SOURCE NAME:          /home/ugrads/m/matthewloden/LVS/OTA.netlist.lvs ('OTA')
RULE FILE:            /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:        Fri Nov 19 02:56:09 2021
CURRENT DIRECTORY:    /home/ugrads/m/matthewloden/CAL
USER NAME:            matthewloden
CALIBRE VERSION:      v2020.1_17.9   Fri Jan 3 14:53:07 PST 2020

```

OVERALL COMPARISON RESULTS

```

#          #          #####
#          #          #          *   *
#          #          #          |
#          #          #          \___/
#          #          #####

```

CORRECT

Warning: Unbalanced smashed mosfets were matched.

Results

Extraction Results

Comparison Results

ERC

ERC Results

ERC Summary

Reports

Extraction Report

LVS Report

Rules

Rules File

View

Info

Finder

Schematics

Setup

Options

Layout Cell / Type	Source Cell	Nets	Insta
OTA	OTA	10L, 10S	14L, 1

Cell OTA Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```

#          #          #####
#          #          #          *   *
#          #          #          |
#          #          #          \___/
#          #          #####

```

CORRECT

Warning: Unbalanced smashed mosfets were matched.

LAYOUT CELL NAME: OTA
SOURCE CELL NAME: OTA

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	10	10	
Instances:	32	10	* MN (4 pins)
	48	6	* MP (4 pins)
Total Inst:	80	16	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

REPORT FILE NAME: OTA.lvs.re

LAYOUT NAME: /home/ugre

SOURCE NAME: /home/ugre

RULE FILE: /home/ugre

CREATION TIME: Fri Nov 15

CURRENT DIRECTORY: /home/ugre

USER NAME: matthewLoc

CALIBRE VERSION: v2020.1_17

OVERF

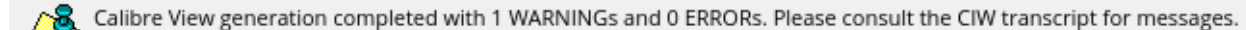
```

#          #          ###
#          #          #
#          #          #
#          #          #
#          #          ###

```

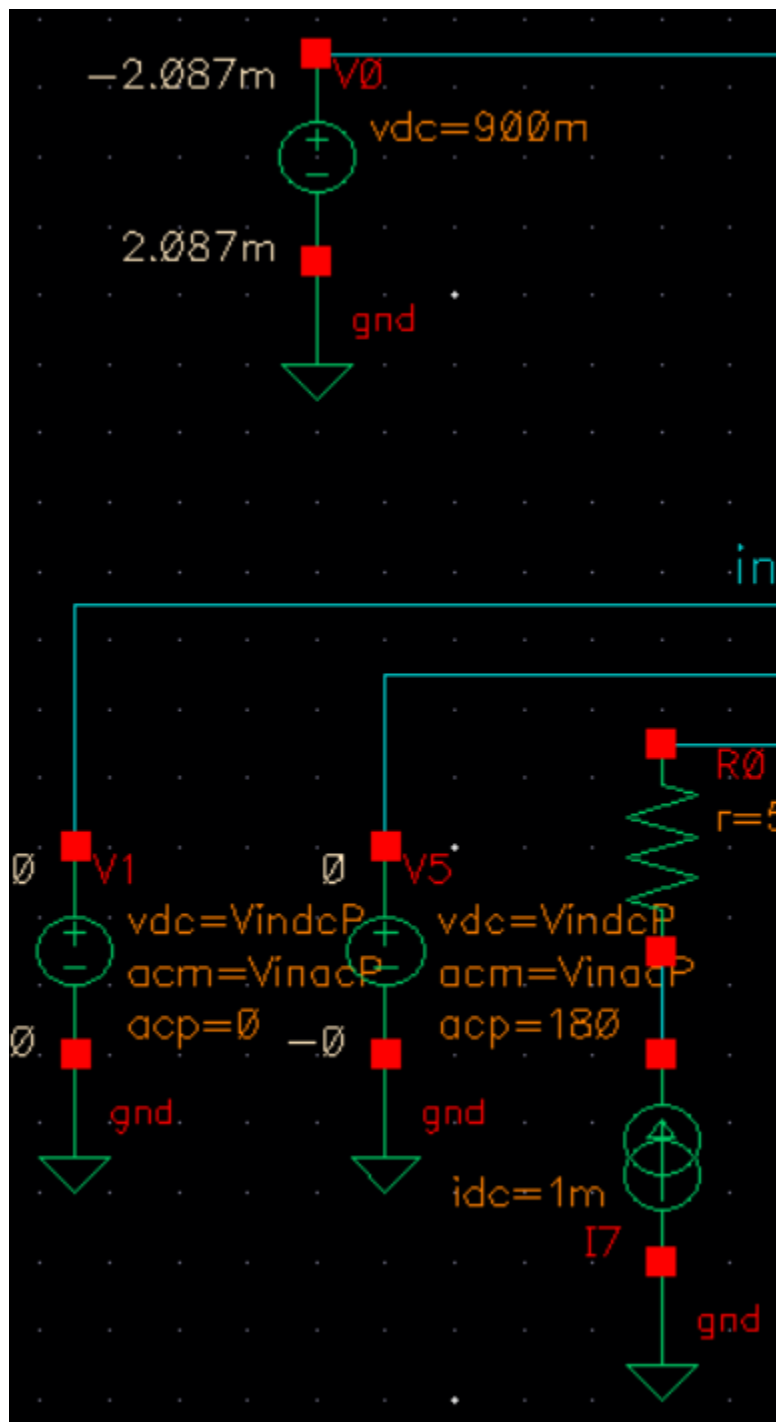
Warning: Unbalanced smashed mosfe

DRC:

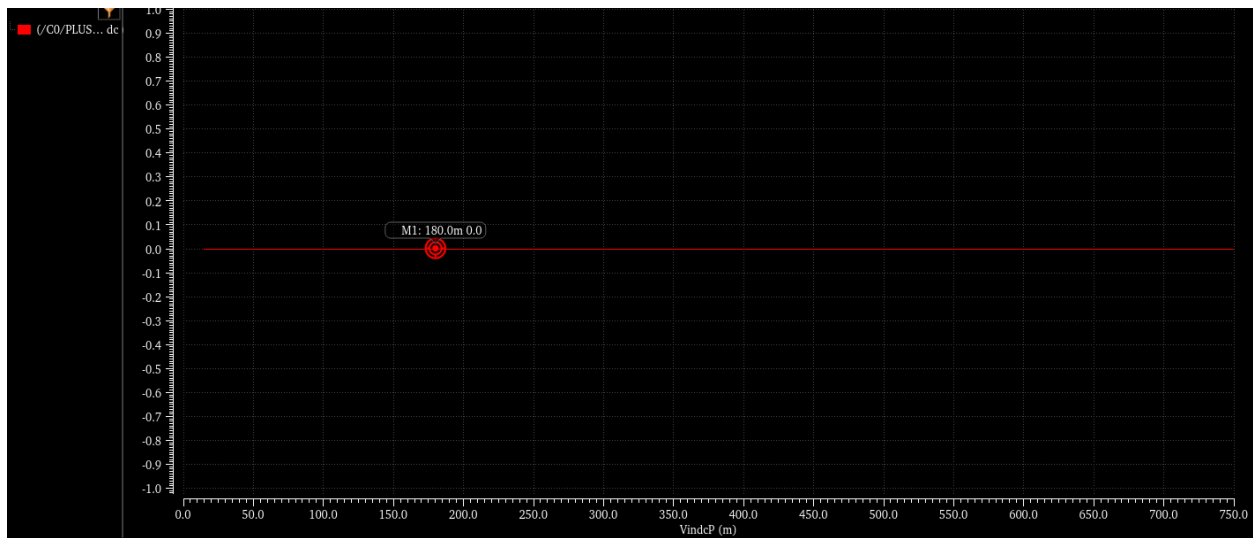


Post Lab Data Calculations and Simulations:

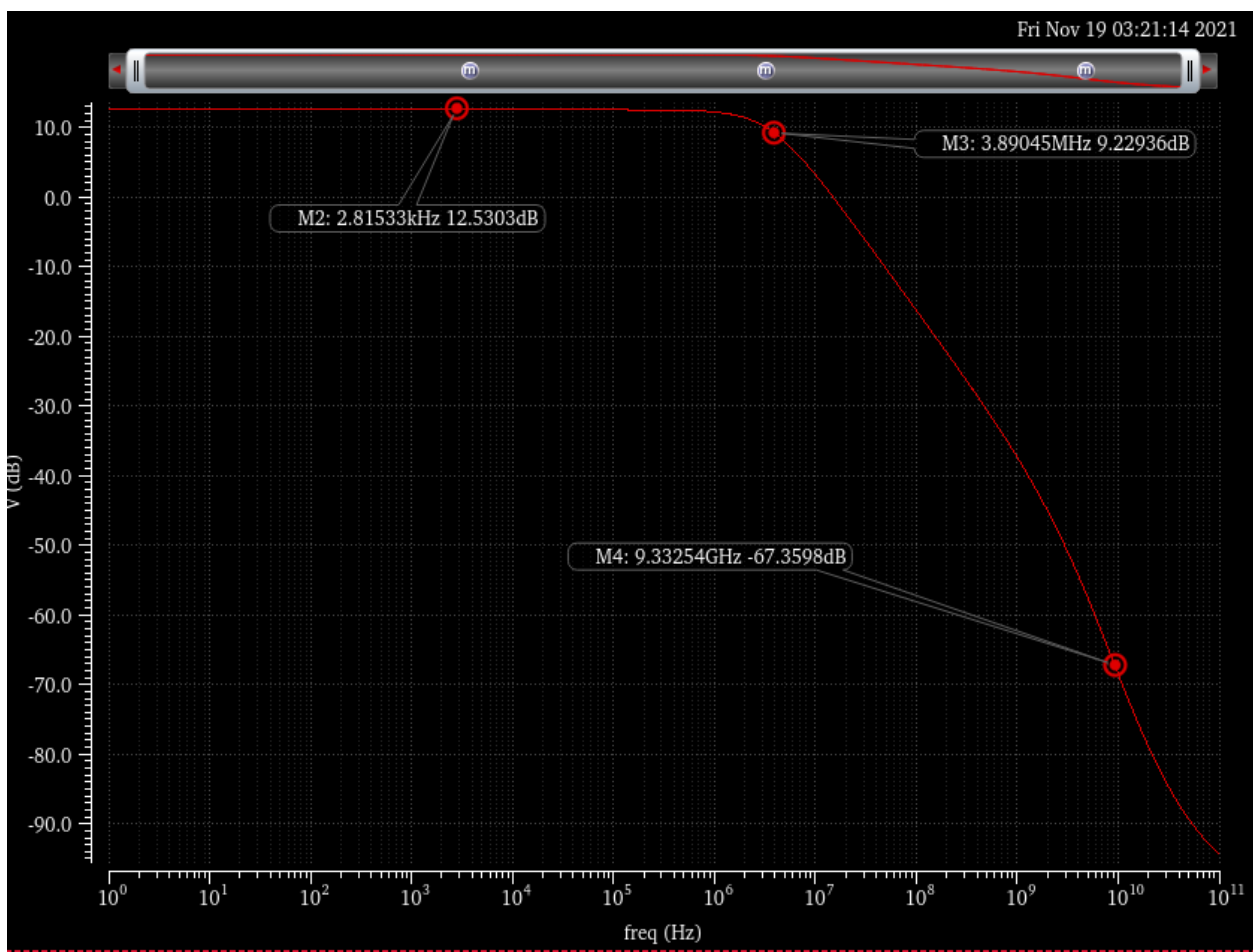
Power Provided by the Voltage Source



$$\text{Power} = 1.8 \cdot (2.087 - 1) = 1.9566mW$$

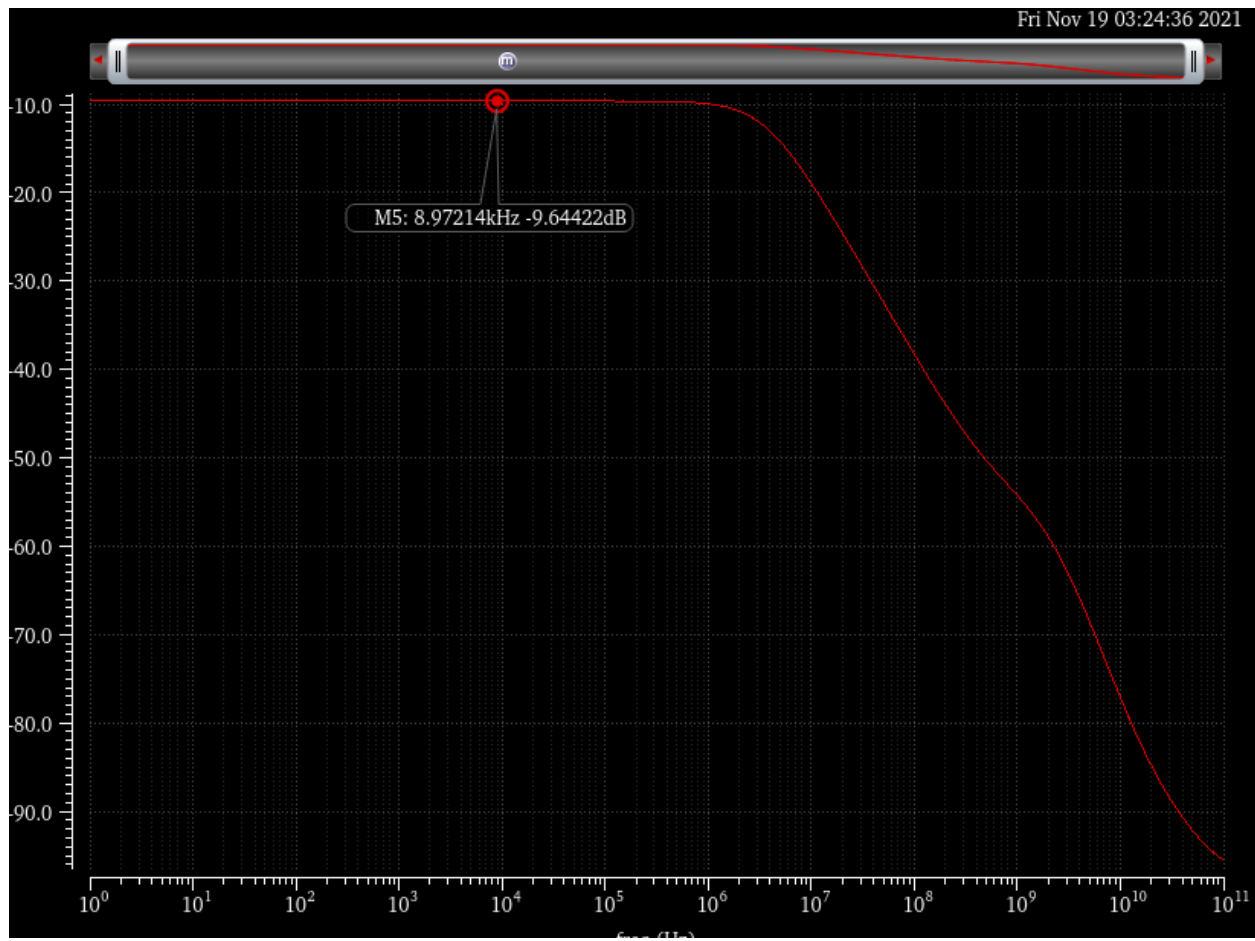


Transconductance



Adm Gain: 12.53dB , P1 = 3.89MHz , GBW = 16.46MHz

$P2 = 9.33 \text{ GHz}$, the stability of the system is ensured due to sufficiently large difference from the first pole to the second $\gg 3$ factor.



Acm = -9.63dB