Matthew Loden

ECEN 474-502

Lab 02: LayoutDesign, Simulation and Verification in Cadence

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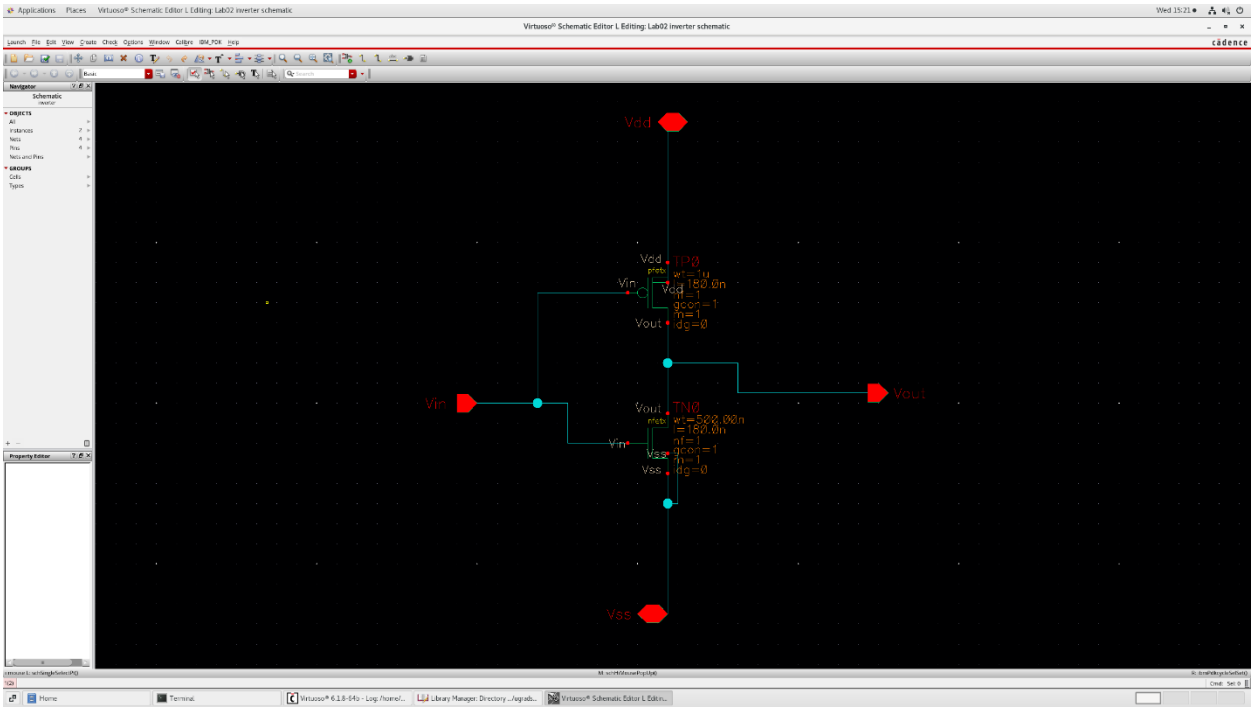
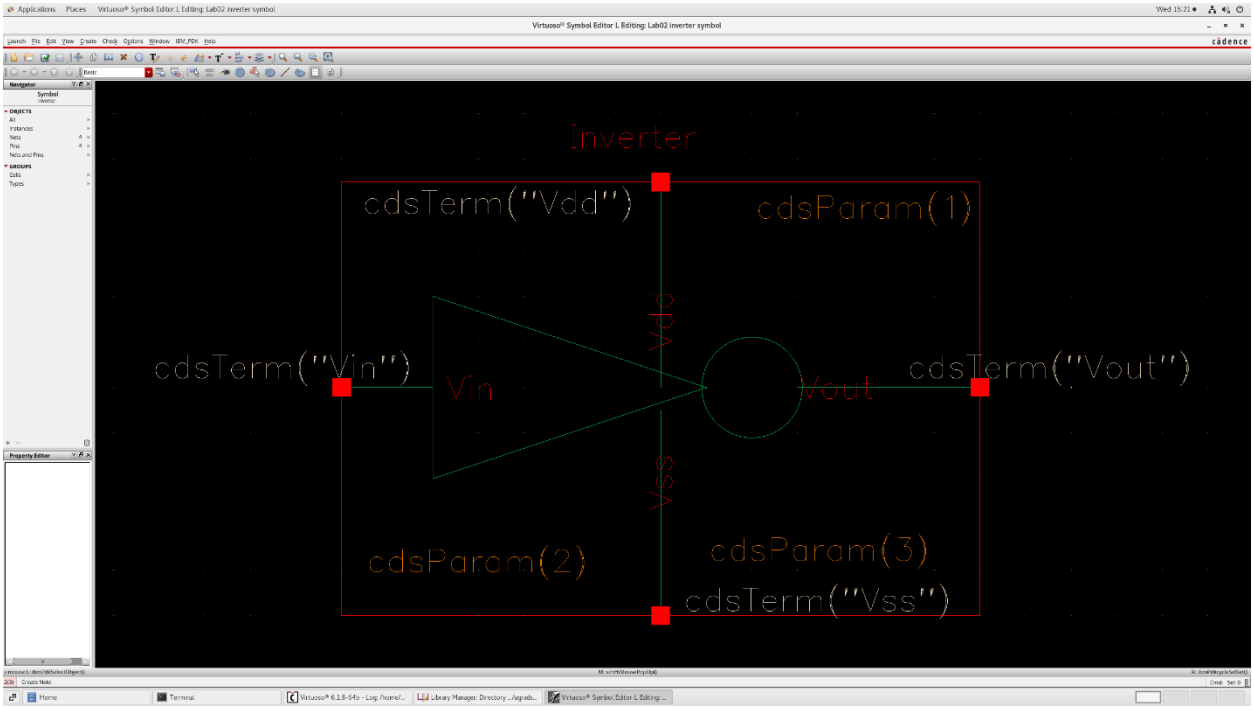
TA: Navid Naseh

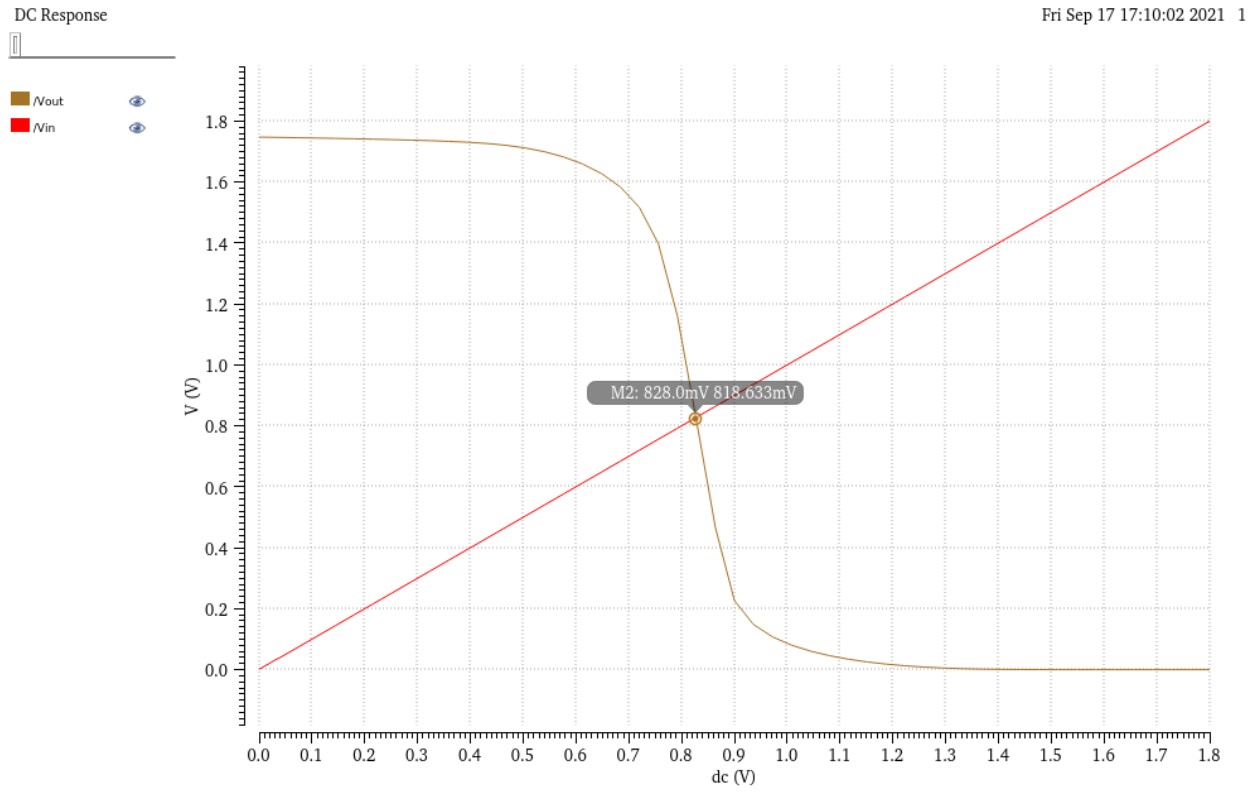
Inverter Schematic:



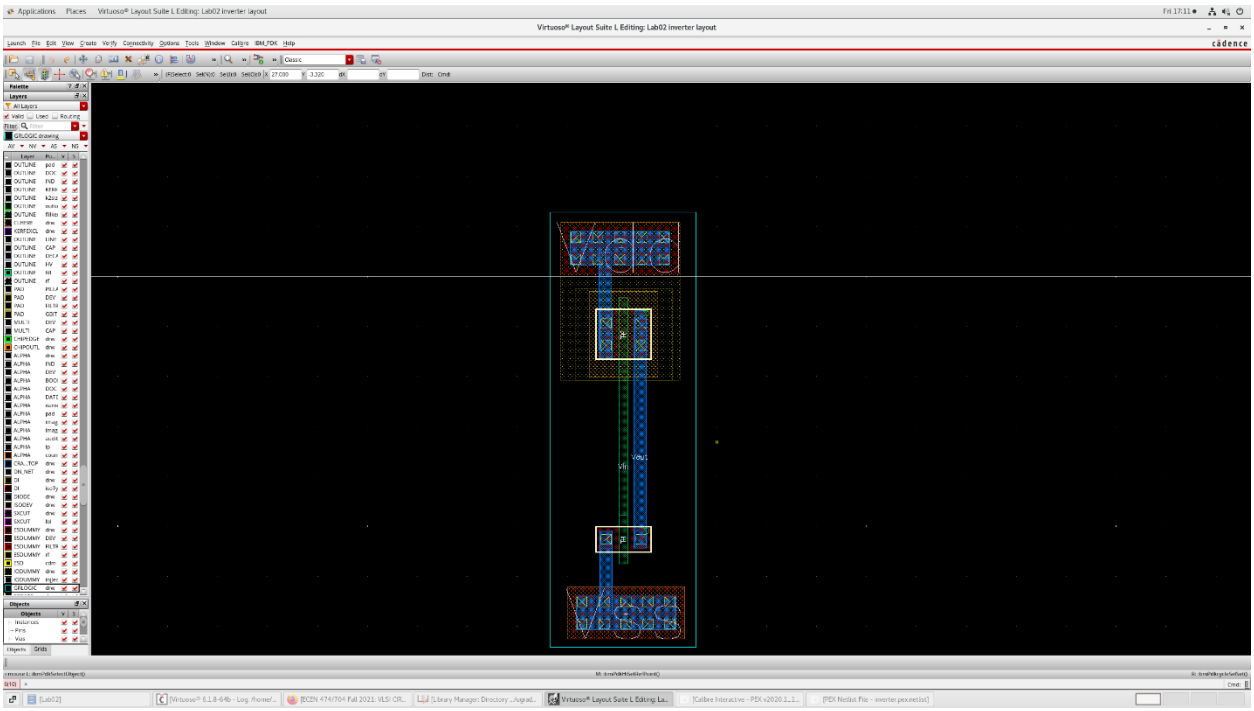
Inverter Symbol:



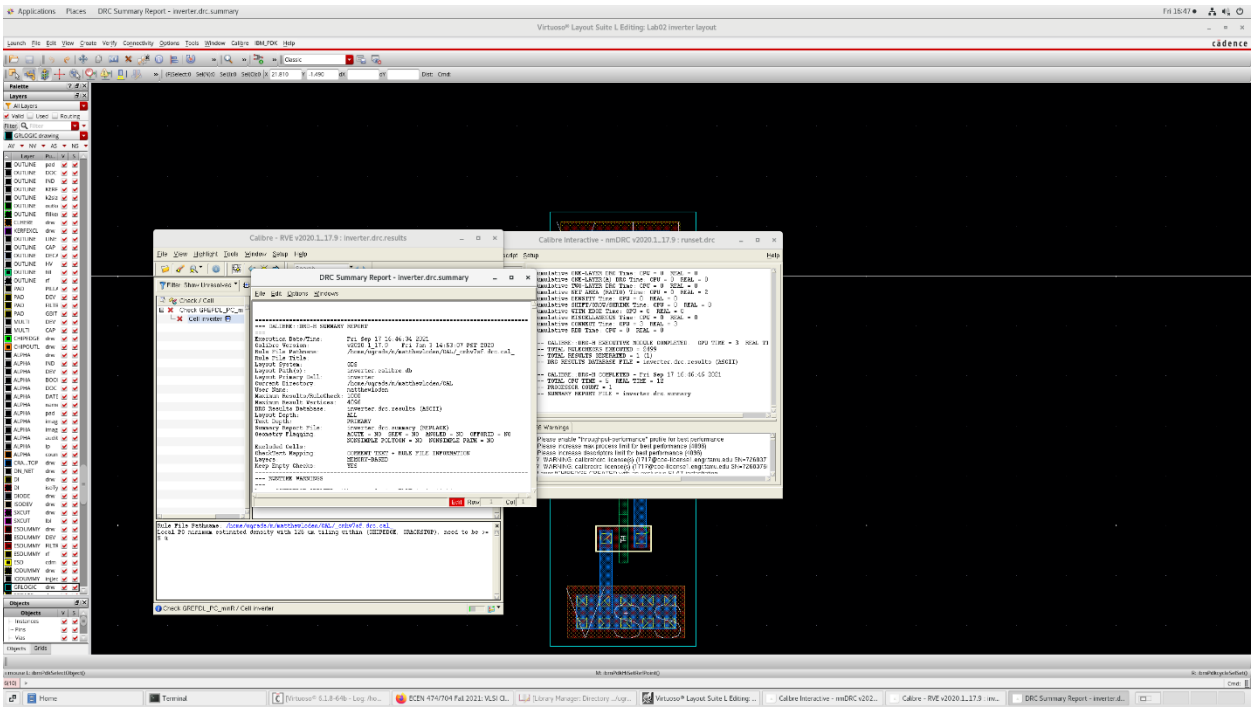
Inverter Testbench with Default Options:



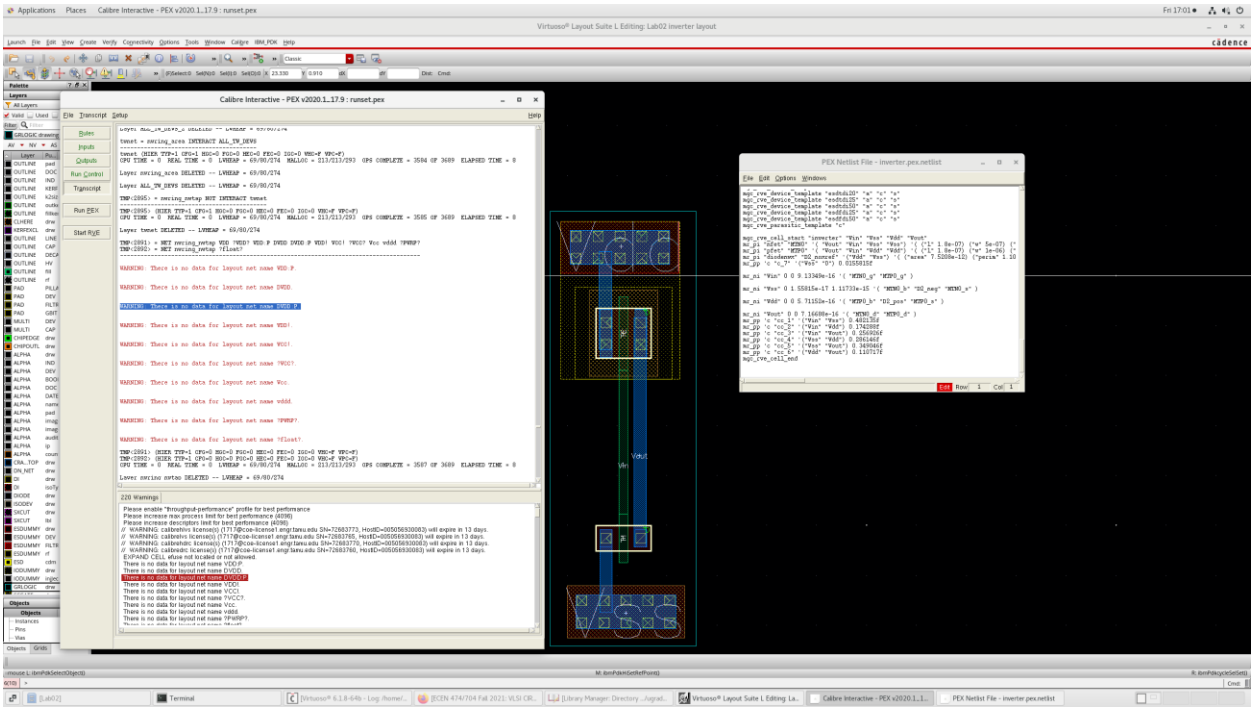
Inverter Layout:



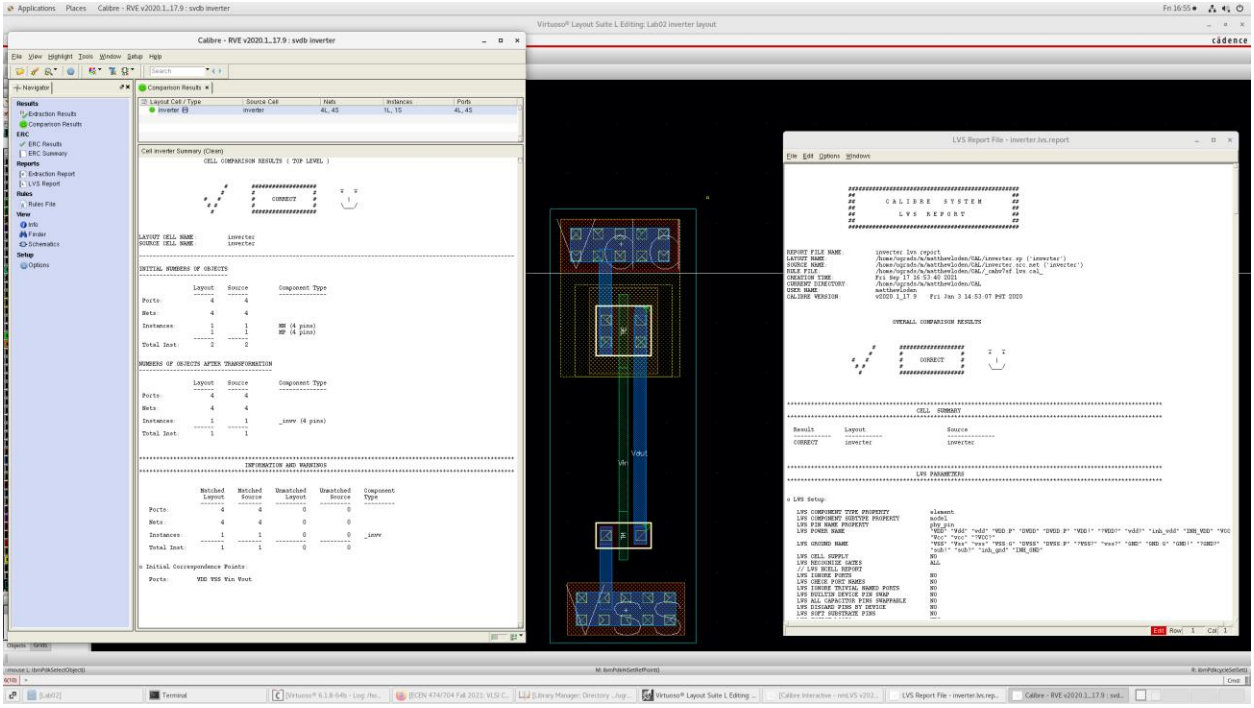
Inverter DRC:



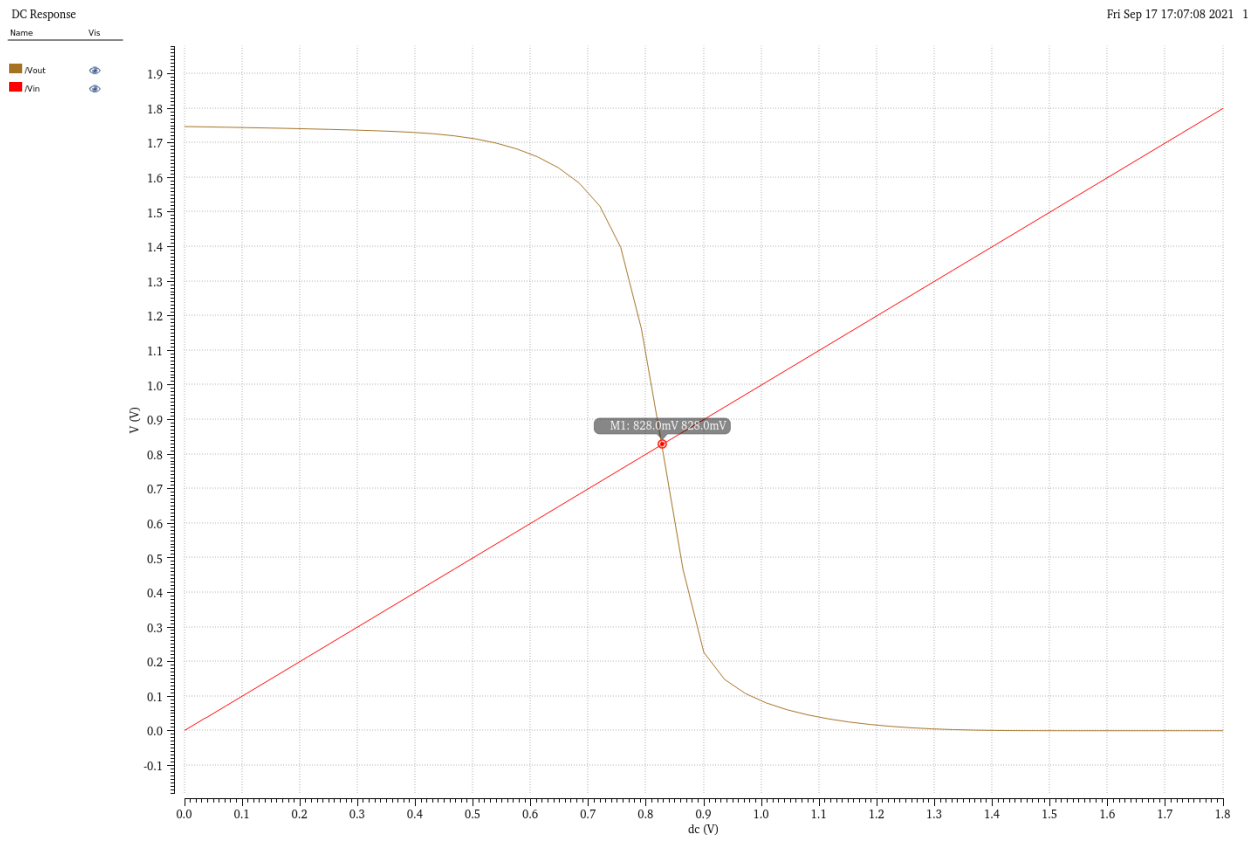
Inverter PEX View



Inverter extracted and LVS:



Inverter Testbench with User Created



Discussion:

In this lab we constructed an Inverter using CMOS transistor logic. Using the program Cadence, we constructed the schematic view with a PMOS and NMOS transistor. Then we created the symbol view following the standard used in industry. After the basic steps were out of the way, we ran a simulation of the schematic using a pre-built layout generated by the system to evaluate the operation of the gate. The resulting data was plotted in a voltage vs voltage manner. The graph shows that as the voltage on the gate increases, the voltage on the output will be exactly opposite. After we took this data, we began constructing our own layout of the physical transistors. This layout passed the design rules check (DRC) which made sure that each component was properly distanced from other parts and that there were adequate connections between layers. After the DRC passed, we extracted the design and it's parasitic capacitors which allowed us to conduct a layout verification. This test made sure that the layout we created was equivalent to the schematic we created, and it was correct so they were functionally the same. Once we had completed the layout, we re-ran the previous test on the inverter however this time we used the hardware we created in the layout portion of the lab. This resulted in an identical graph of the input and output voltages which means that we created a functionally equivalent layout to the standard.