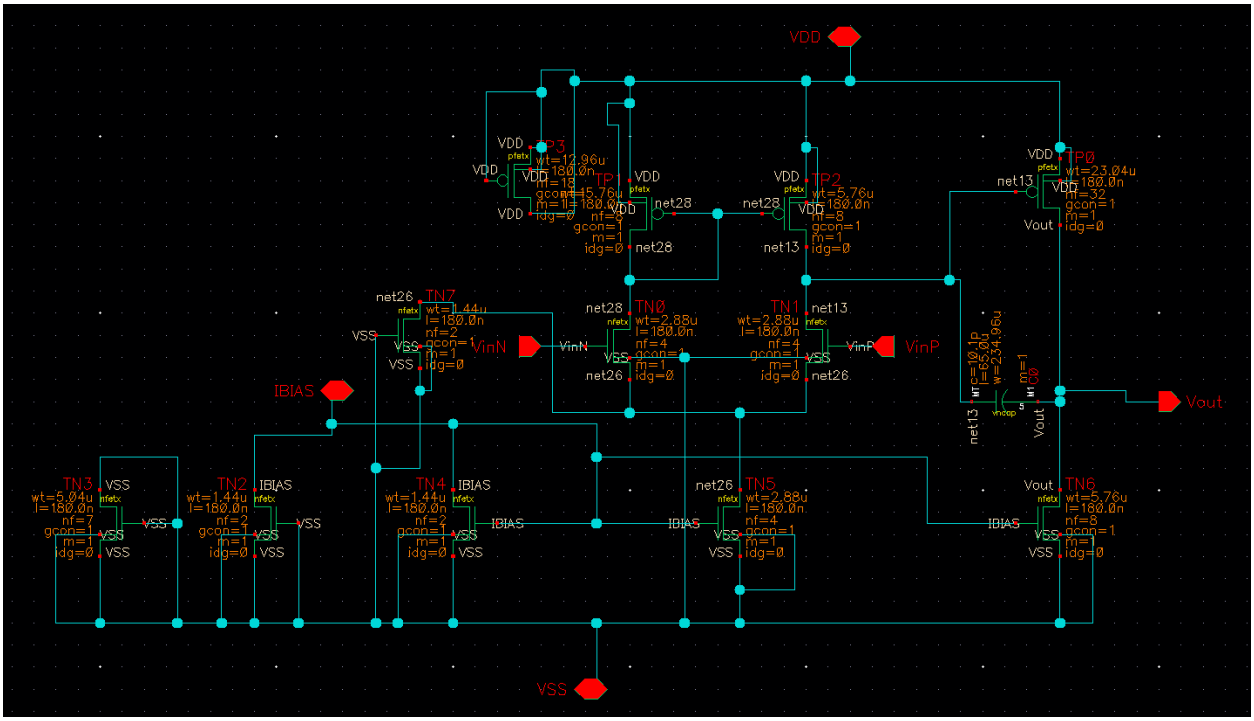
Matthew Loden

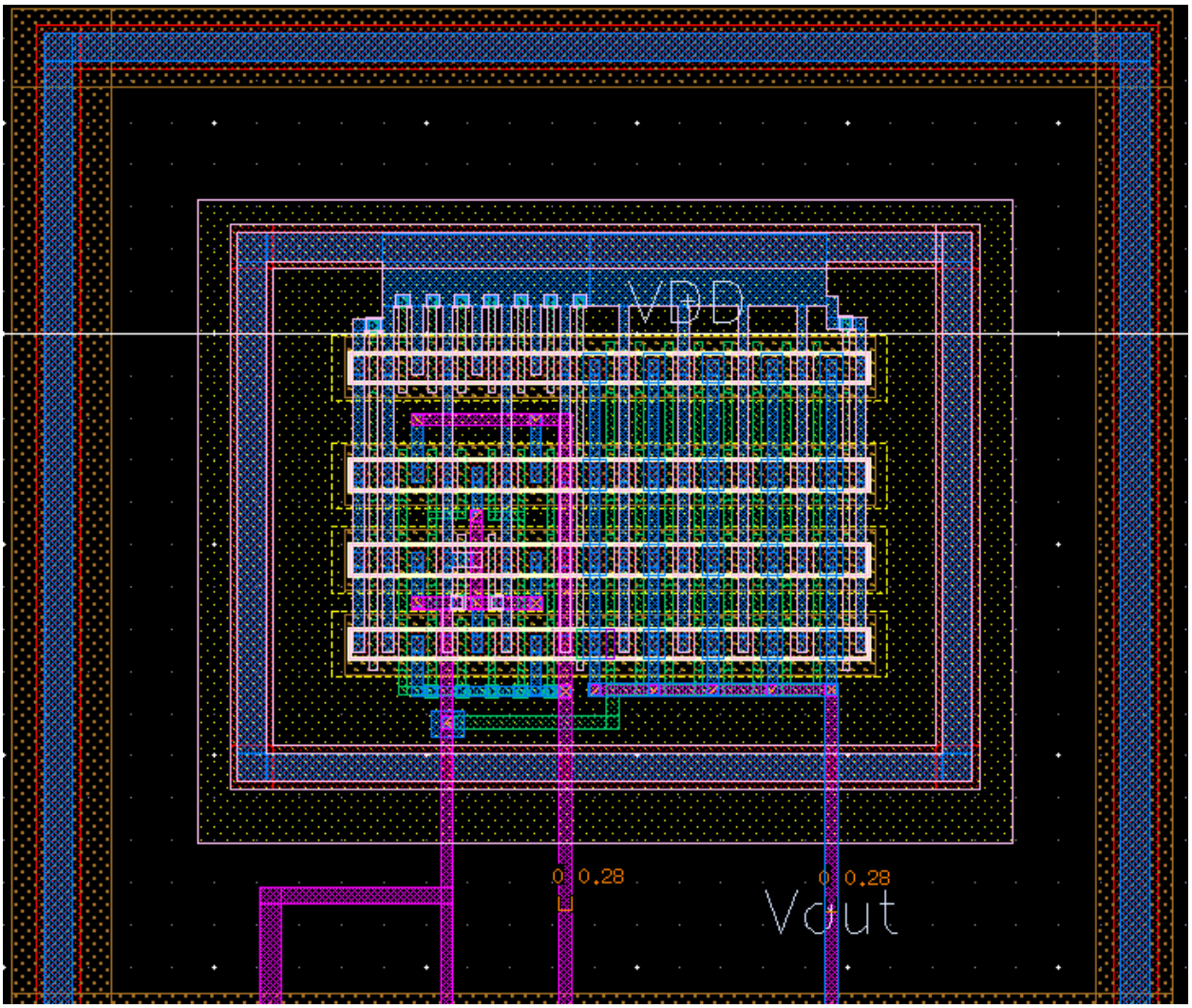
ECEN 474

Lab 04 – Advanced Layout Techniques

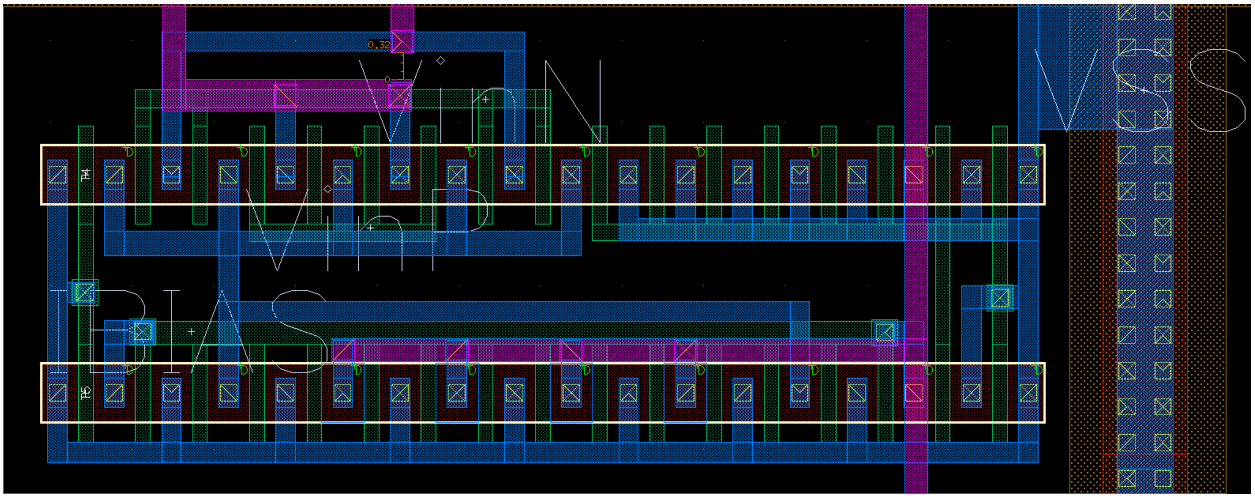
Schematic View:



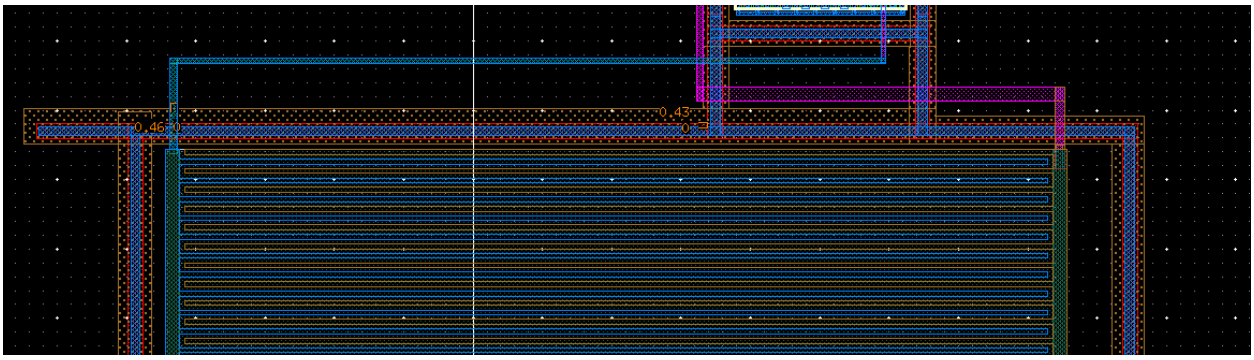
Layout:



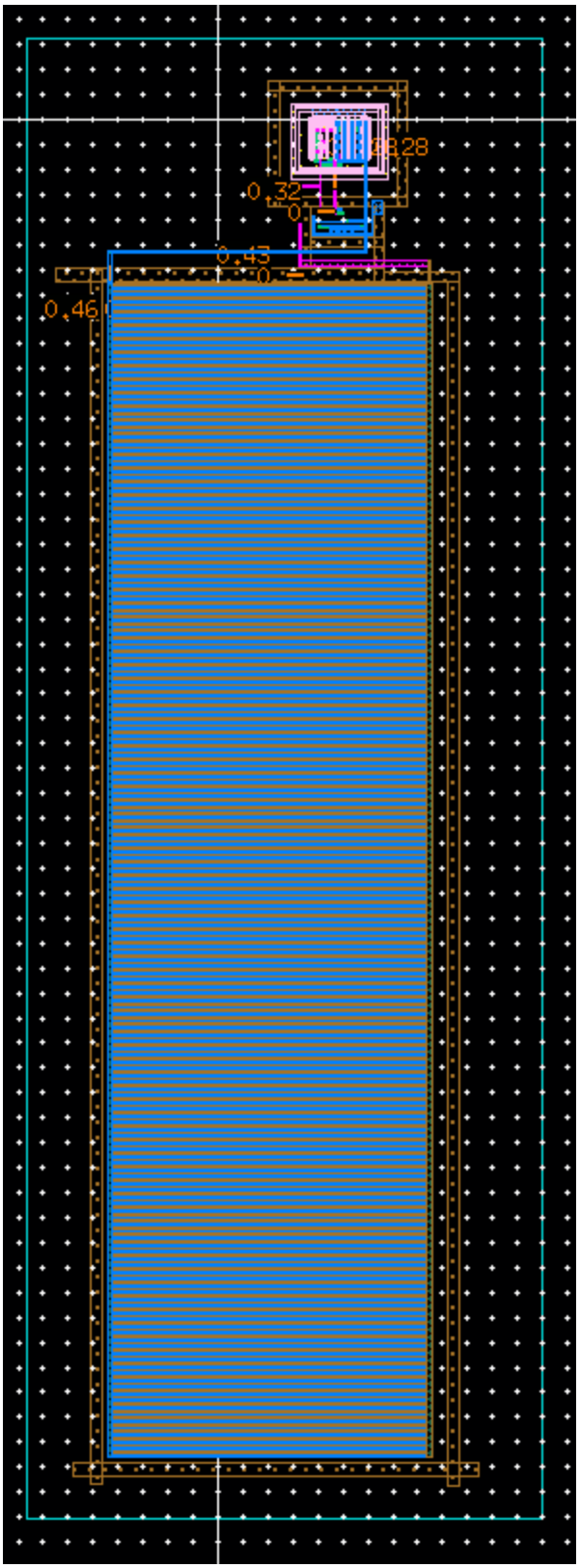
Nmos layout:



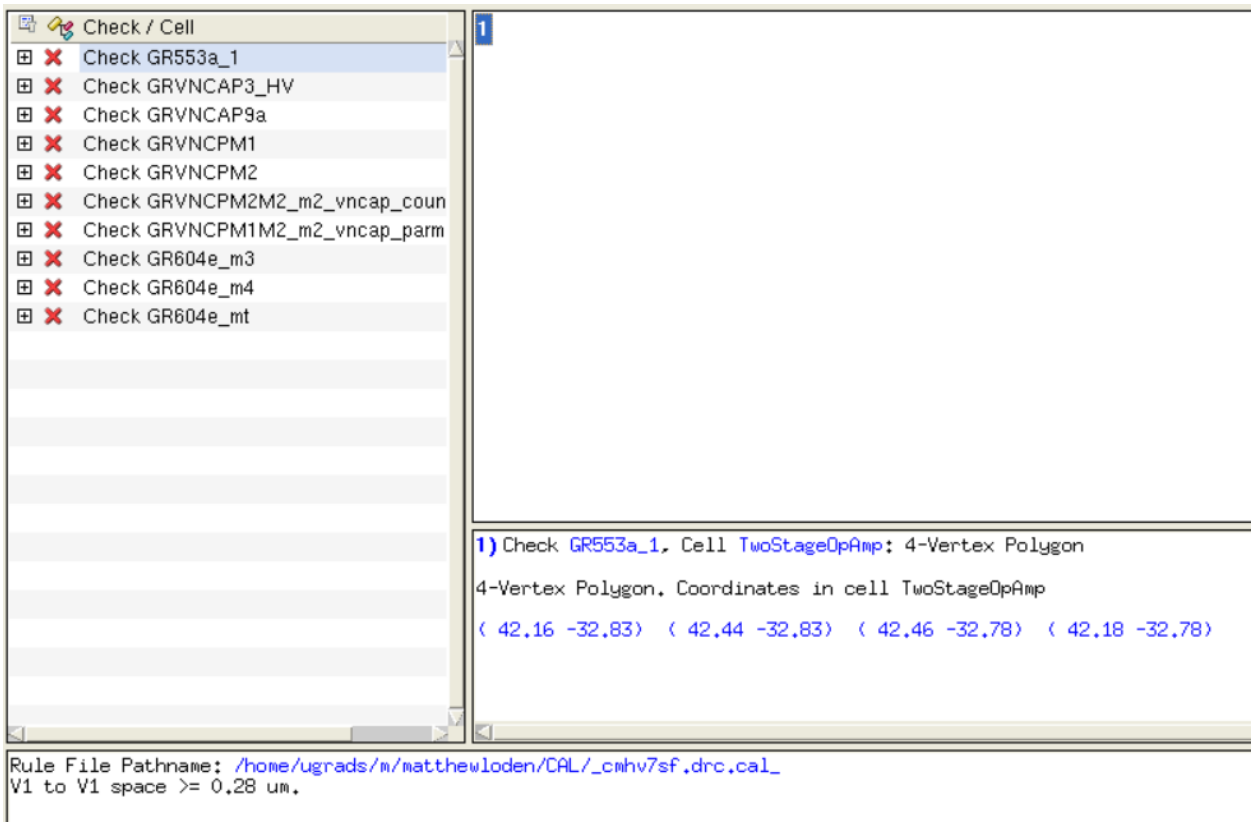
Cap layout:



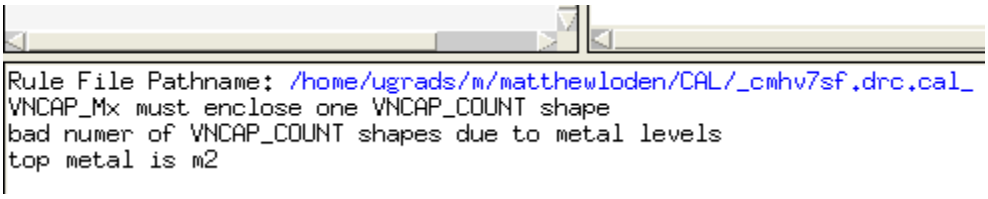
All of it



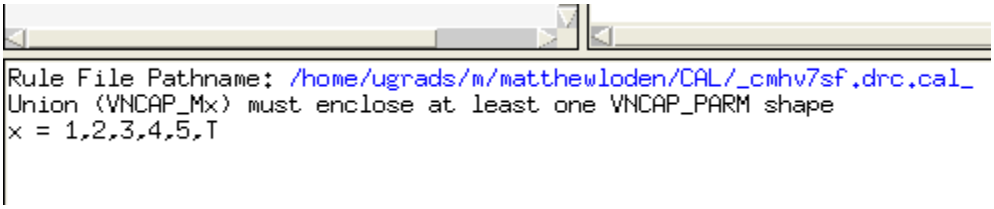
DRC Check:



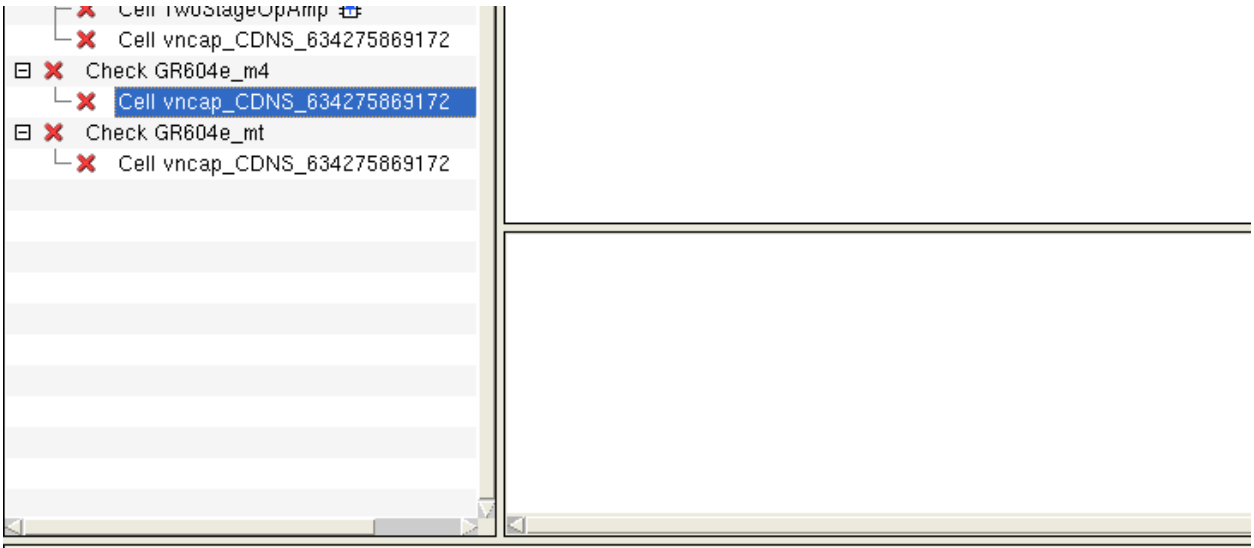
My DRC is kind of a mess however most of the issues could be resolved if my capacitor was correctly connected. I have 13 total DRC errors however 9 of them are related to the capacitor. An example of this is:



Or:



The first DRC error is warning about a via being too close to another via however that is where I am transitioning to the Capacitor, so I was just trying to get that to work more than I care about this small DRC error check. The remaining DRC errors come from using metal layers to travel large distances on my layout, so they are throwing errors like:

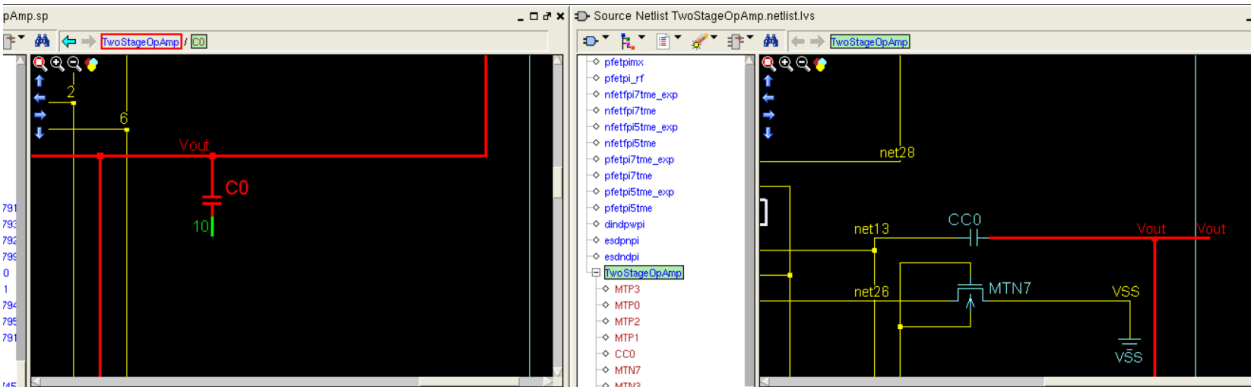



```
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
M4 space >= 0.80 um. ([if one M4 shape is greater than 200um2 and is not electrically connected to RX]
and [the other M4 shape (of any area) is electrically connected to RX])
```

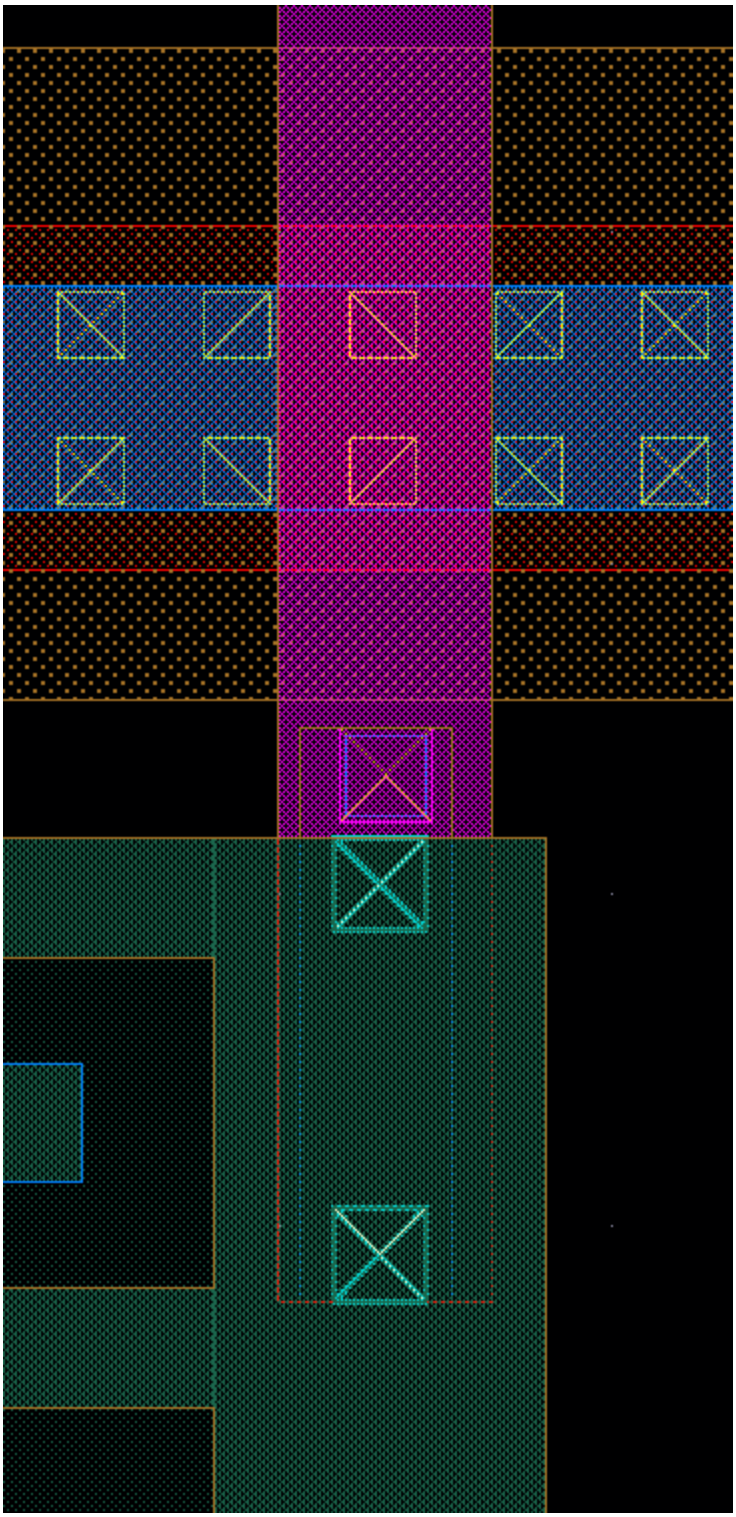
LVS Check:

```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##            L V S   R E P O R T             ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         TwoStageOpAmp.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/TwoStageOpAmp.sp ('TwoStageOpAmp')
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/TwoStageOpAmp.netlist.lvs ('TwoStageOpAmp')
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Fri Oct 15 00:10:03 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                          OVERALL COMPARISON RESULTS


                #   #         ####################
                 # #          #                  #
                  #           #     INCORRECT    #
                 # #          #                  #
                #   #         ####################


  Error:    Different numbers of instances.
  Error:    Property errors.


*****************************************************************************************************************
                                    CELL  SUMMARY
*****************************************************************************************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  INCORRECT      TwoStageOpAmp               TwoStageOpAmp
```

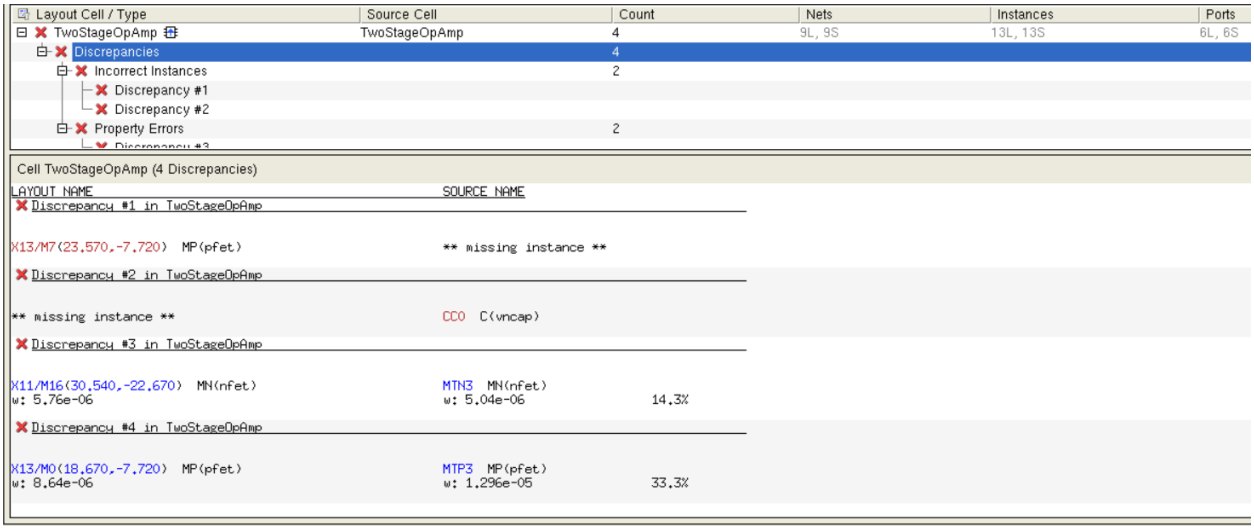
My main errors come from the capacitor connection not being correctly connected into the circuit. The error shown below demonstrates this:

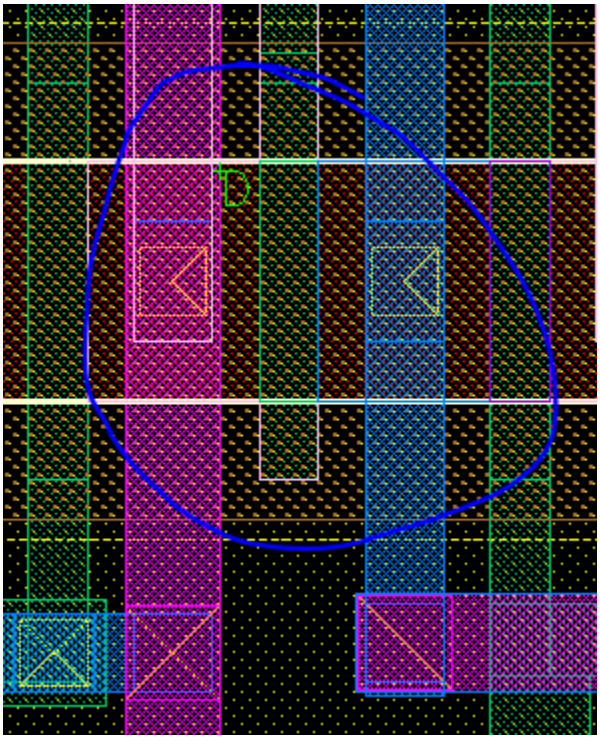


This should be resolvable by connecting the top plate the relevant area however no matter what I do it won't connect correctly… I am using m1 to continue over the connection region then using a M1 to MT via placed over that region and it still won't register the connection point.



In addition to this weird connection error, I also had an error with the connection of the dummy to the correct location within my PMOS section. This error however made no sense to me so perhaps I don't understand it well enough.





My understanding is that the dummy gate is sharing a drain with it's neighboring M8 on the right and they are traveling to different locations. I'm sure there is a fix to this problem, but I can't figure out why it is only affecting this side of the transistor layout and not the other side which is set up the same way.