Matthew Loden

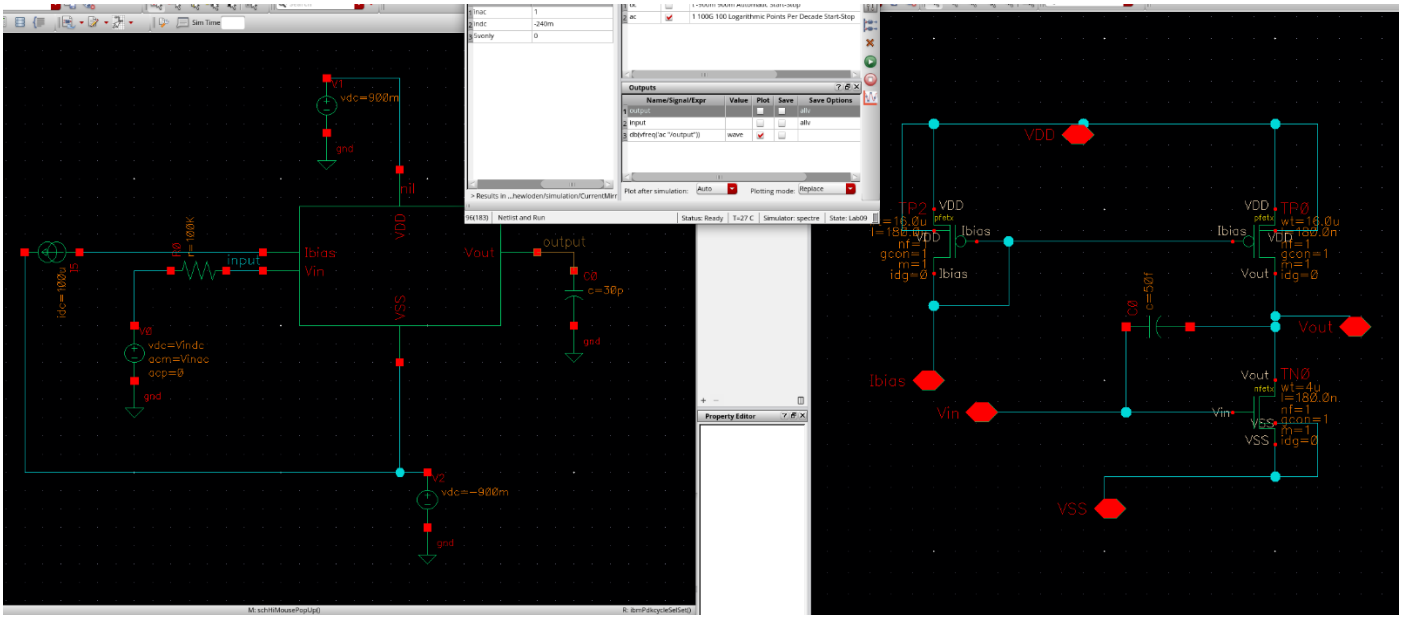
ECEN 474

Lab 07 – Characterization of Inverters

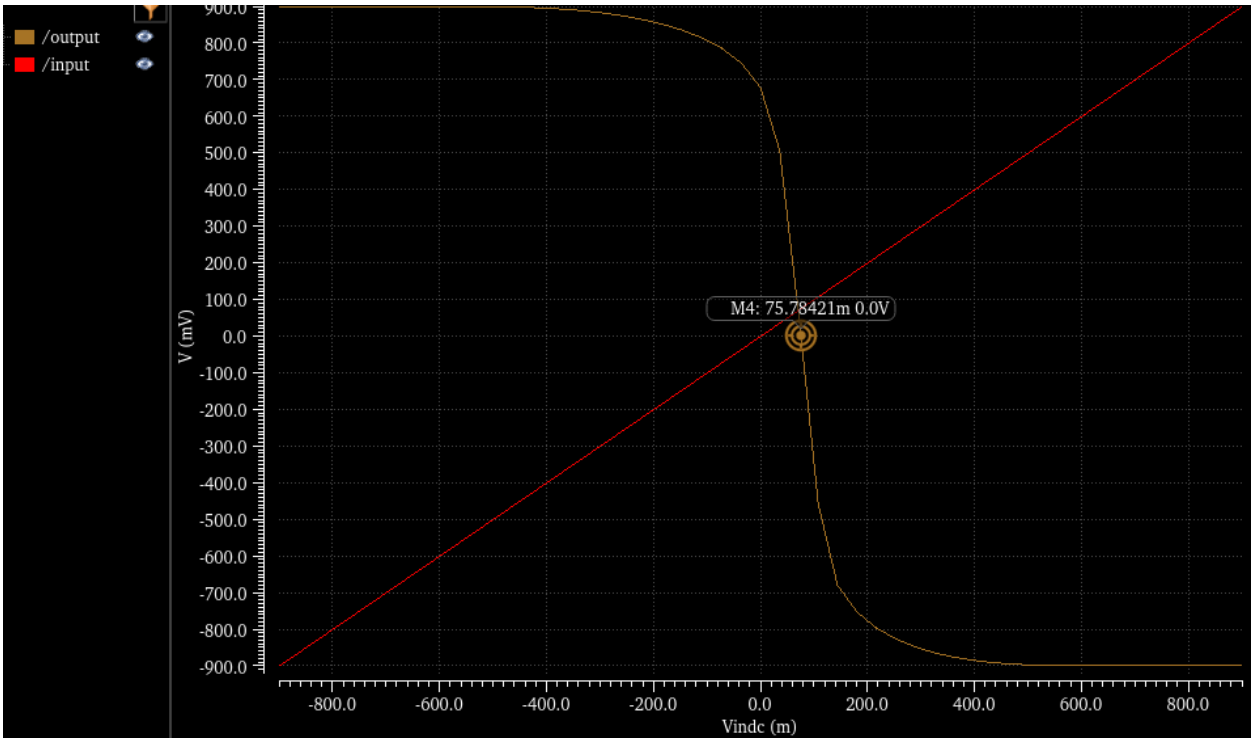
Relevant Data for all values found at end of report.

Current Mirror Load Information:

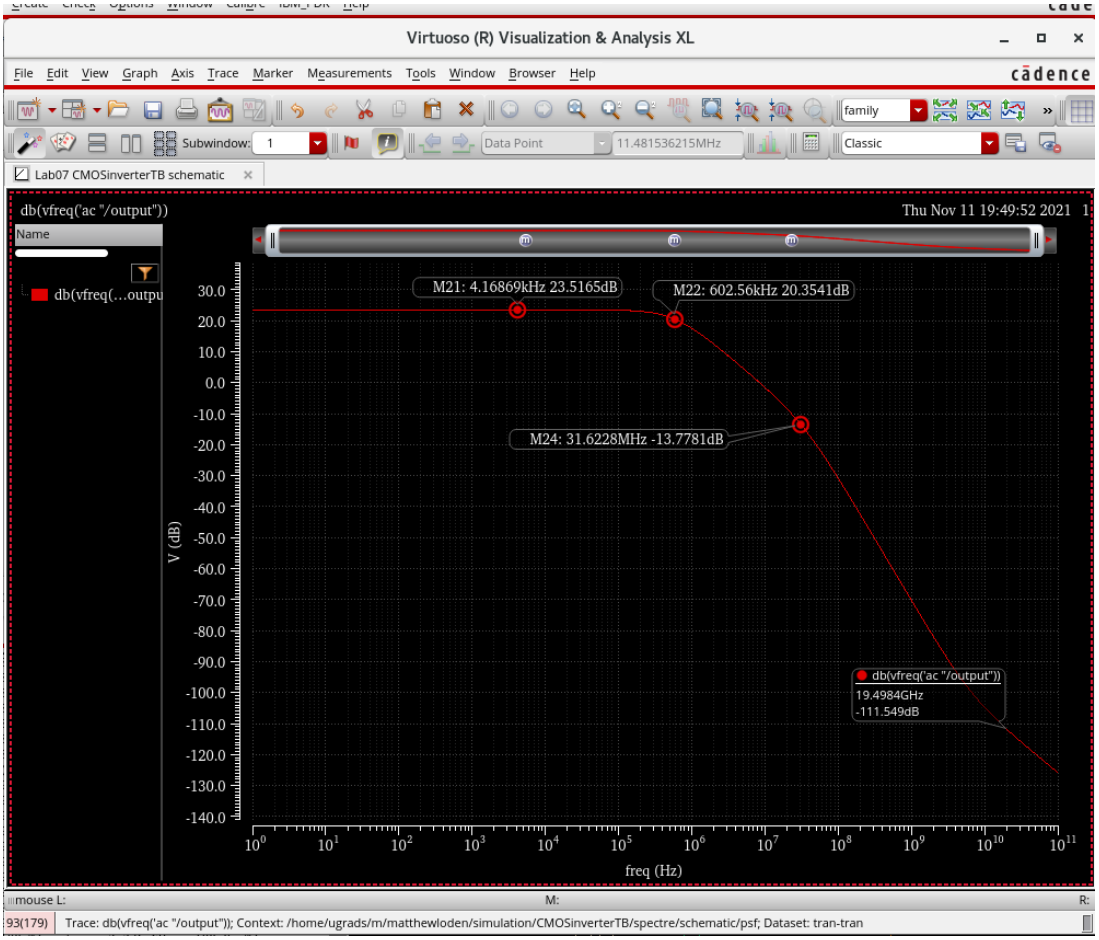
Schematic:



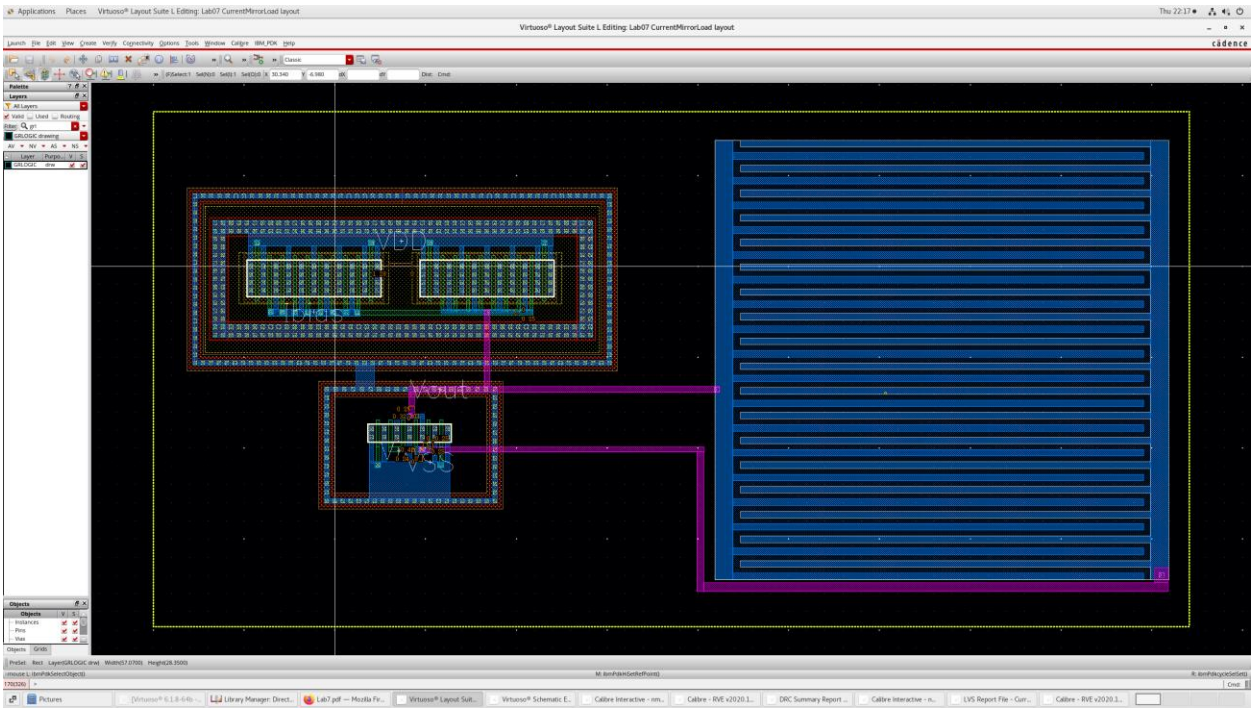
Dc Operation Point Curve:



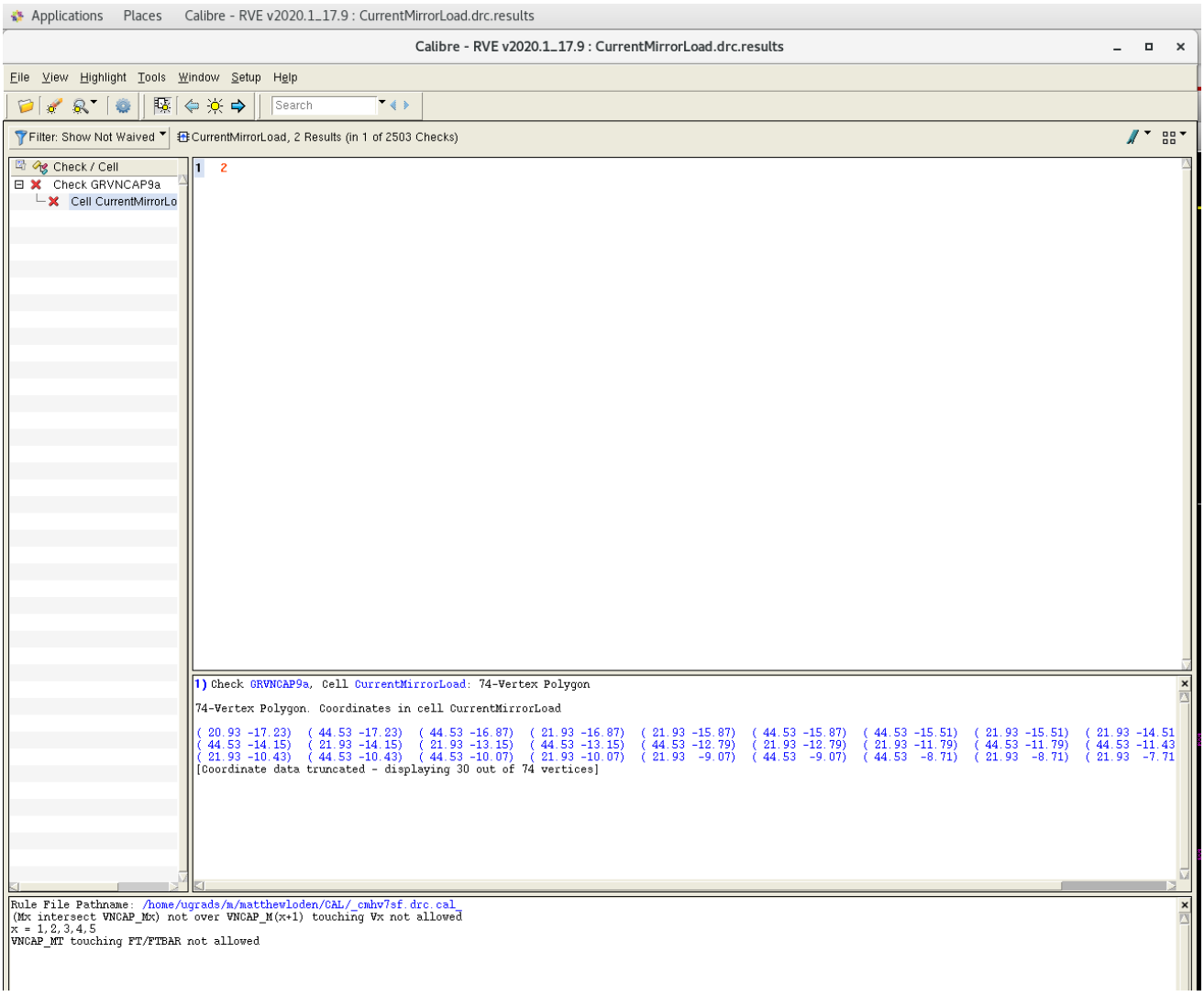
Gain/Pole1/Pole2:


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Lab07 CMOSinverterTB schematic
db(vfreq('ac "/output"))
Thu Nov 11 19:49:52 2021
Name
M21: 4.16869kHz 23.5165dB
M22: 602.56kHz 20.3541dB
M24: 31.6228MHz -13.7781dB
db(vfreq('ac "/output"))
19.4984GHz
-111.549dB
V (dB)
freq (Hz)
mouse L:
M:
R:
Trace: db(vfreq('ac "/output")); Context: /home/ugrads/m/matthewloden/simulation/CMOSinverterTB/spectre/schematic/psf; Dataset: tran-tran

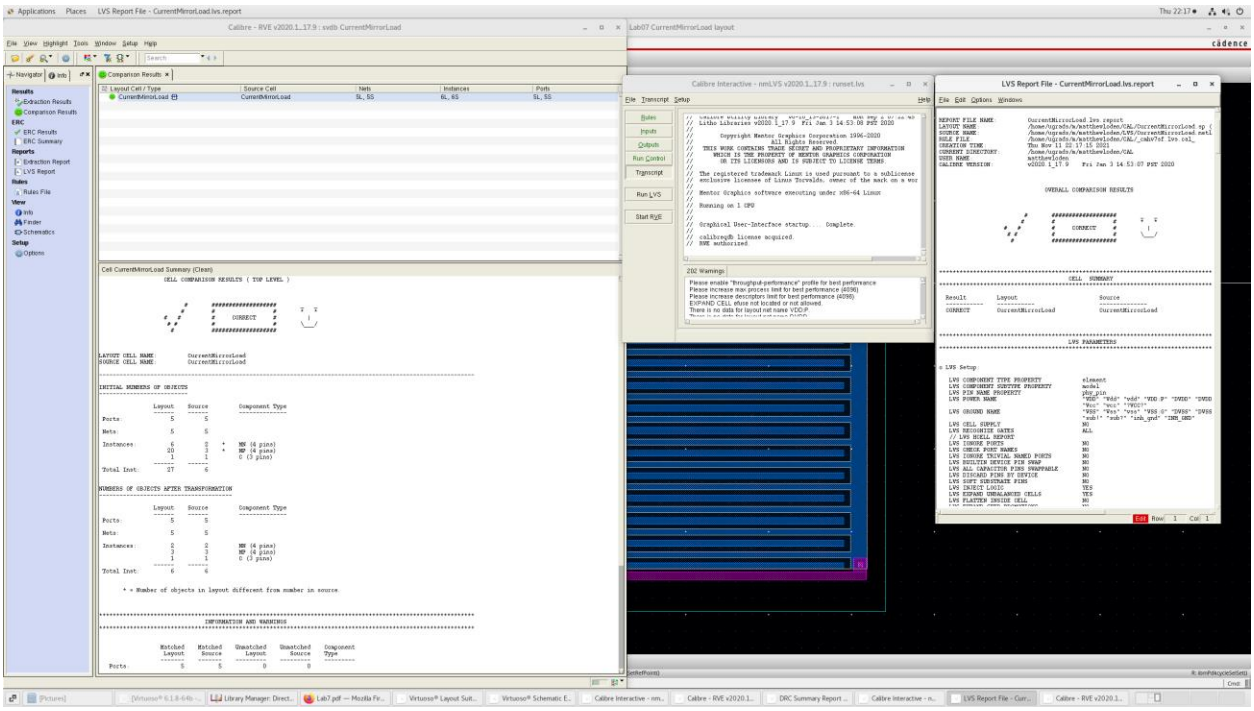
Layout:


Virtuoso® Layout Suite L Editing: Lab07 CurrentMirrorLoad layout
cadence
VDD
VOUT
VSS

DRC:


Applications Places Calibre - RVE v2020.1_17.9 : CurrentMirrorLoad.drc.results
Calibre - RVE v2020.1_17.9 : CurrentMirrorLoad.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show Not Waived
CurrentMirrorLoad, 2 Results (in 1 of 2503 Checks)
Check / Cell
Check GRVNCAP9a
Cell CurrentMirrorLo
1 2
1) Check GRVNCAP9a, Cell CurrentMirrorLoad: 74-Vertex Polygon
74-Vertex Polygon. Coordinates in cell CurrentMirrorLoad
(20.93 -17.23) (44.53 -17.23) (44.53 -16.87) (21.93 -16.87) (21.93 -15.87) (44.53 -15.87) (44.53 -15.51) (21.93 -15.51) (21.93 -14.51
(44.53 -14.15) (21.93 -14.15) (21.93 -13.15) (44.53 -13.15) (44.53 -12.79) (21.93 -12.79) (21.93 -11.79) (44.53 -11.79) (44.53 -11.43
(21.93 -10.43) (44.53 -10.43) (44.53 -10.07) (21.93 -10.07) (21.93 -9.07) (44.53 -9.07) (44.53 -8.71) (21.93 -8.71) (21.93 -7.71
[Coordinate data truncated - displaying 30 out of 74 vertices]
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal
(Mx intersect VNCAP_Mx) not over VNCAP_M(x+1) touching Vx not allowed
x = 1, 2, 3, 4, 5
VNCAP_MT touching FT/FTBAR not allowed

LVS:

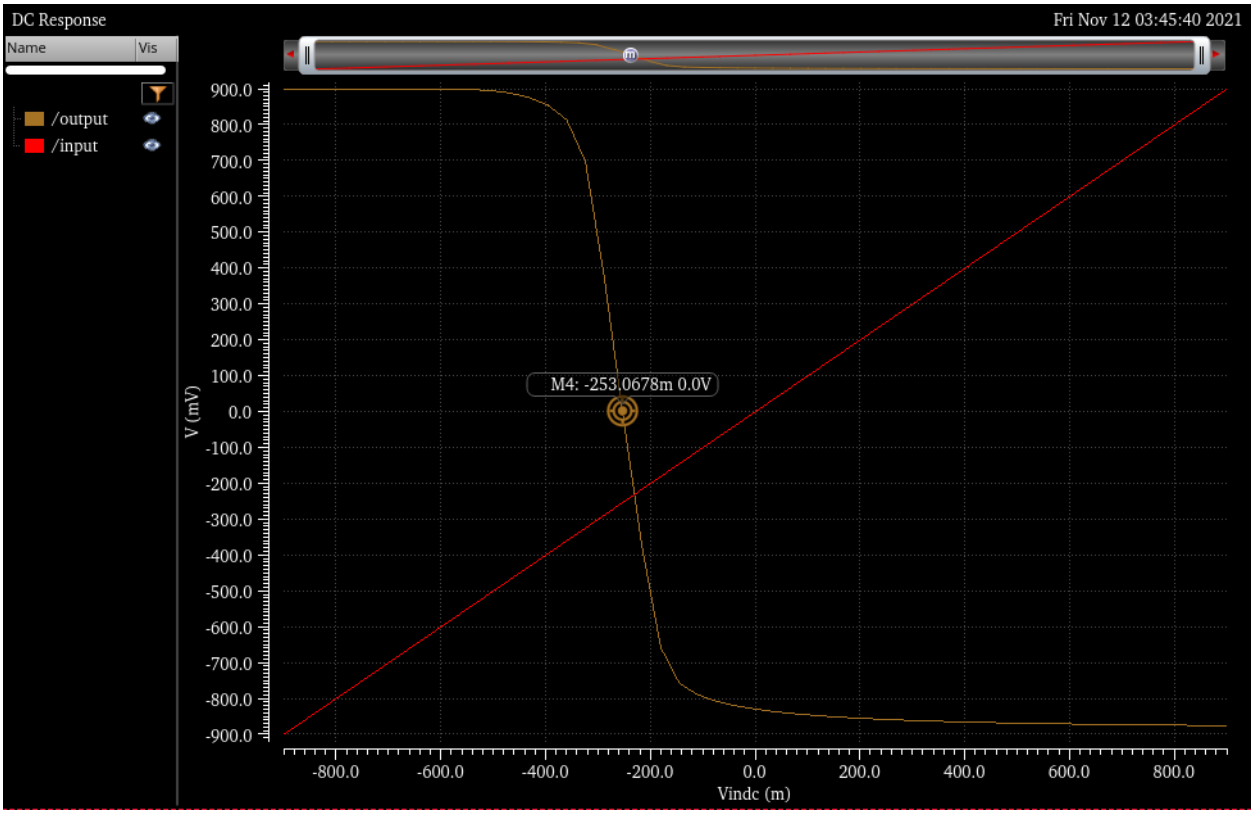


File Edit Options Windows

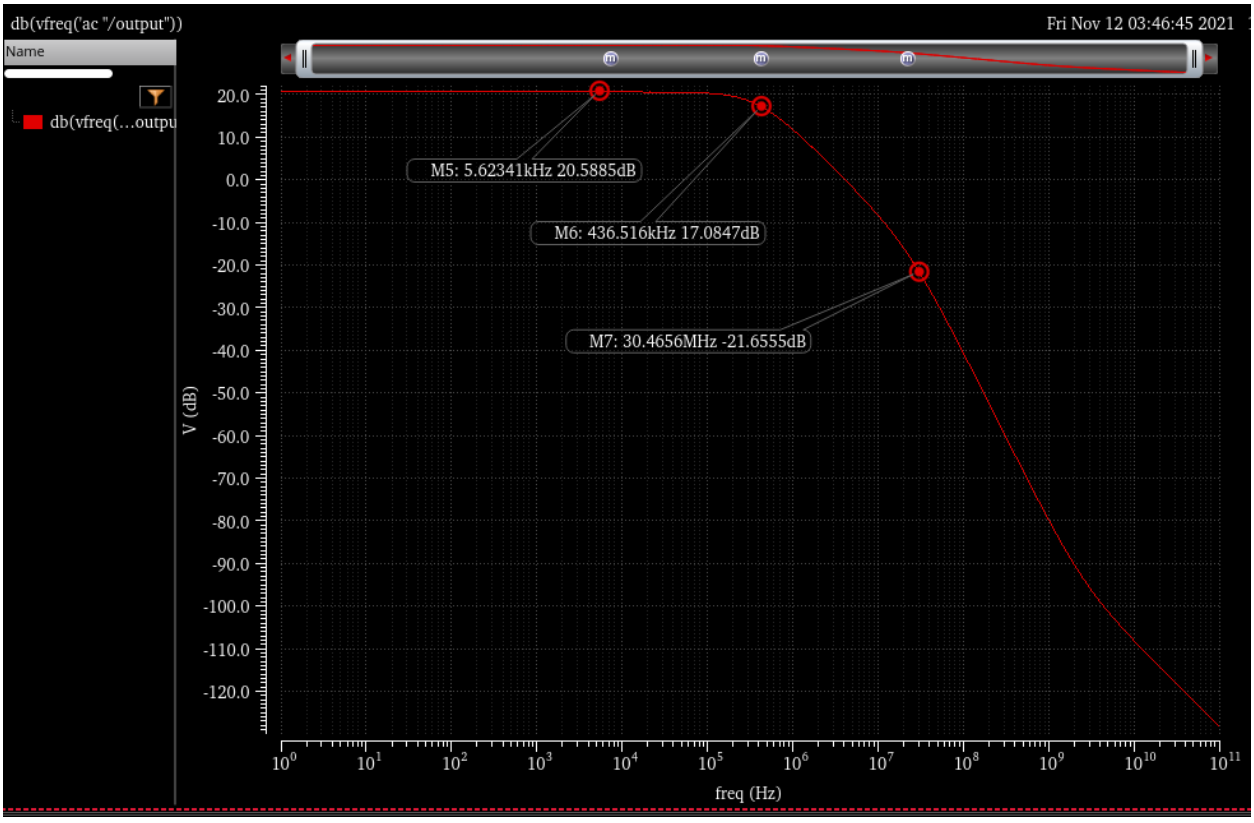
```
REPORT FILE NAME:          CurrentMirrorLoad.lvs.report
LAYOUT NAME:               /home/ugrads/m/matthewloden/CAL/CurrentMirrorLoad.sp (
SOURCE NAME:               /home/ugrads/m/matthewloden/LVS/CurrentMirrorLoad.netl
RULE FILE:                 /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:             Thu Nov 11 22:17:15 2021
CURRENT DIRECTORY:         /home/ugrads/m/matthewloden/CAL
USER NAME:                 matthewloden
CALIBRE VERSION:           v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                        OVERALL COMPARISON RESULTS


                  #       ####################
                    #     #                  #      _   _
                #   #     #     CORRECT      #       |
                  # #     #                  #      \___/
                    #     ####################
```

PostLayout Information:

DcOp:

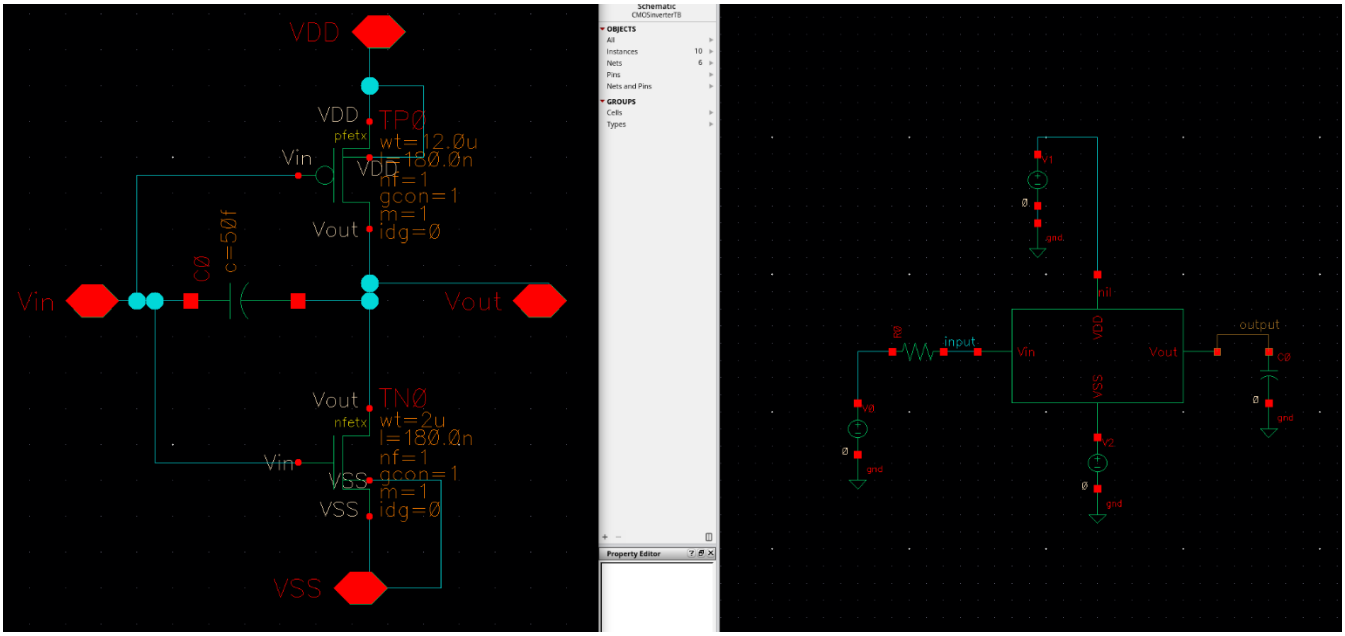


Av/Pole1/Pole2:



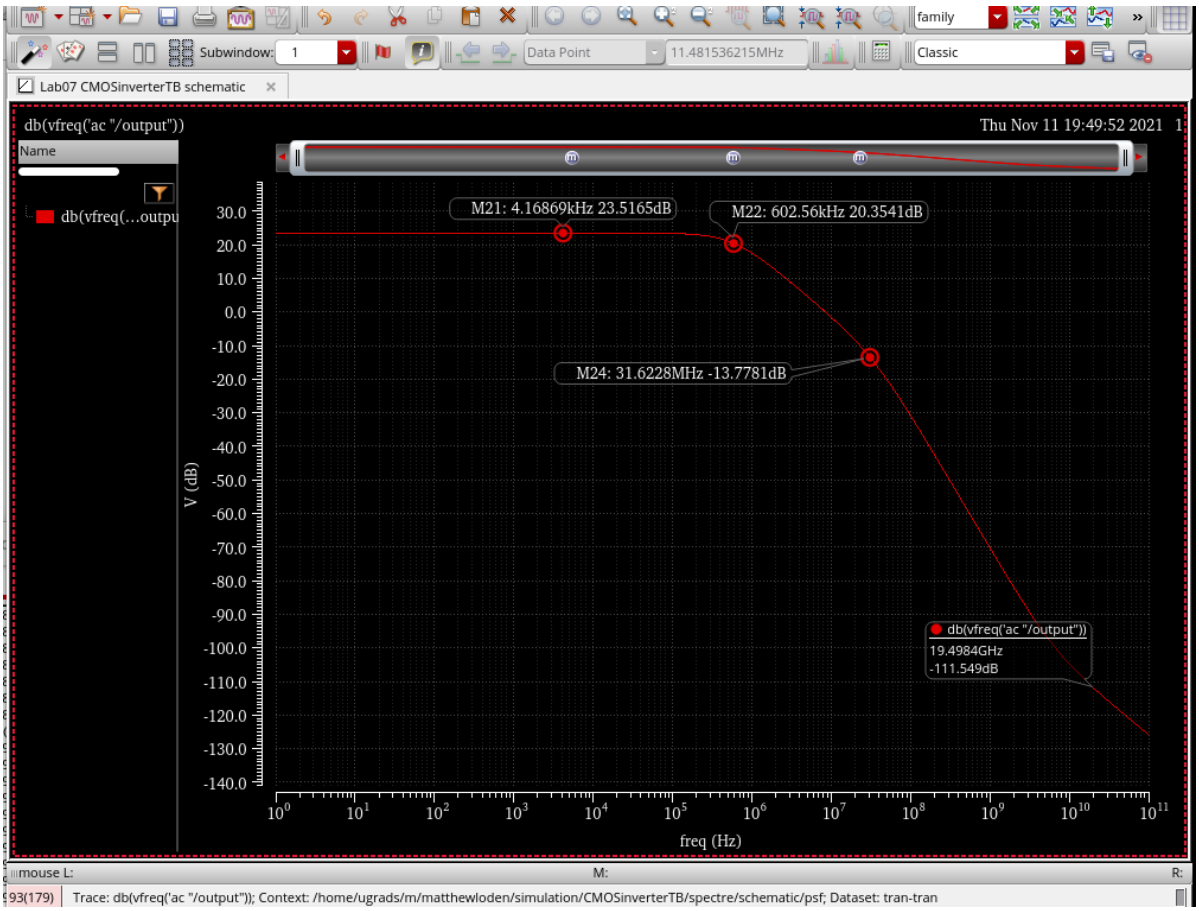
CMOS Inverter Information:

Schematic:

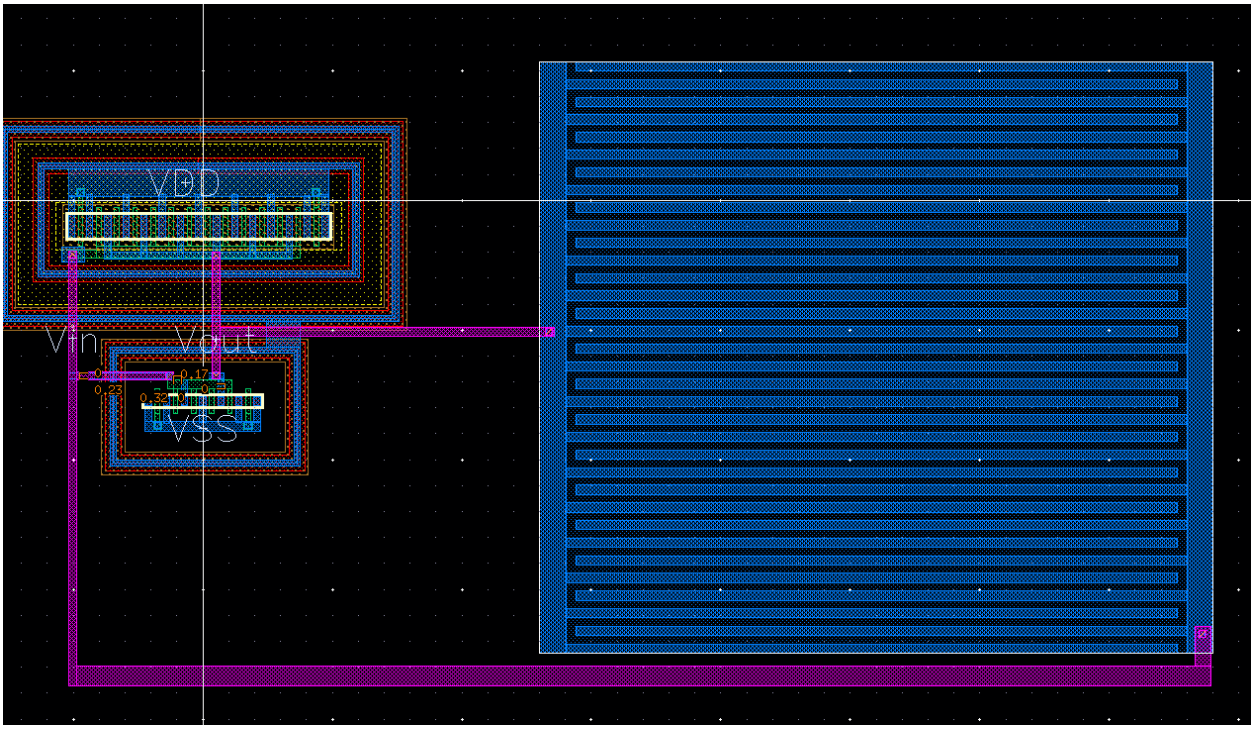


Dc Operation Point Curve:

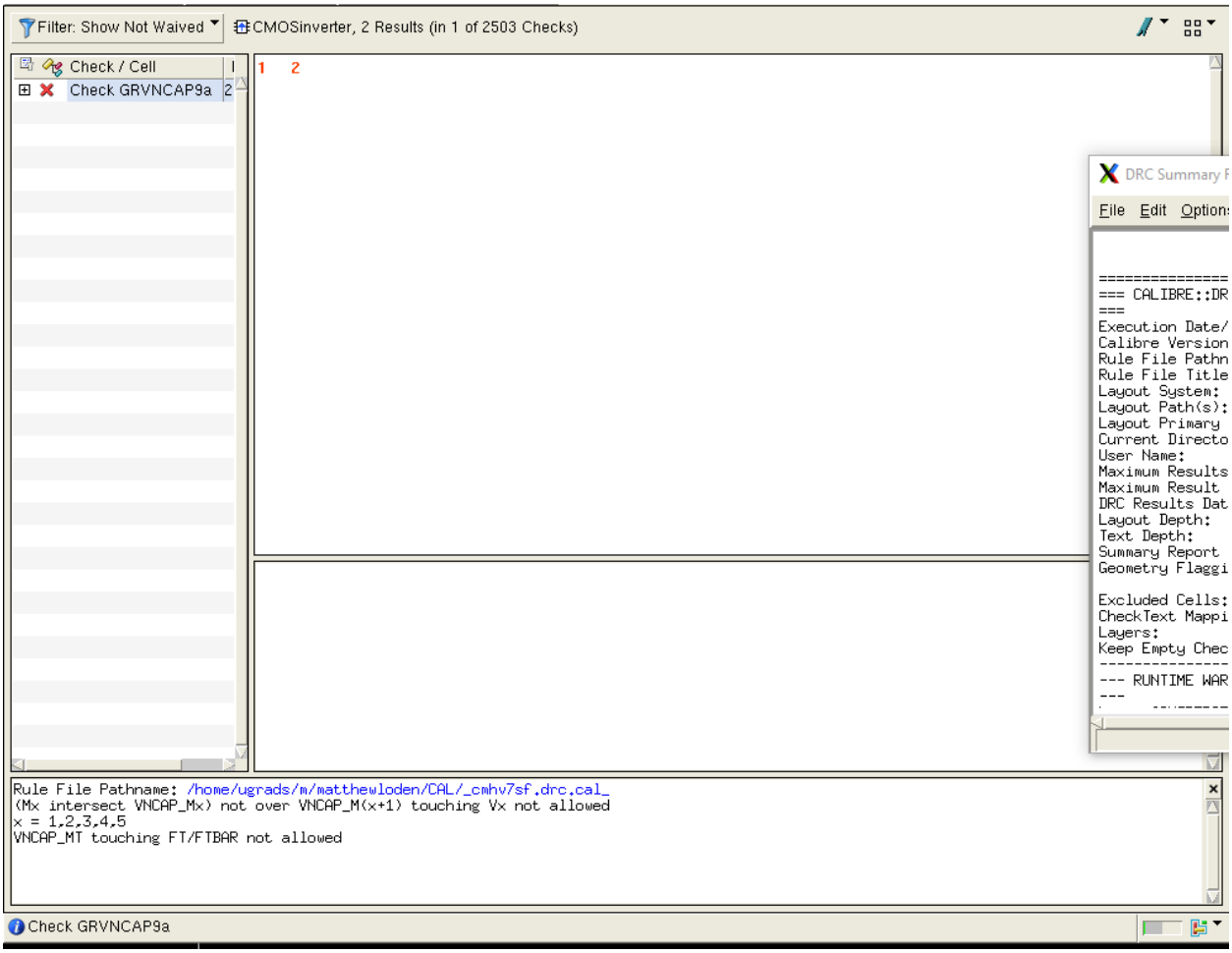
Gain/Pole1/Pole2:


Lab07 CMOSinverterTB schematic
db(vfreq("ac "/output"))
Thu Nov 11 19:49:52 2021
Name
db(vfreq(...outpu
M21: 4.16869kHz 23.5165dB
M22: 602.56kHz 20.3541dB
M24: 31.6228MHz -13.7781dB
db(vfreq("ac "/output"))
19.4984GHz
-111.549dB
V (dB)
freq (Hz)
mouse L:
M:
R:
Trace: db(vfreq("ac "/output")); Context: /home/ugrads/m/matthewloden/simulation/CMOSinverterTB/spectre/schematic/psf; Dataset: tran-tran

Layout:


VDD
Vin
Vout
Vss

DRC:

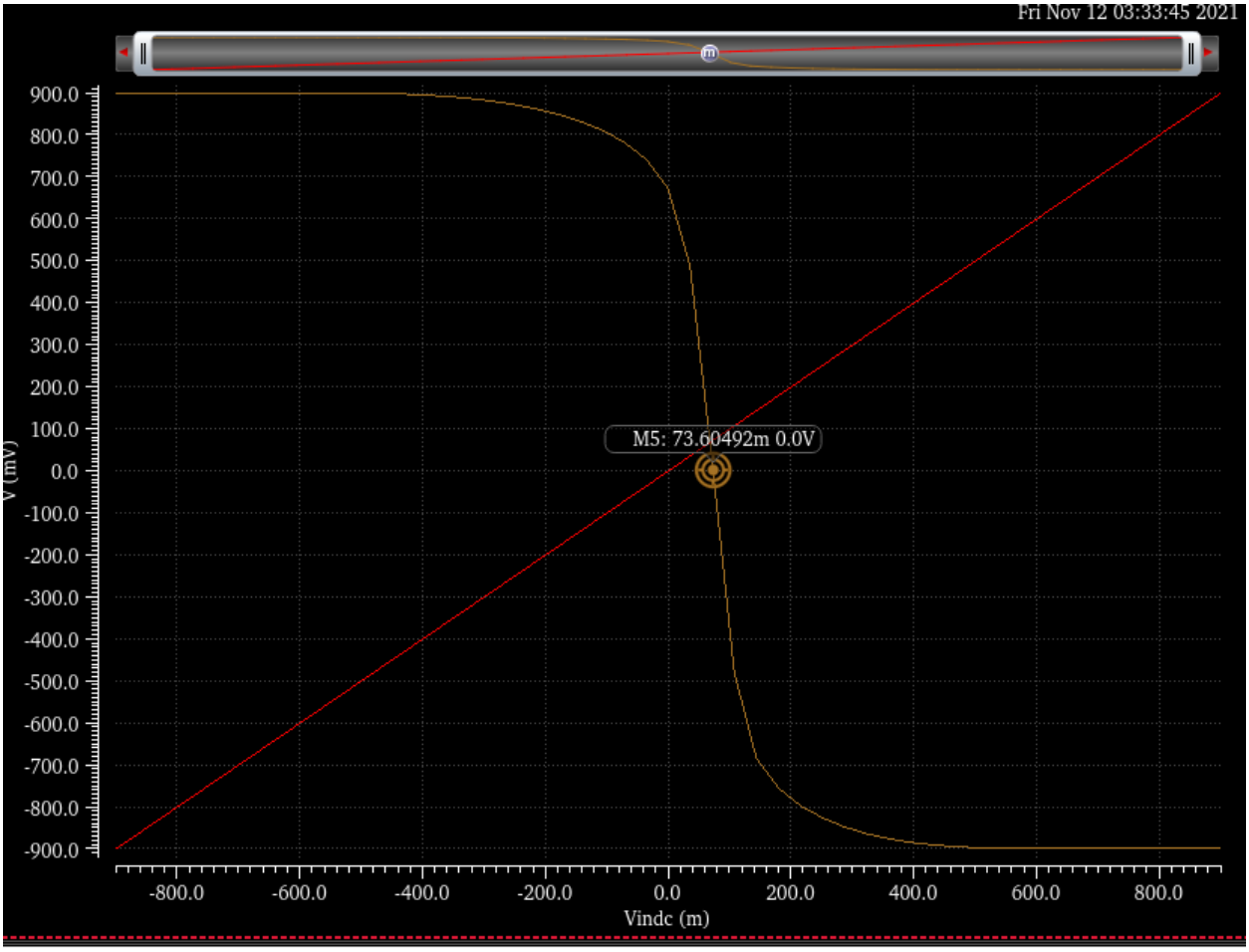

Filter: Show Not Waived
CMOSinverter, 2 Results (in 1 of 2503 Checks)
Check / Cell
Check GRVNCAP9a
1 2
DRC Summary
File Edit Option
=== CALIBRE::DR
Execution Date/
Calibre Version
Rule File Pathn
Rule File Title
Layout System:
Layout Path(s):
Layout Primary
Current Directo
User Name:
Maximum Results
Maximum Result
DRC Results Dat
Layout Depth:
Text Depth:
Summary Report
Geometry Flaggi
Excluded Cells:
CheckText Mappi
Layers:
Keep Empty Chec
--- RUNTIME WAR
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
(Mx intersect VNCAP_Mx) not over VNCAP_M(x+1) touching Vx not allowed
x = 1,2,3,4,5
VNCAP_MT touching FT/FTBAR not allowed
Check GRVNCAP9a

LVS:

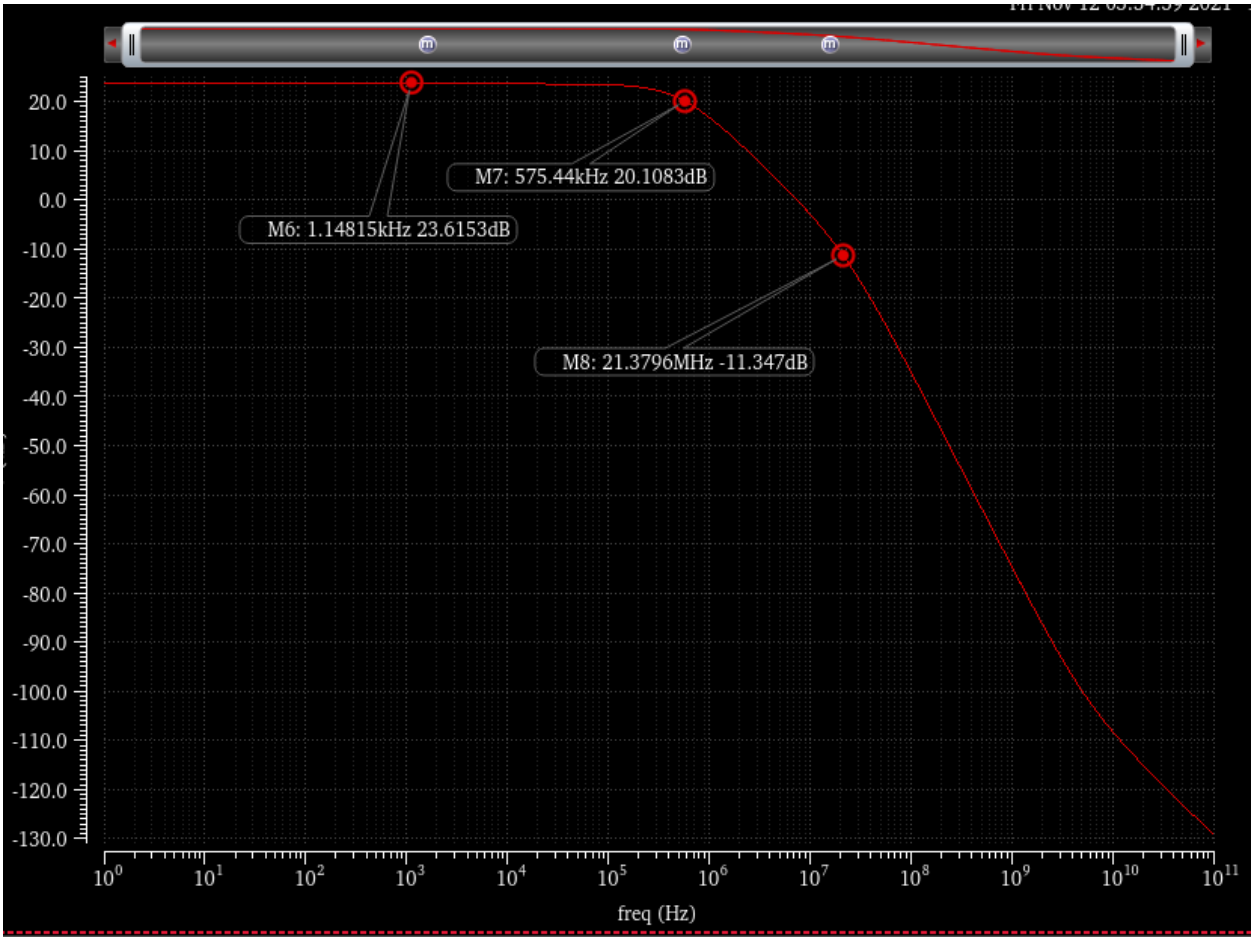
```
REPORT FILE NAME:         CMOSinverter.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/CMOSinverter.sp ('CMOS
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/CMOSinverter.netlist.l
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Fri Nov 12 01:17:43 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                              OVERALL COMPARISON RESULTS


                        #       ###################       _   _
                       #        #                 #       *   *
                  #   #         #     CORRECT     #         |
                   # #          #                 #       \___/
                    #           ###################
```

PostLayout Information:

DcOp:

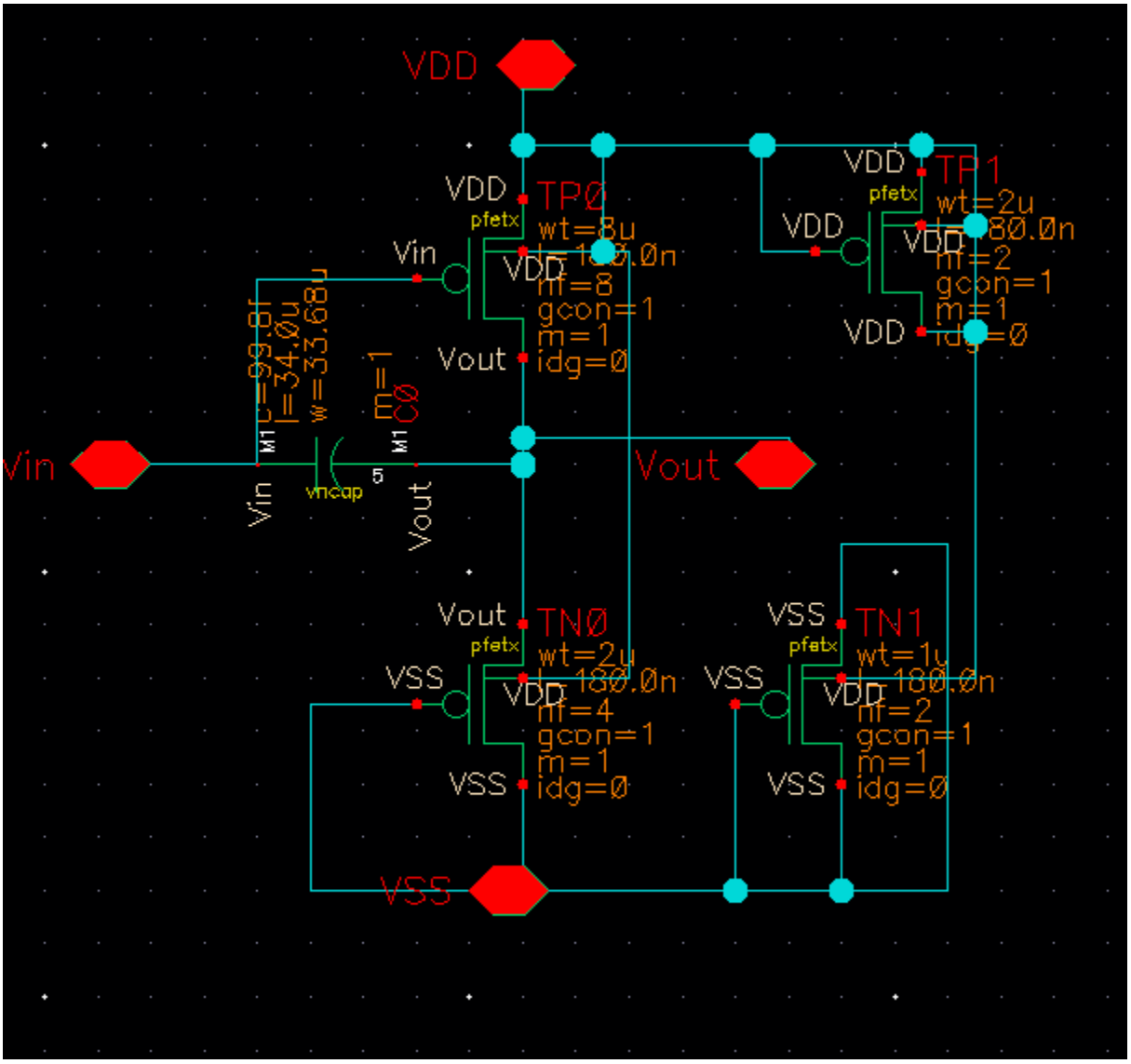


Av/Pole1/Pole2:

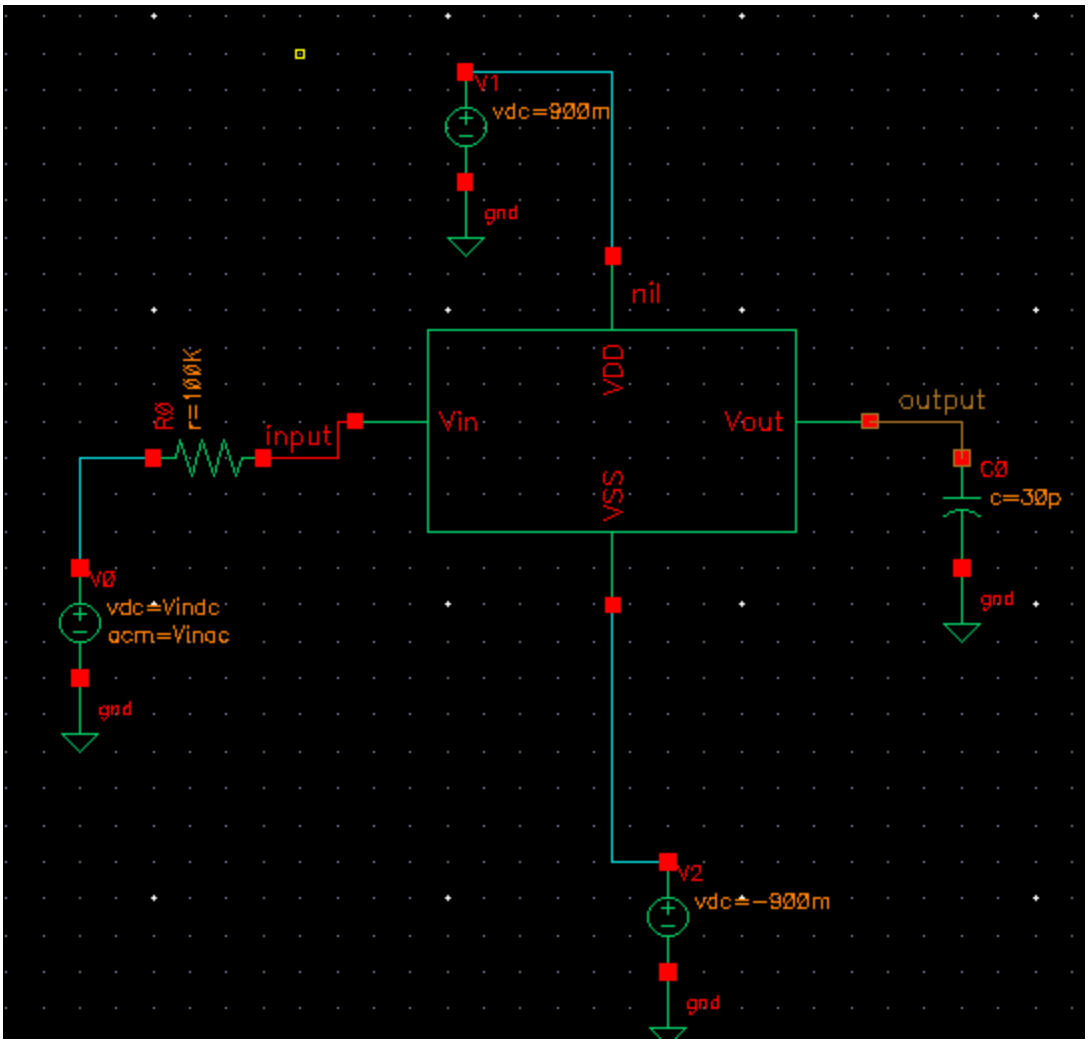

M7: 575.44kHz 20.1083dB
M6: 1.14815kHz 23.6153dB
M8: 21.3796MHz -11.347dB
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
-130.0
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
10^{11}
freq (Hz)

PMOS Biased Information:

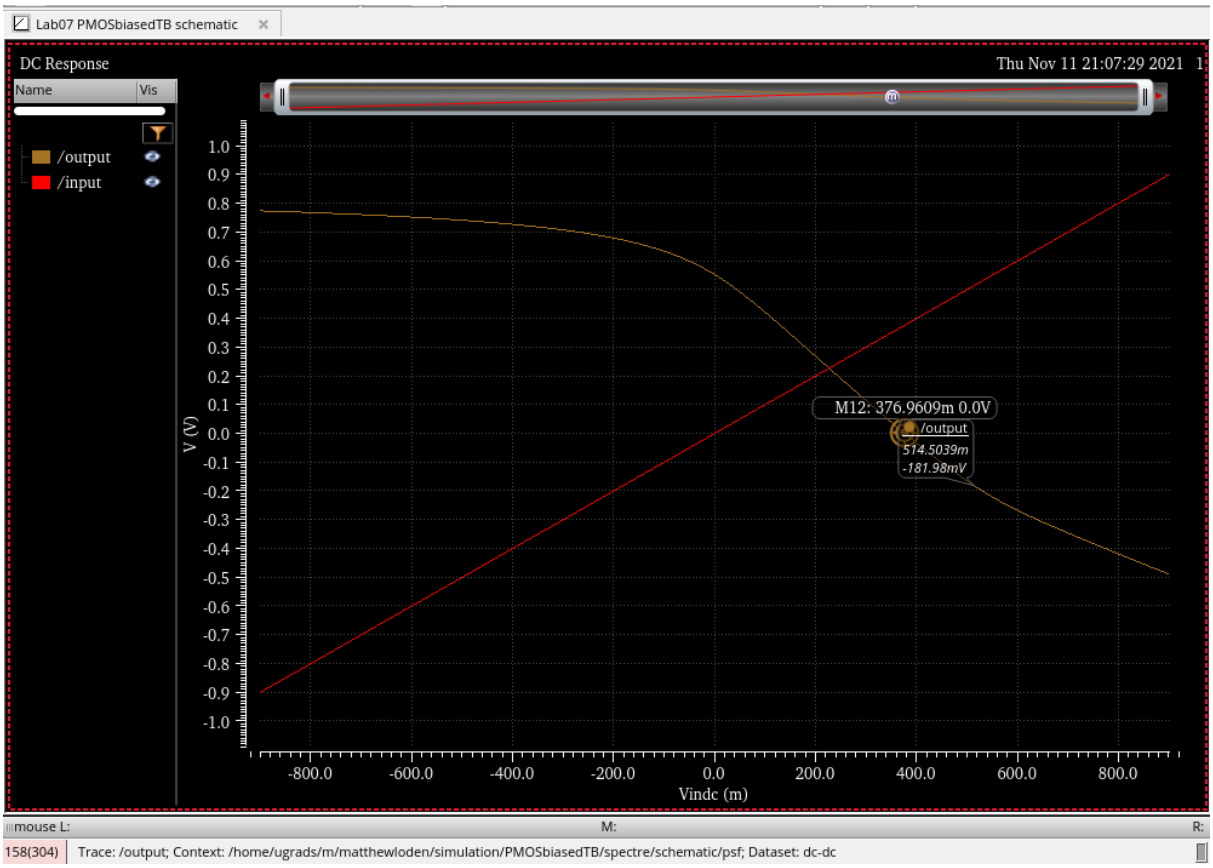
Schematic:



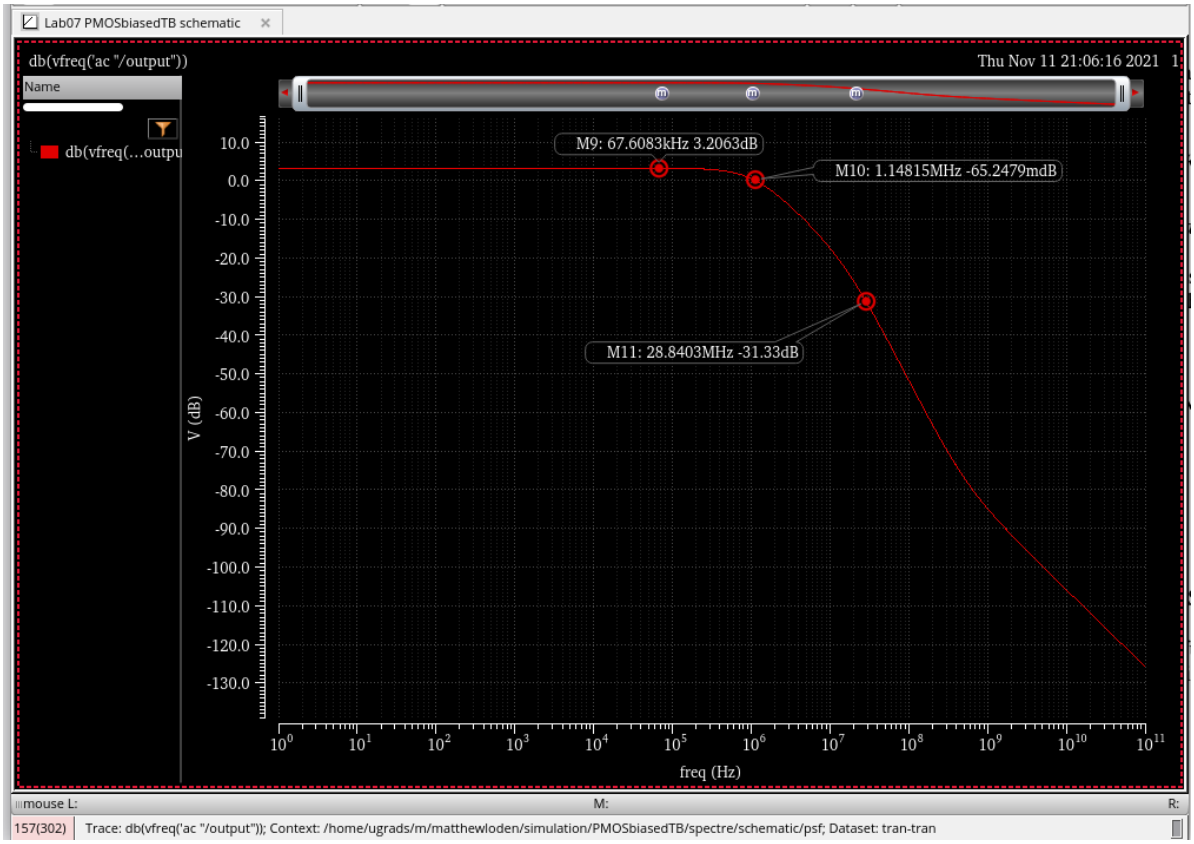
Test Bench:



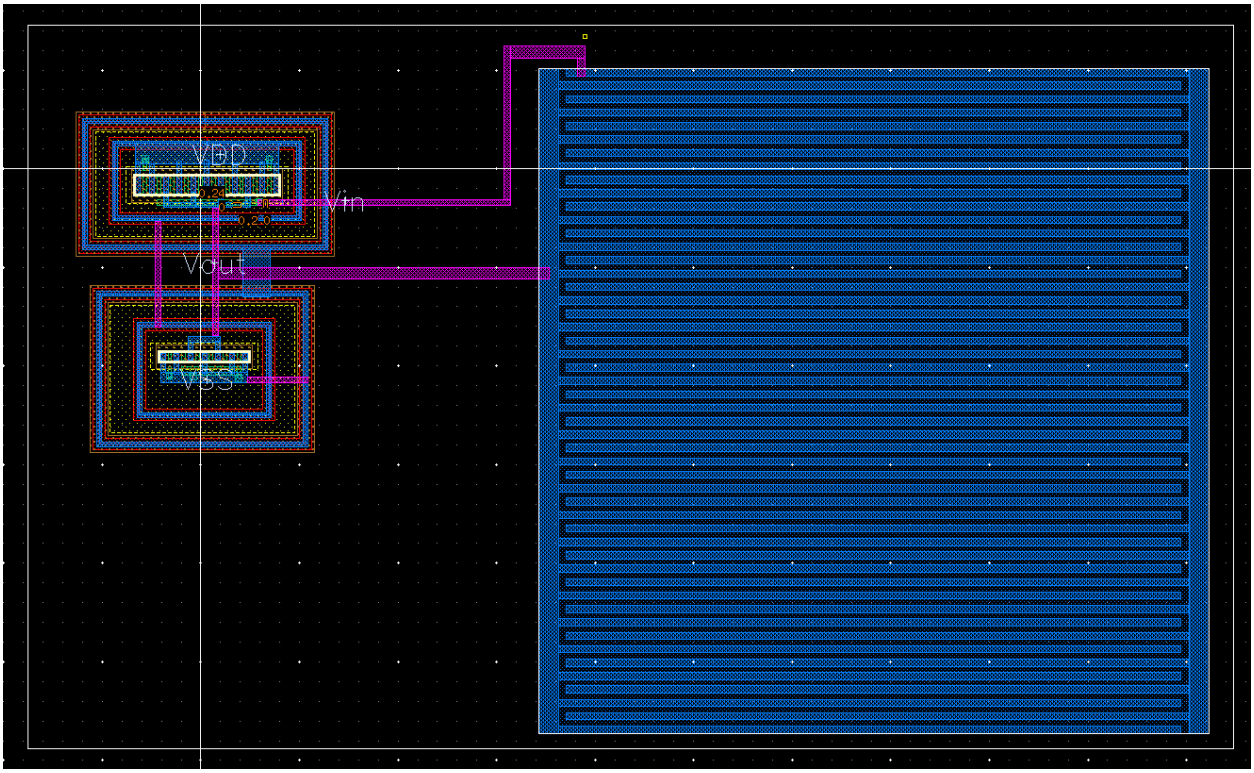
Dc Operation Point Curve:

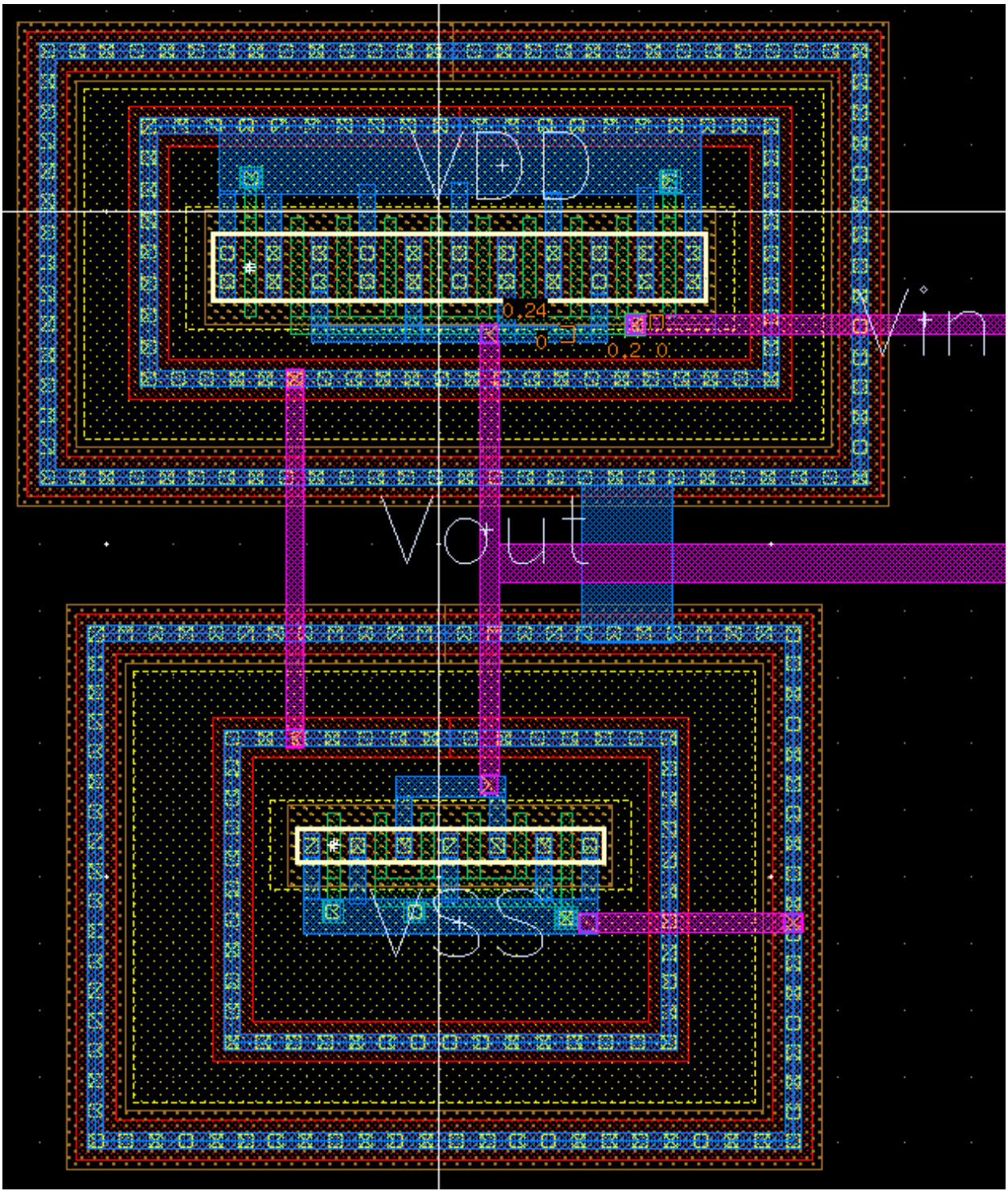


Gain/Pole1/Pole2:

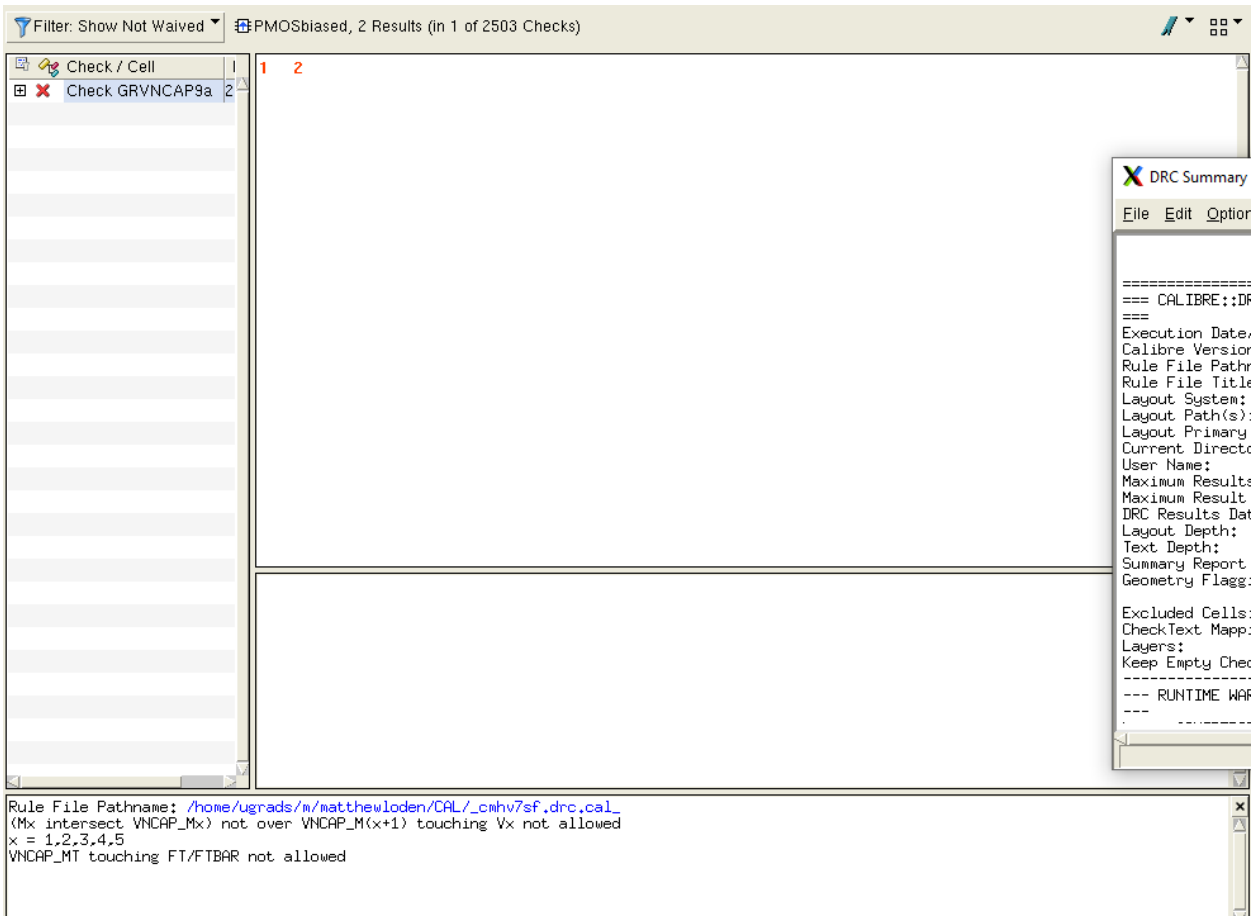

Lab07 PMOSbiasedTB schematic
db(vfreq('ac "/output"))
Thu Nov 11 21:06:16 2021
Name
db(vfreq(...outpu
M9: 67.6083kHz 3.2063dB
M10: 1.14815MHz -65.2479mdB
M11: 28.8403MHz -31.33dB
V (dB)
freq (Hz)
mouse L:
M:
R:
157(302)
Trace: db(vfreq('ac "/output")); Context: /home/ugrads/m/matthewloden/simulation/PMOSbiasedTB/spectre/schematic/psf; Dataset: tran-tran

Layout:


VDD
Vin
Vout
VSS



DRC:

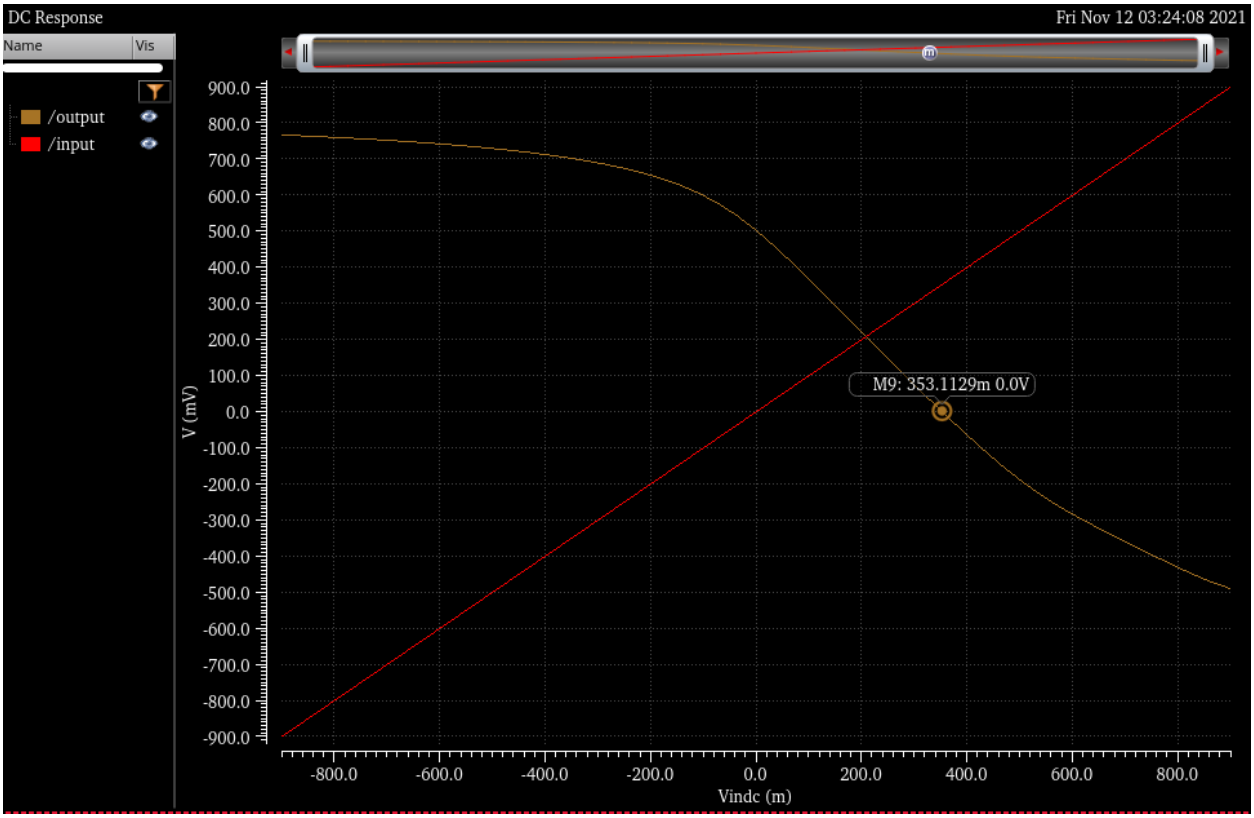

Filter: Show Not Waived
PMOSbiased, 2 Results (in 1 of 2503 Checks)
Check / Cell
Check GRVNCAP9a
1 2
DRC Summary
File Edit Optior
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
(Mx intersect VNCAP_Mx) not over VNCAP_M(x+1) touching Vx not allowed
x = 1,2,3,4,5
VNCAP_MT touching FT/FTBAR not allowed

LVS:

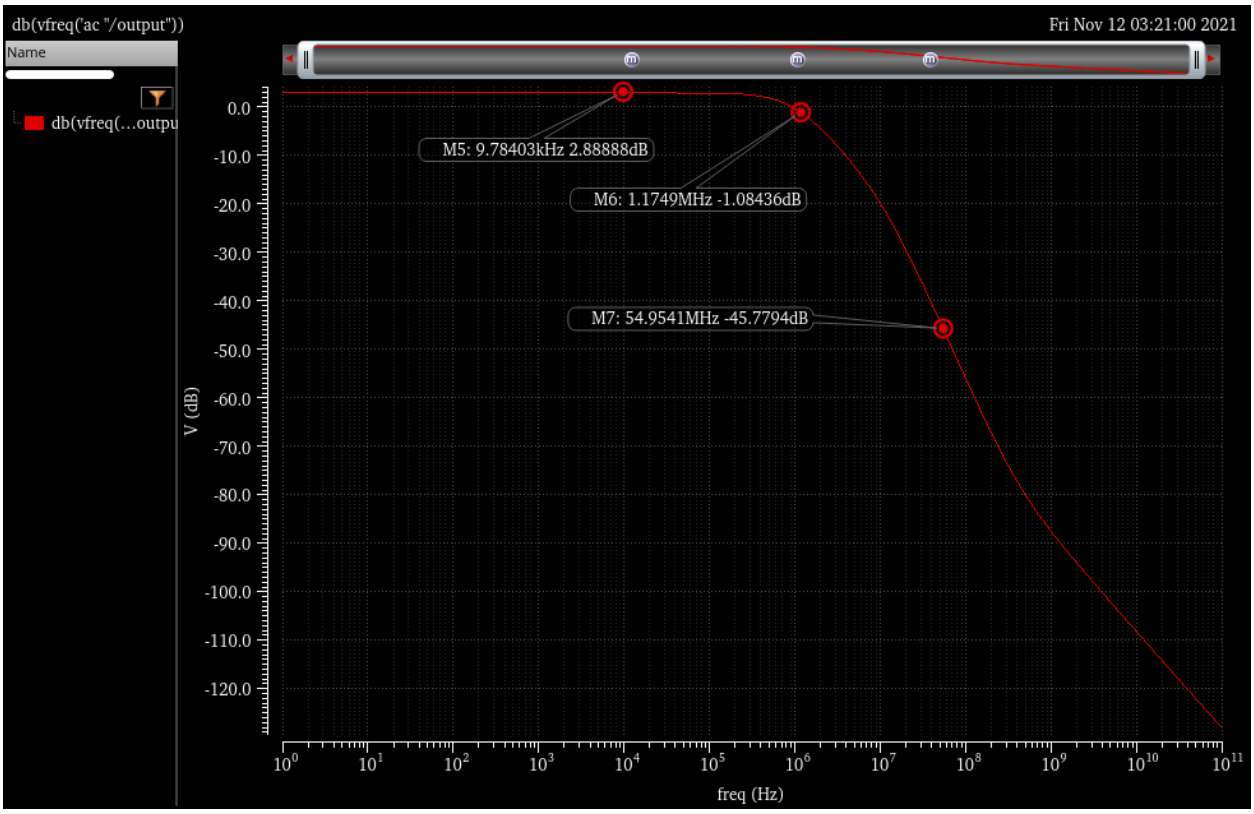
```
                ##                                                  ##
                ######################################################


REPORT FILE NAME:         PMOSbiased.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/PMOSbiased.sp ('PMOSbi
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/PMOSbiased.netlist.lvs
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Fri Nov 12 02:16:13 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                              OVERALL COMPARISON RESULTS


                       #       ####################       _   _
                     #         #                  #       *   *
                  #    #       #     CORRECT      #         |
                   # #         #                  #       \___/
                    #          ####################
```

PostLayout Information:

DcOp:

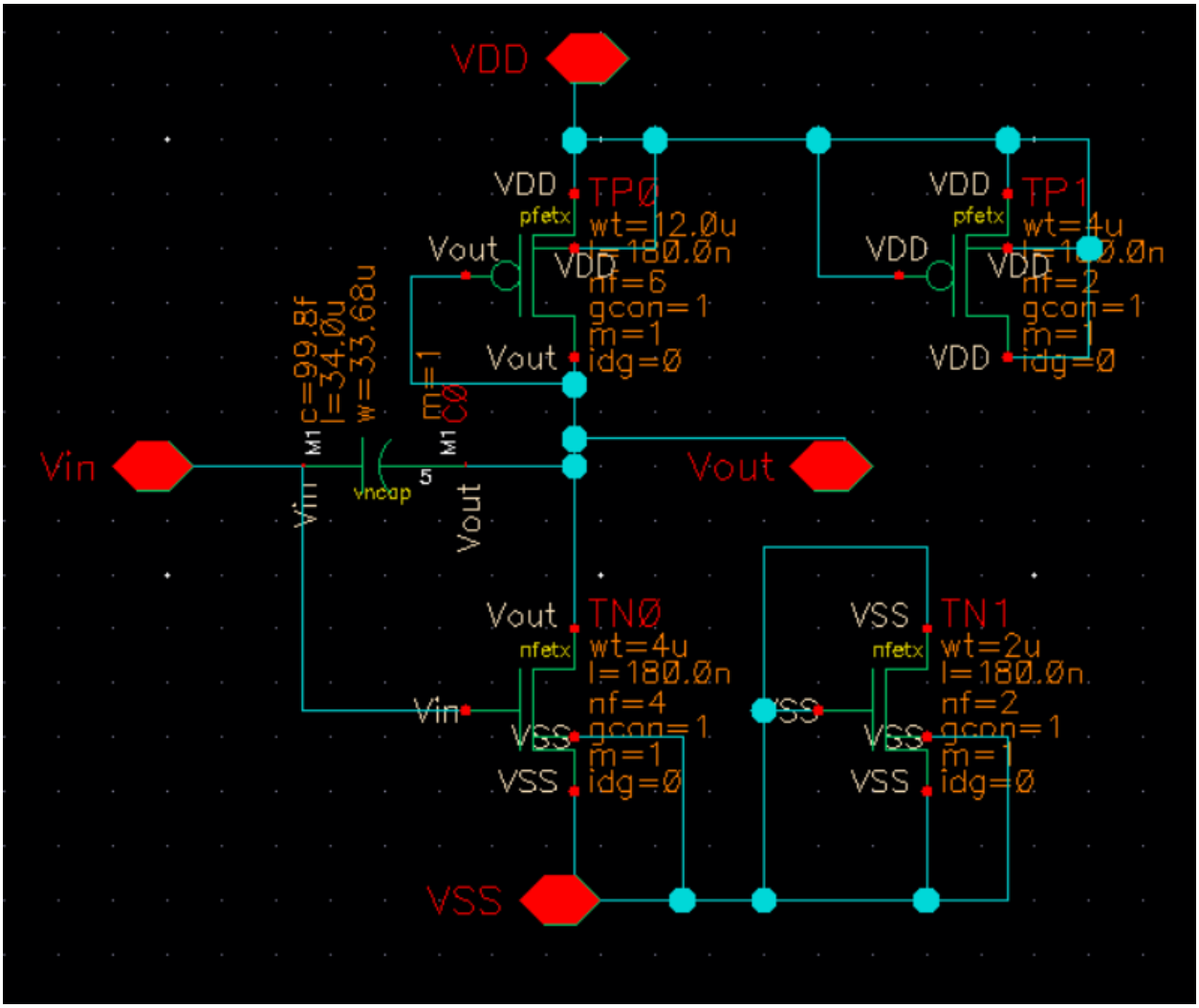


Av/Pole1/Pole2:

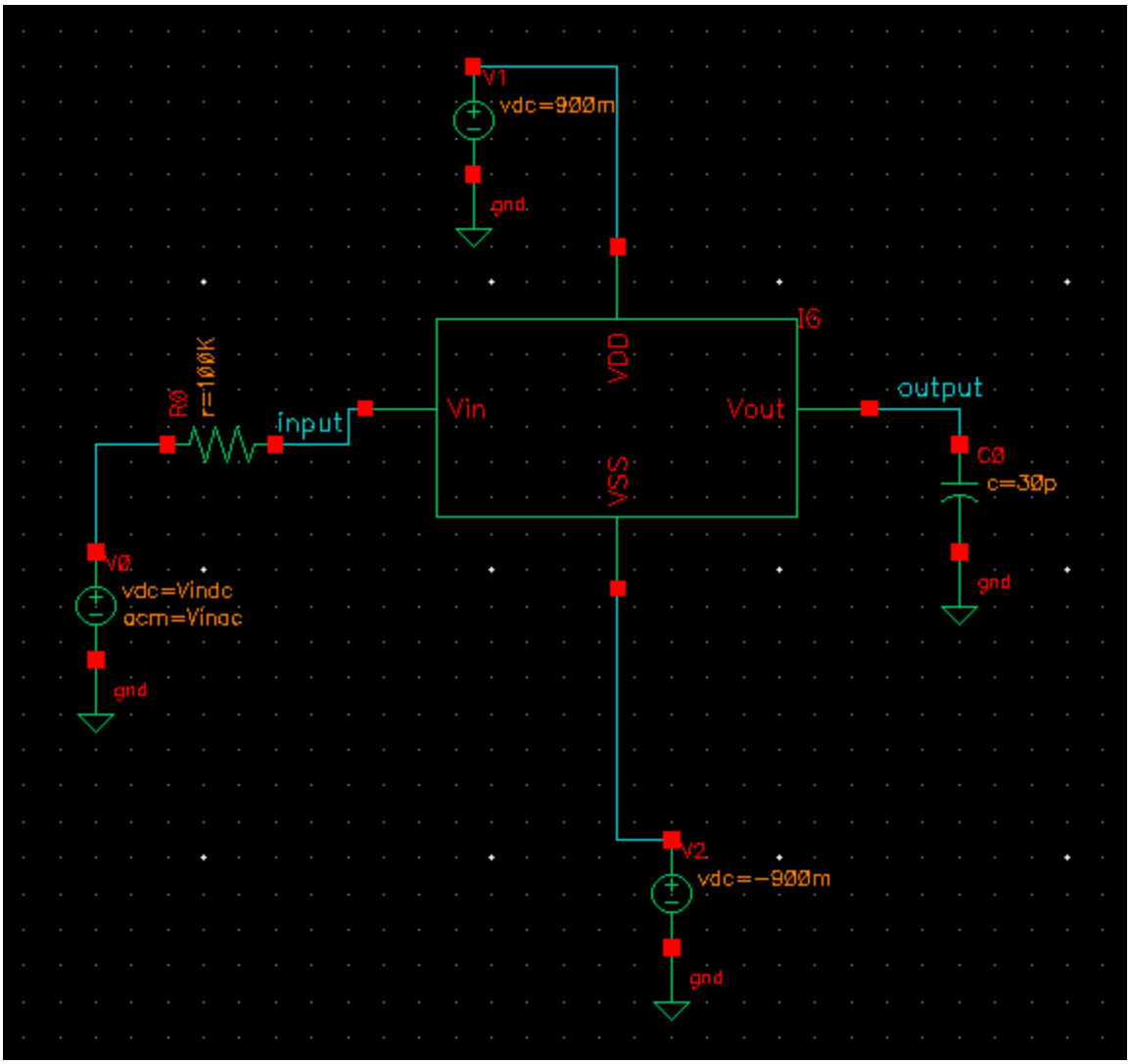

db(vfreq('ac "/output"))
Fri Nov 12 03:21:00 2021
Name
db(vfreq(...outpu
M5: 9.78403kHz 2.88888dB
M6: 1.1749MHz -1.08436dB
M7: 54.9541MHz -45.7794dB
V (dB)
freq (Hz)

CMOS Biased Information:

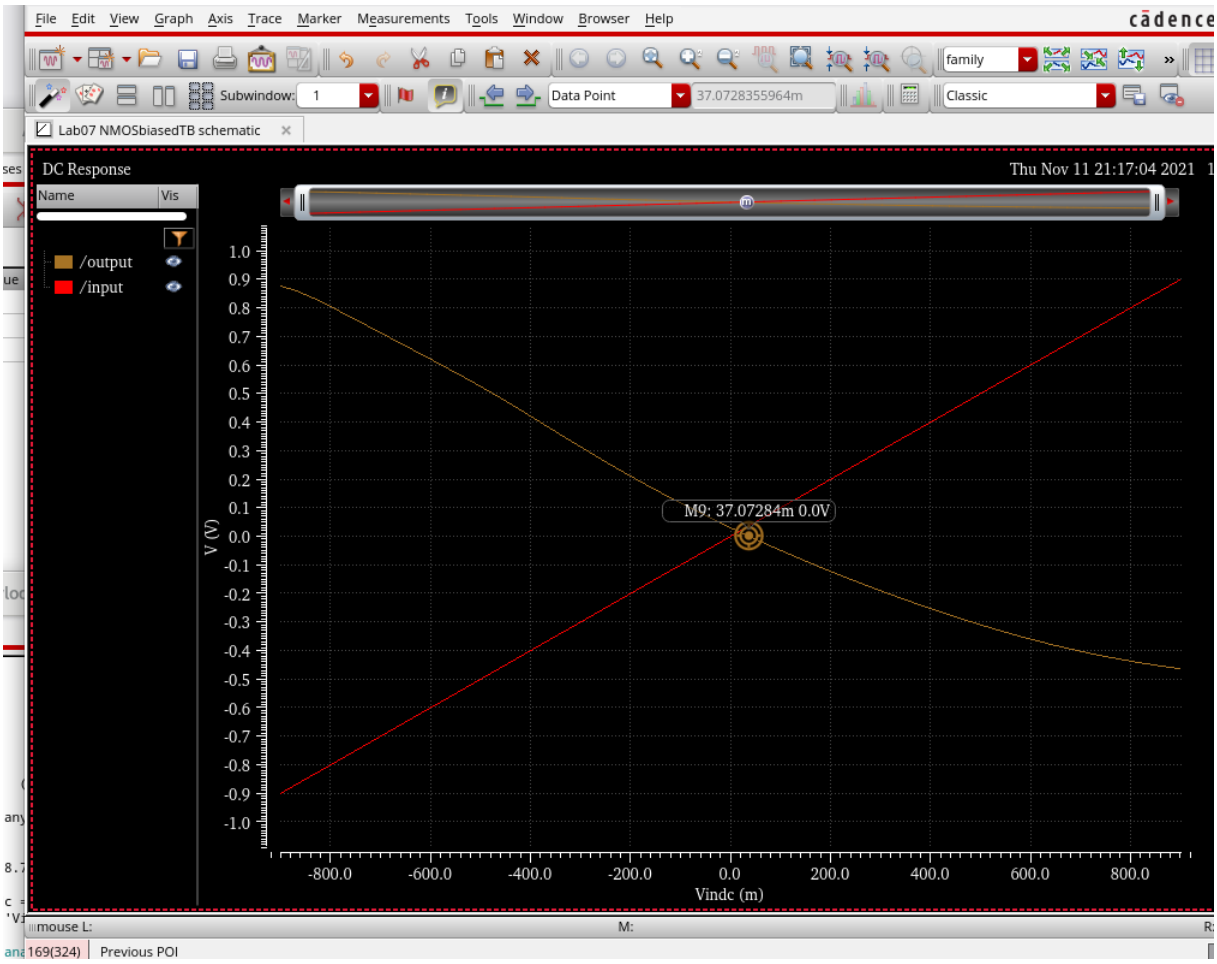
Schematic:



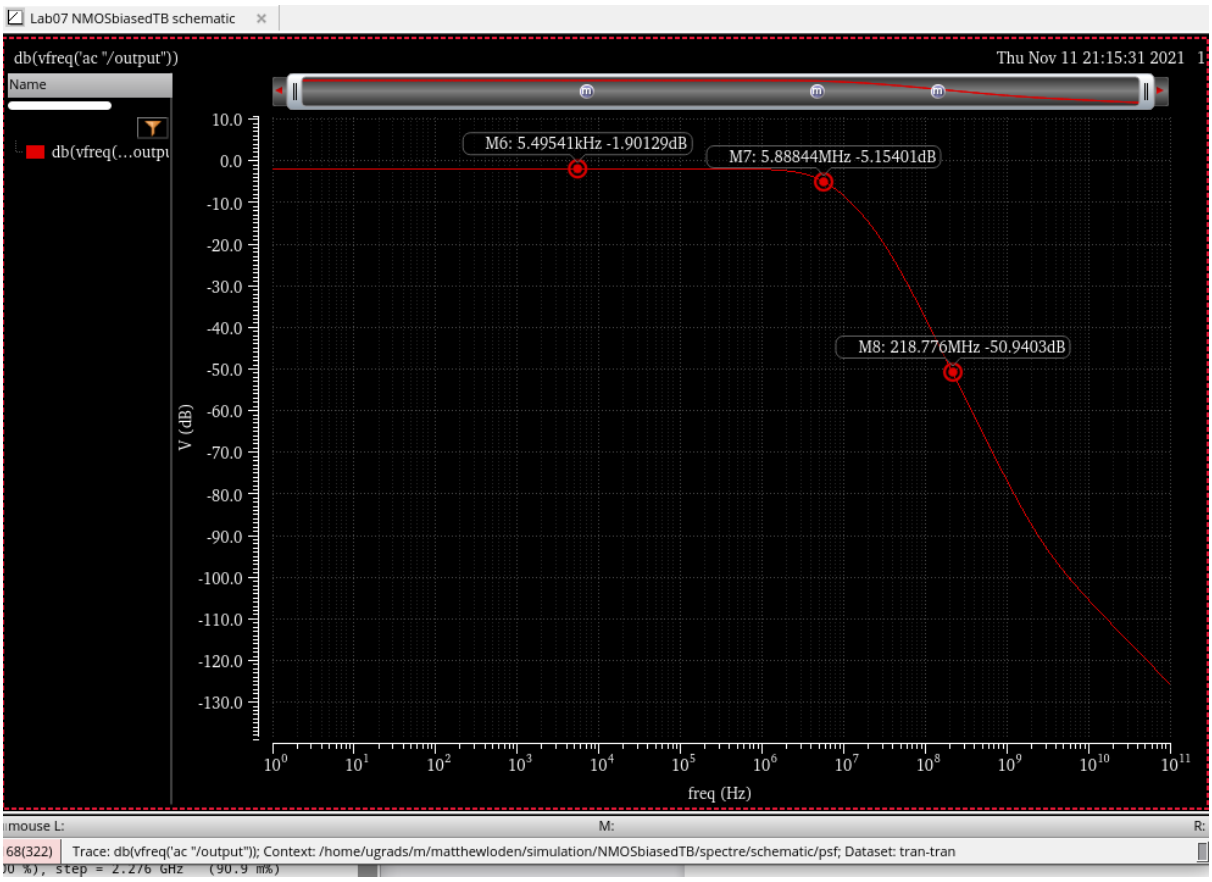
Test Bench:



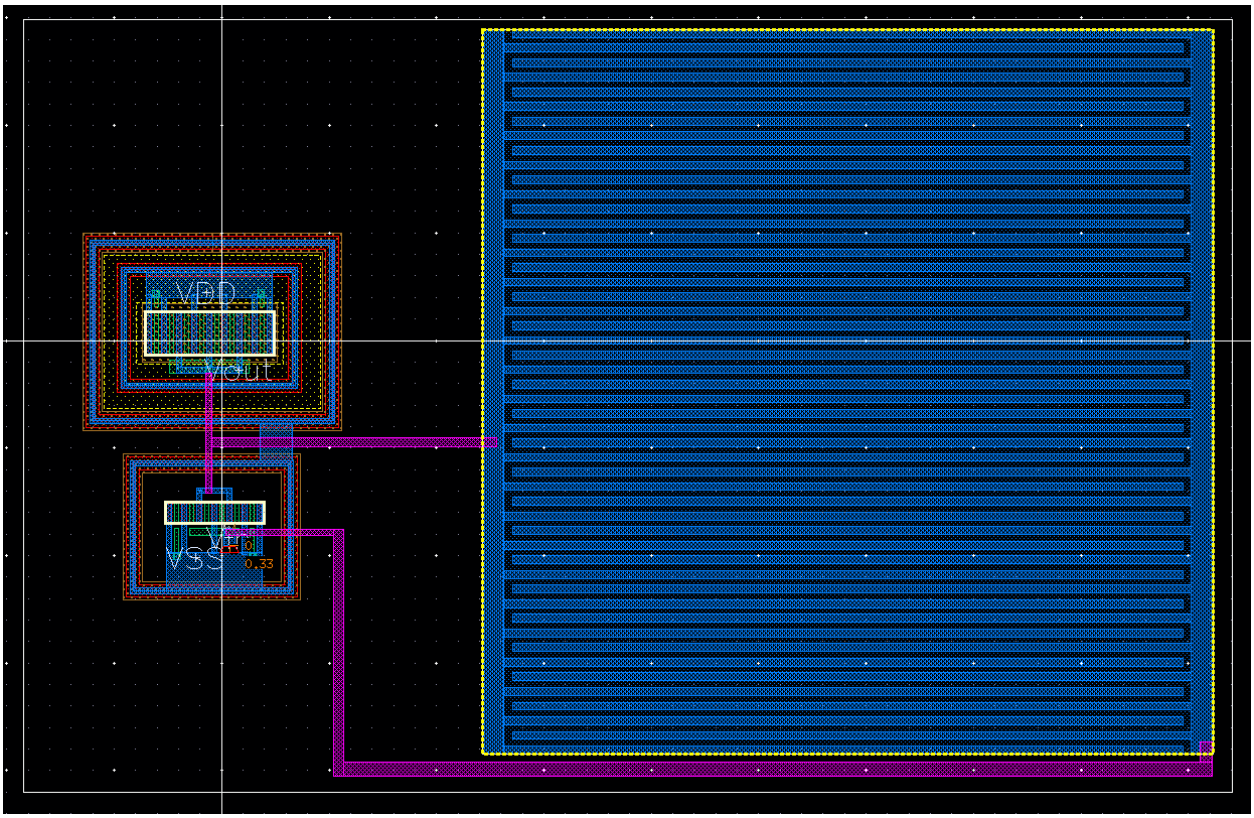
Dc Operation Point Curve:

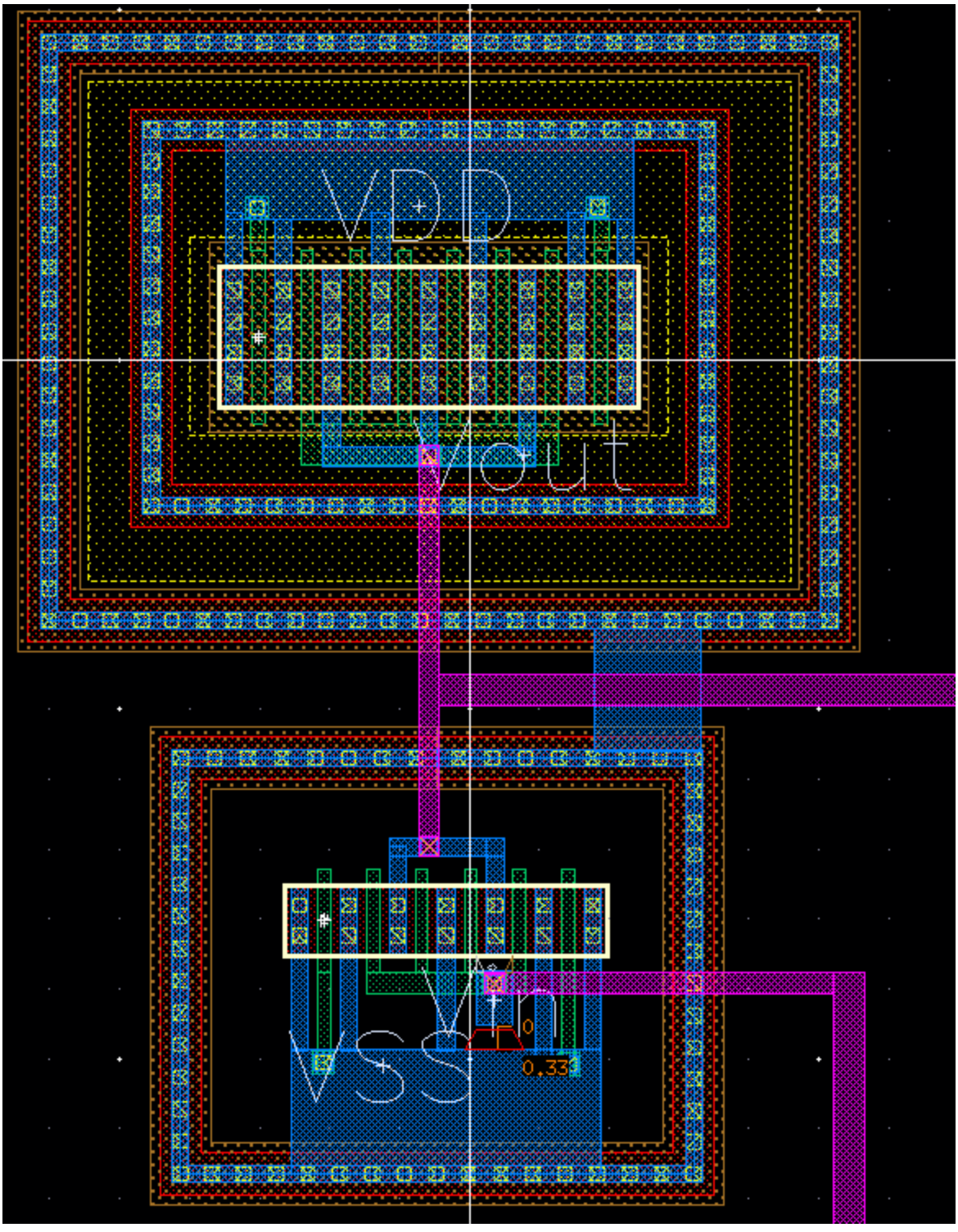


Gain/Pole1/Pole2:

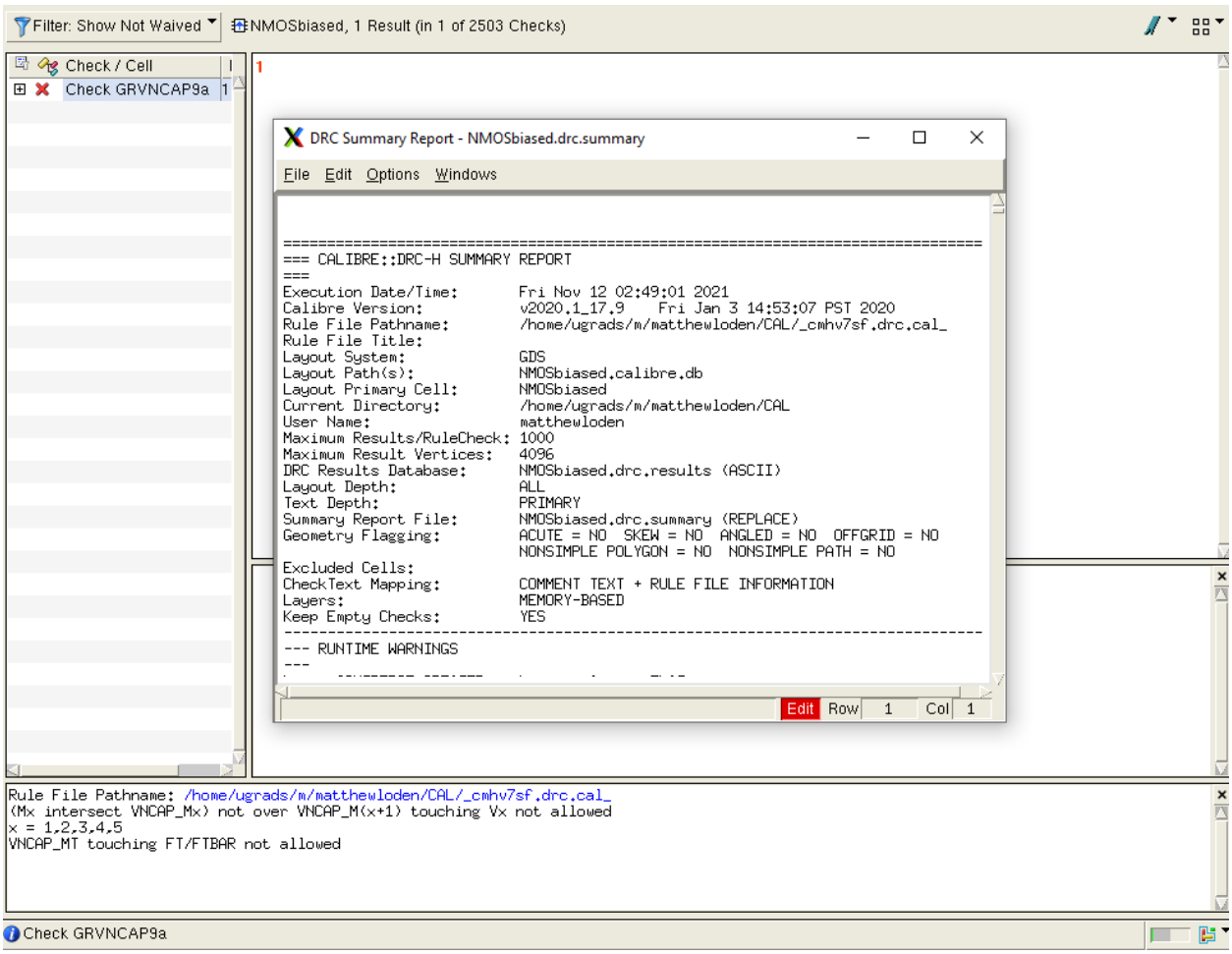

Lab07 NMOSbiasedTB schematic
db(vfreq('ac "/output"))
Thu Nov 11 21:15:31 2021
Name
db(vfreq(...outpu
M6: 5.49541kHz -1.90129dB
M7: 5.88844MHz -5.15401dB
M8: 218.776MHz -50.9403dB
V (dB)
freq (Hz)
mouse L:
M:
R:
68(322)
Trace: db(vfreq('ac "/output")); Context: /home/ugrads/m/matthewloden/simulation/NMOSbiasedTB/spectre/schematic/psf; Dataset: tran-tran

Layout:


VDD
Vout
VSS
0.33



DRC:

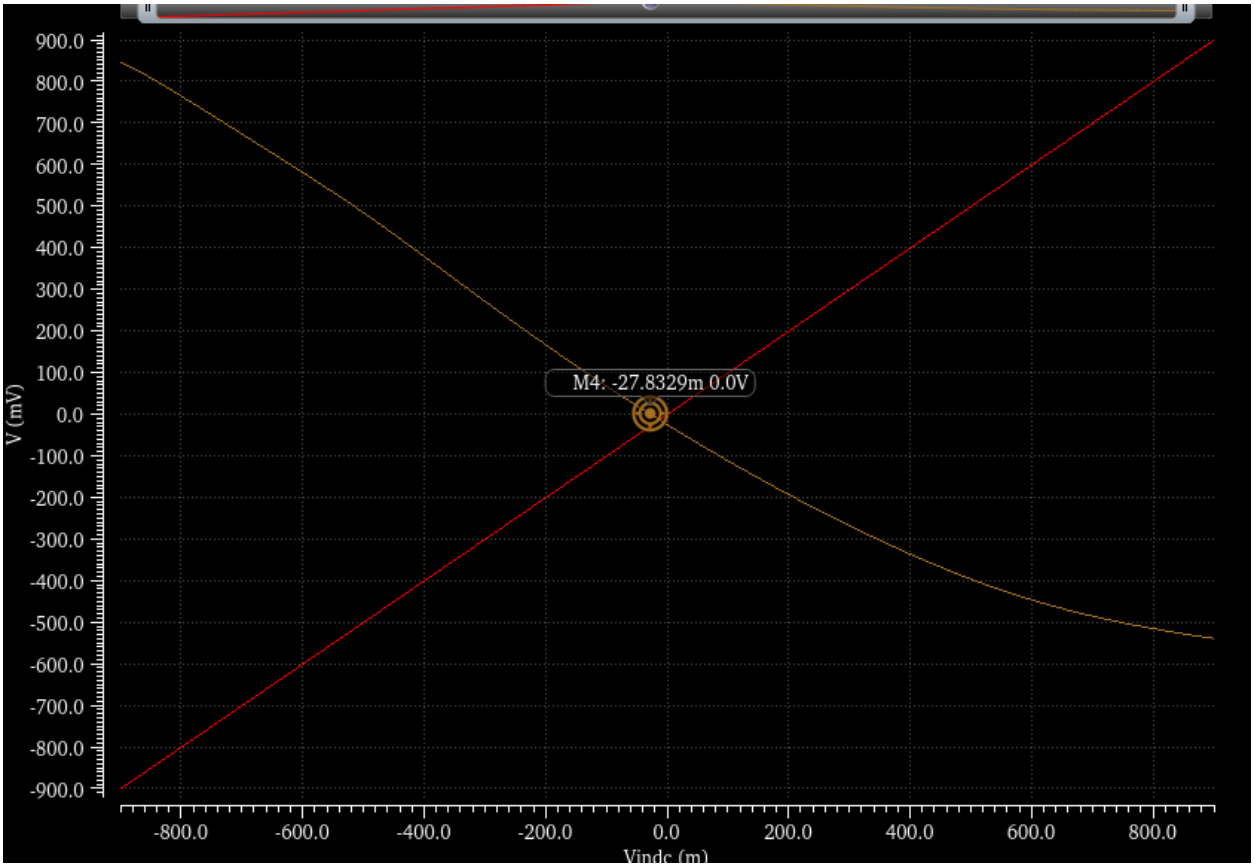

Filter: Show Not Waived
NMOSbiased, 1 Result (in 1 of 2503 Checks)
Check / Cell
Check GRVNCAP9a
DRC Summary Report - NMOSbiased.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Nov 12 02:49:01 2021
Calibre Version: v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
Rule File Title:
Layout System: GDS
Layout Path(s): NMOSbiased.calibre.db
Layout Primary Cell: NMOSbiased
Current Directory: /home/ugrads/m/matthewloden/CAL
User Name: matthewloden
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: NMOSbiased.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: NMOSbiased.drc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
Edit Row 1 Col 1
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
(Mx intersect VNCAP_Mx) not over VNCAP_M(x+1) touching Vx not allowed
x = 1,2,3,4,5
VNCAP_MT touching FT/FTBAR not allowed
Check GRVNCAP9a

LVS:

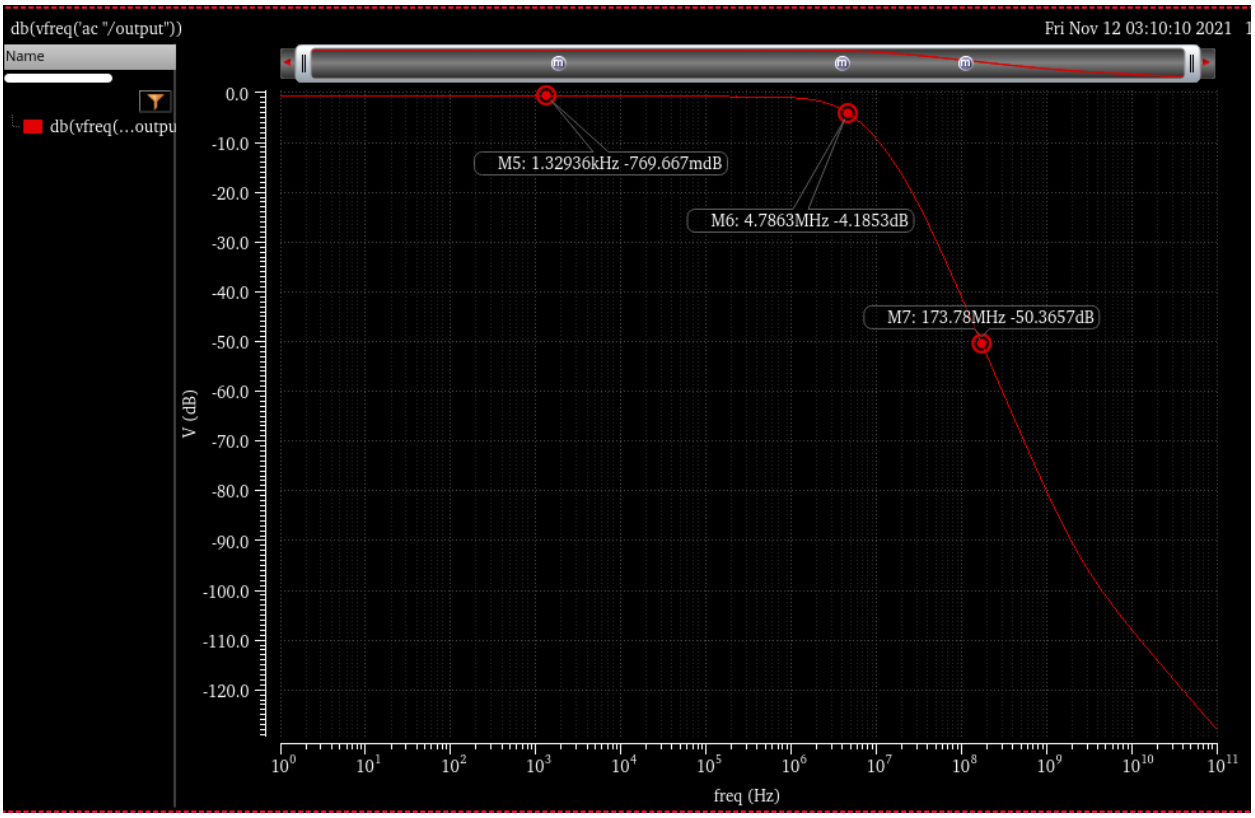
```
                  ##                                                  ##
                  ######################################################


REPORT FILE NAME:         NMOSbiased.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/NMOSbiased.sp ('NMOSbi
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/NMOSbiased.netlist.lvs
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Fri Nov 12 02:57:12 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                              OVERALL COMPARISON RESULTS


                        #       ###################       _   _
                       #        #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################
```

PostLayout Information:

DcOp:



Av/Pole1/Pole2:


db(vfreq('ac "/output"))
Fri Nov 12 03:10:10 2021
Name
db(vfreq(...outpu
M5: 1.32936kHz -769.667mdB
M6: 4.7863MHz -4.1853dB
M7: 173.78MHz -50.3657dB
V (dB)
freq (Hz)

Data Discussed

Lab09, PreLayout	Av	P1	P2	GBW
Current Mirror Load	23.5165dB	60255kHz	30.690MHz	8.96MHz
CMOS Inverter	23.5165dB	602.56kHz	31.6288MHz	9.02MHz
PMOS Biased	3.206dB	1.148MHz	28.403MHz	1.66MHz
CMOS Self Biased	-1.901dB	5.888MHz	218.77MHz	4.73MHz

PostLab	Av	P1	P2	GBW
CML	20.5885dB	436.516kHz	30.4656MHz	4.6711MHz
CMOS I	23.6153dB	575.44kHz	21.3796MHz	8.709MHz
PMOS B	2.8888dB	1.1749MHz	54.9541MHz	1.638MHz
CMOS B	-769mdB	4.7863MHz	173.78MHz	4.3MHz

In this lab, may different data points were taken. Most data points met the requirements laid out in the lab manual. The major differences came in the Gain of the inverters. The unity gain values were very close to the expected values however the 30dB mark was unattainable for my designs. The Gain Bandwidth was still met due to the pole frequency being large enough to compensate for the lower gain. All pole two frequencies were three times larger than the related pole one frequency so we can safely assume all poles were stable.