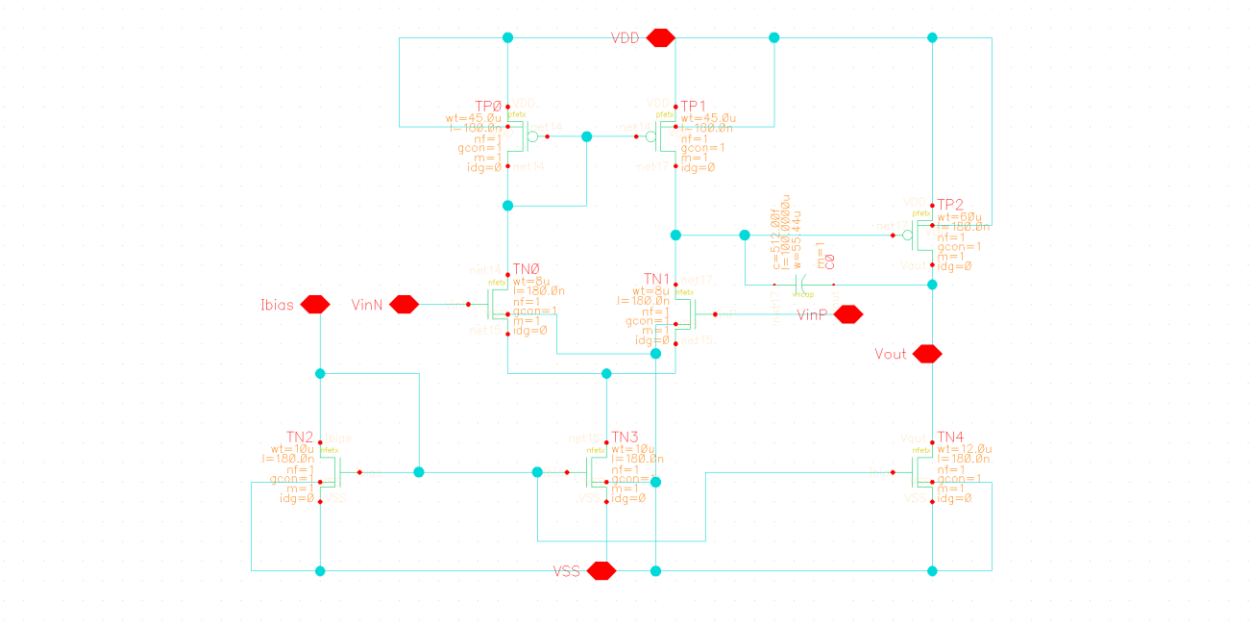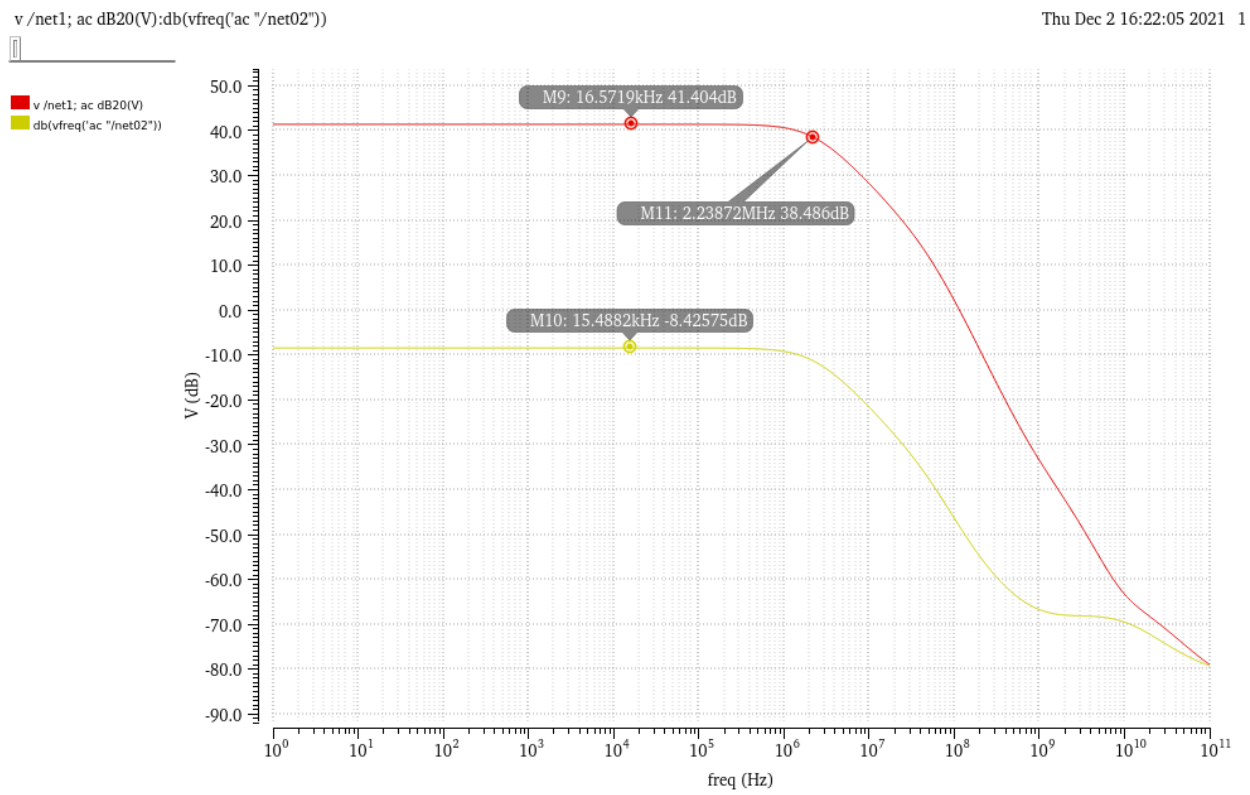Matthew Loden

ECEN 474

Lab 09: Miller Operational Amplifier

Schematic:

Pre-Layout Data:

Av0:

Acm: -8.425dB   Pole 1: 2.23MHz   Adm: 41.404dB   Pole 2 ~~ 25MHz

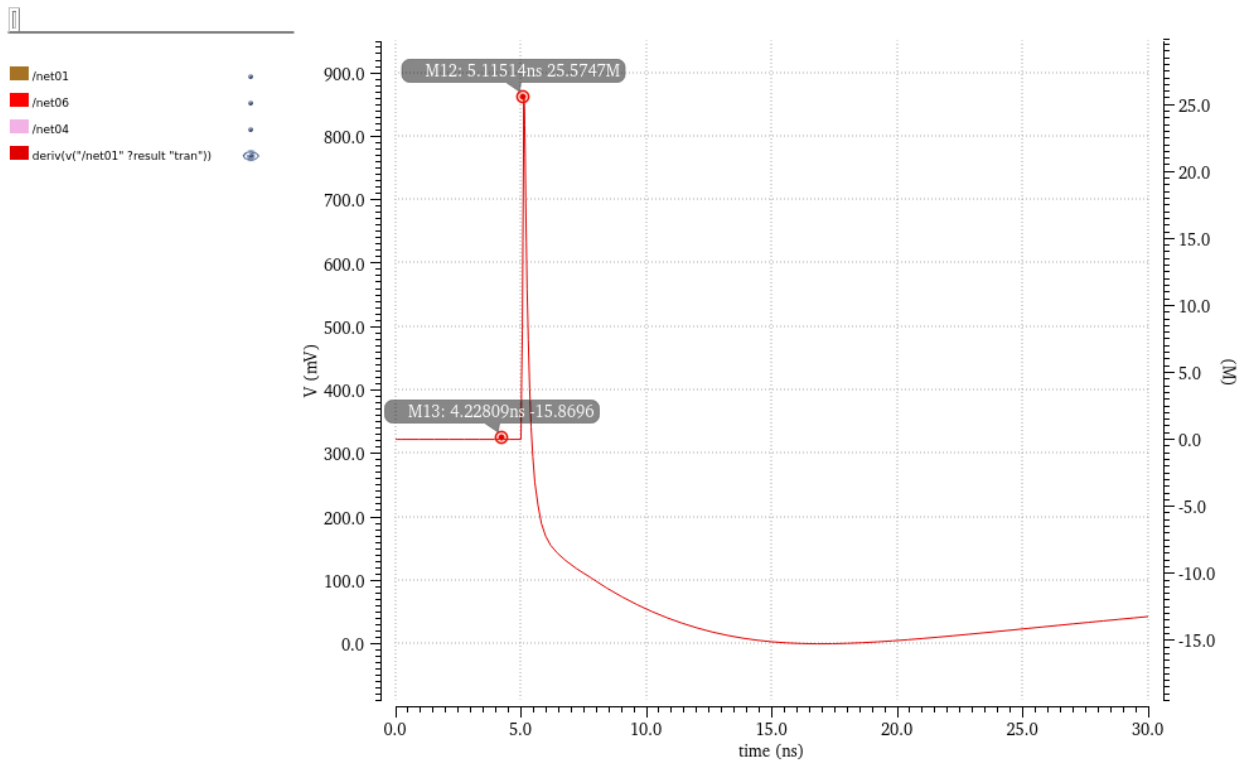CMRR: 49.829dB   GBW: 92.33MHz   Phase Margin ~~ 40°

Power Consumed: 550uW

6	OP("/I0/TP0" "region")	2	☐	☐
7	OP("/I0/TN0" "region")	2	☐	☐
8	OP("/I0/TN1" "region")	2	☐	☐
9	OP("/I0/TN2" "region")	2	☐	☐
10	OP("/I0/TN3" "region")	2	☐	☐
11	OP("/I0/TN4" "region")	2	☐	☐
12	(((- OP("/V0" "i")) - OP("/I1" "i")) * 1.8)	550u	☐	☐
13	db(vfreq('ac "/net02"))	wave	☐	☐

Plot after simulation: Auto ▼   Plotting mode: Replace ▼
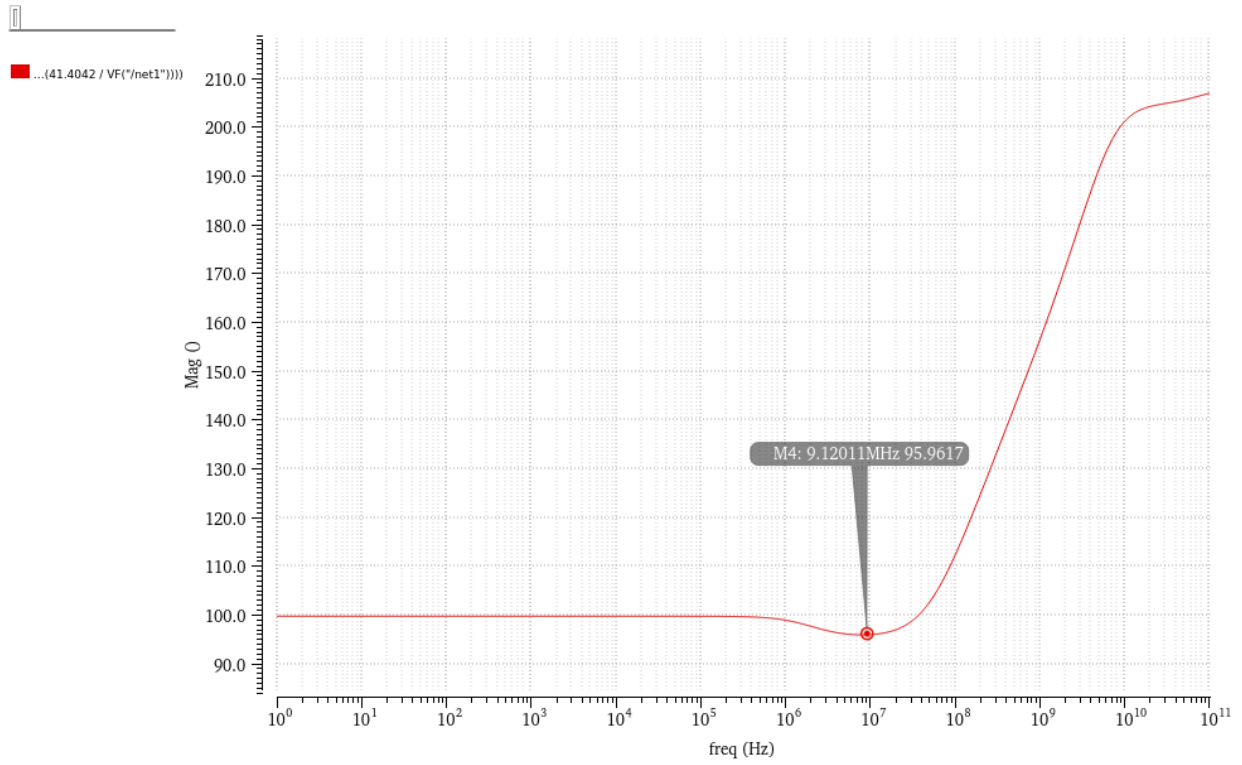

Slew Rate:

Transient Response   Thu Dec 2 16:35:21 2021 1
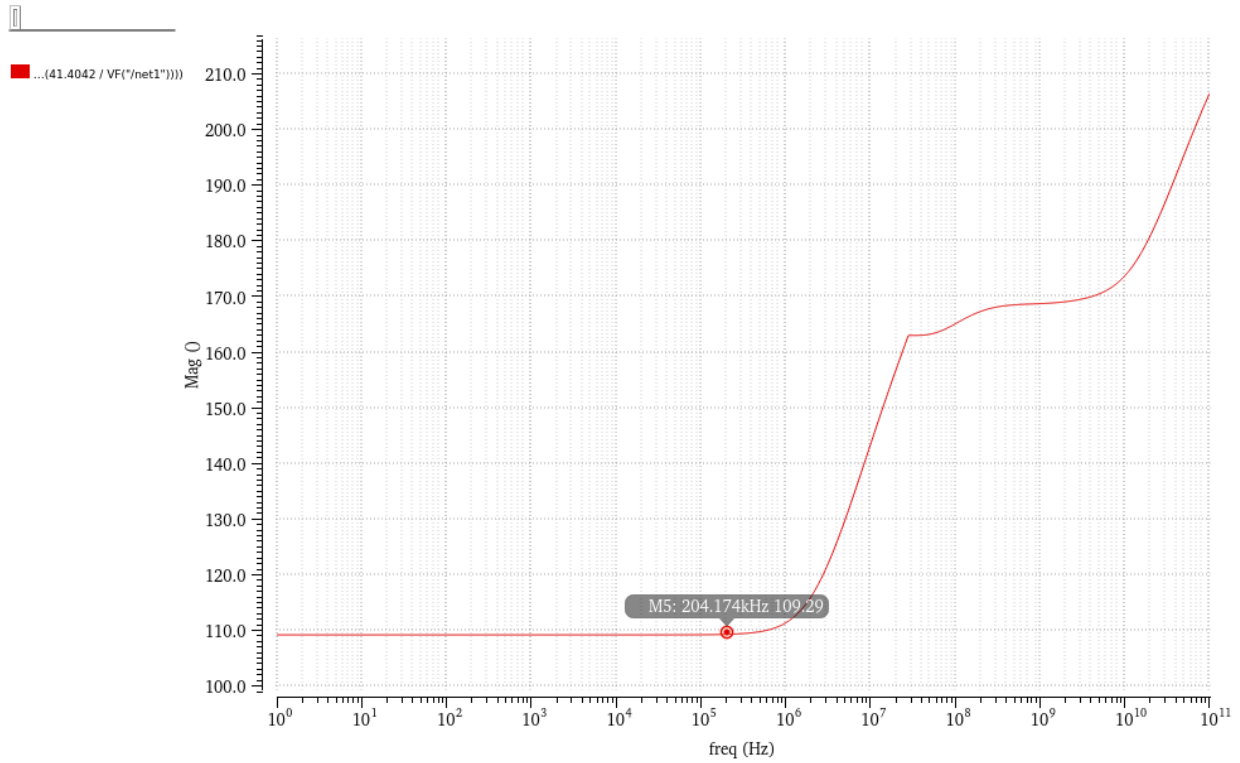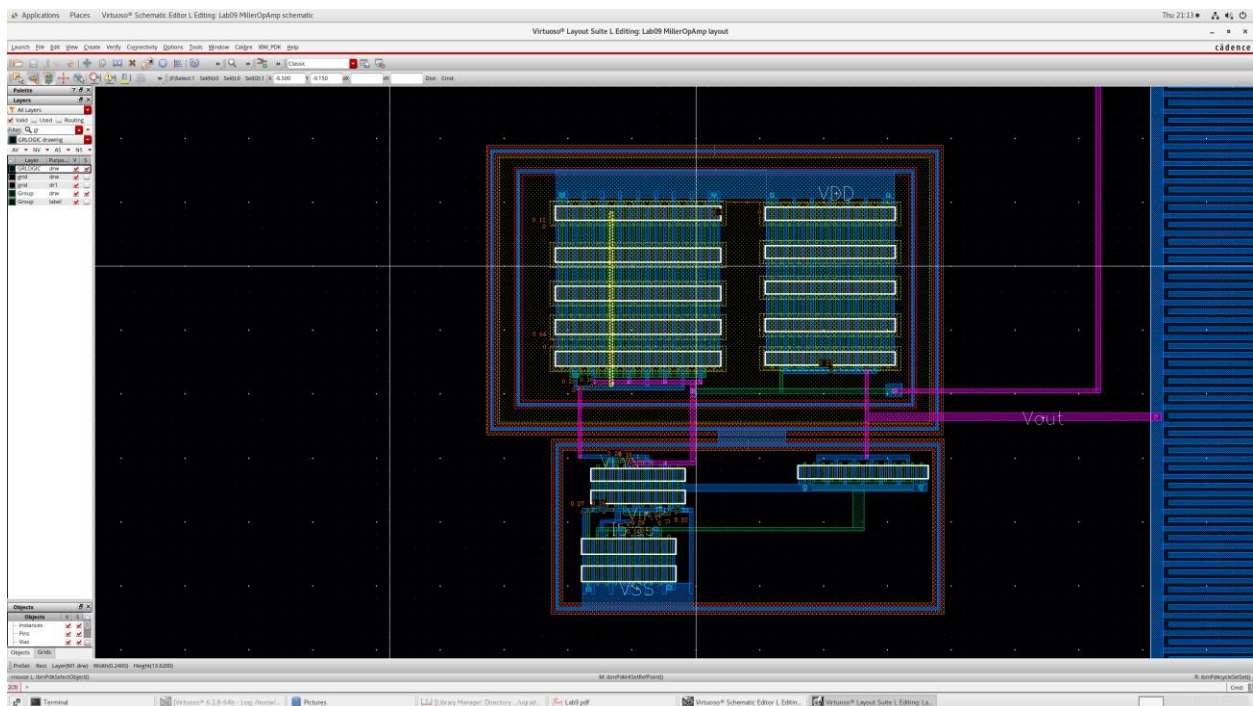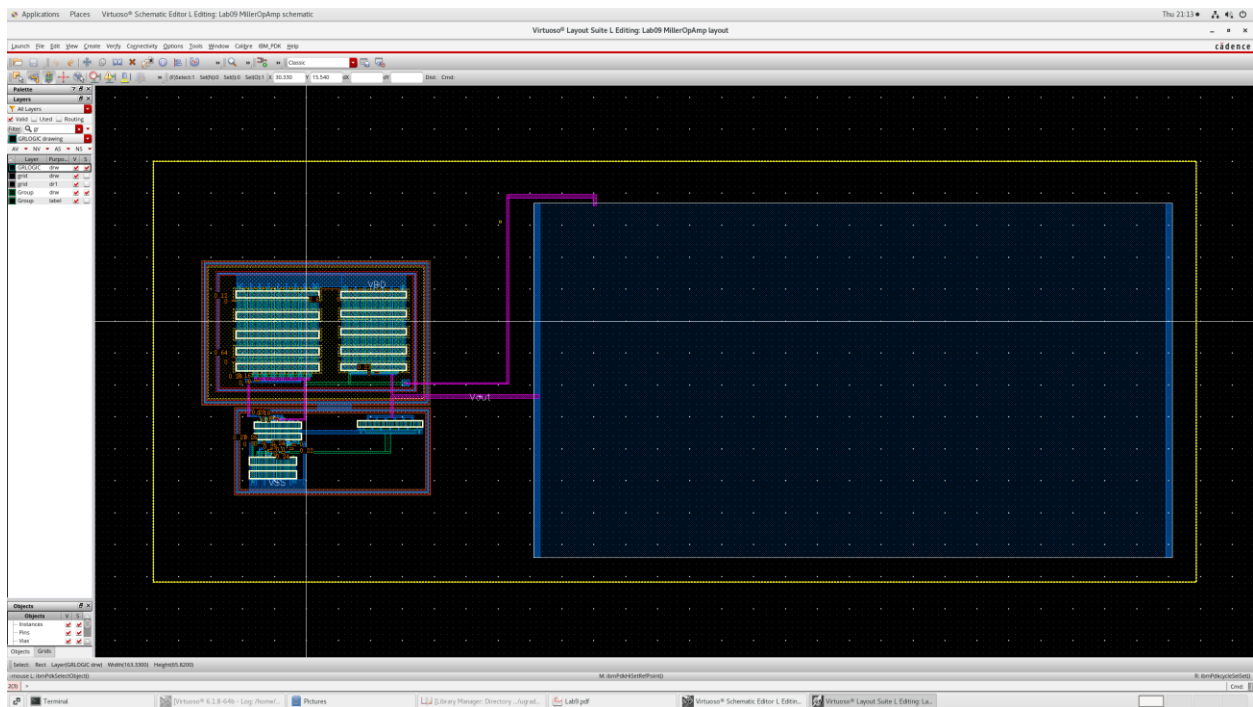

PSRR+:

PSRR-:

(20 * log((41.4042 / VF("/net1"))))

...(41.4042 / VF("/net1"))))

M5: 204.174kHz 109.29

freq (Hz)

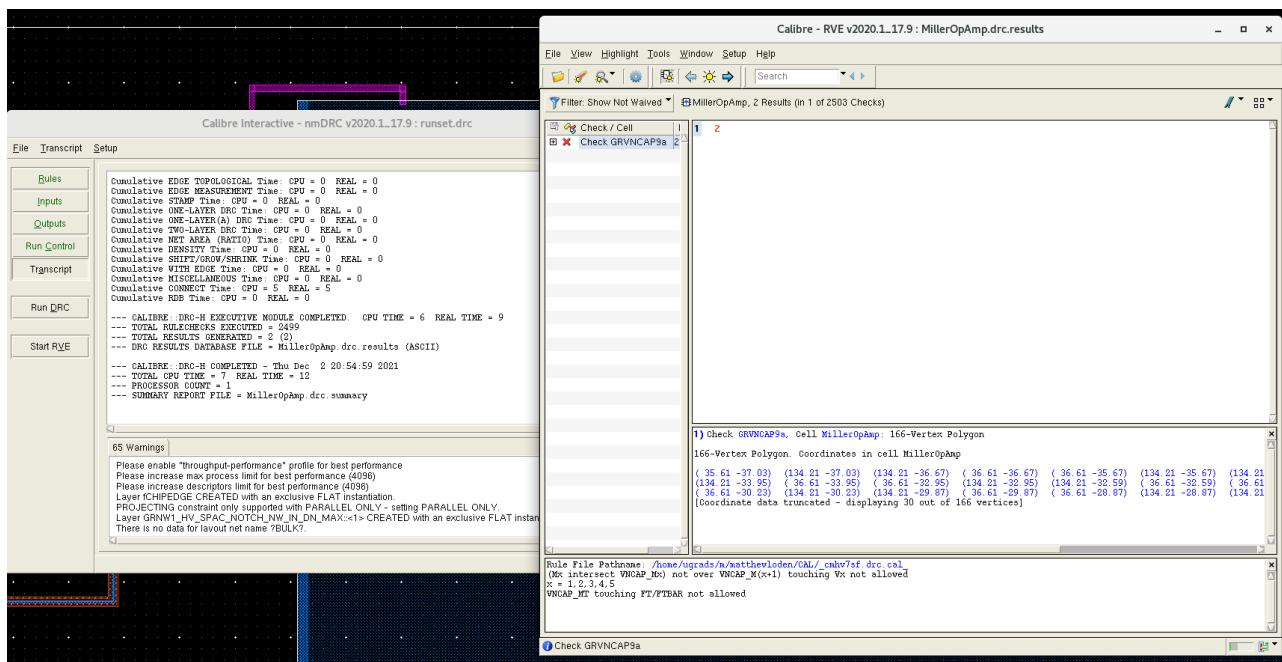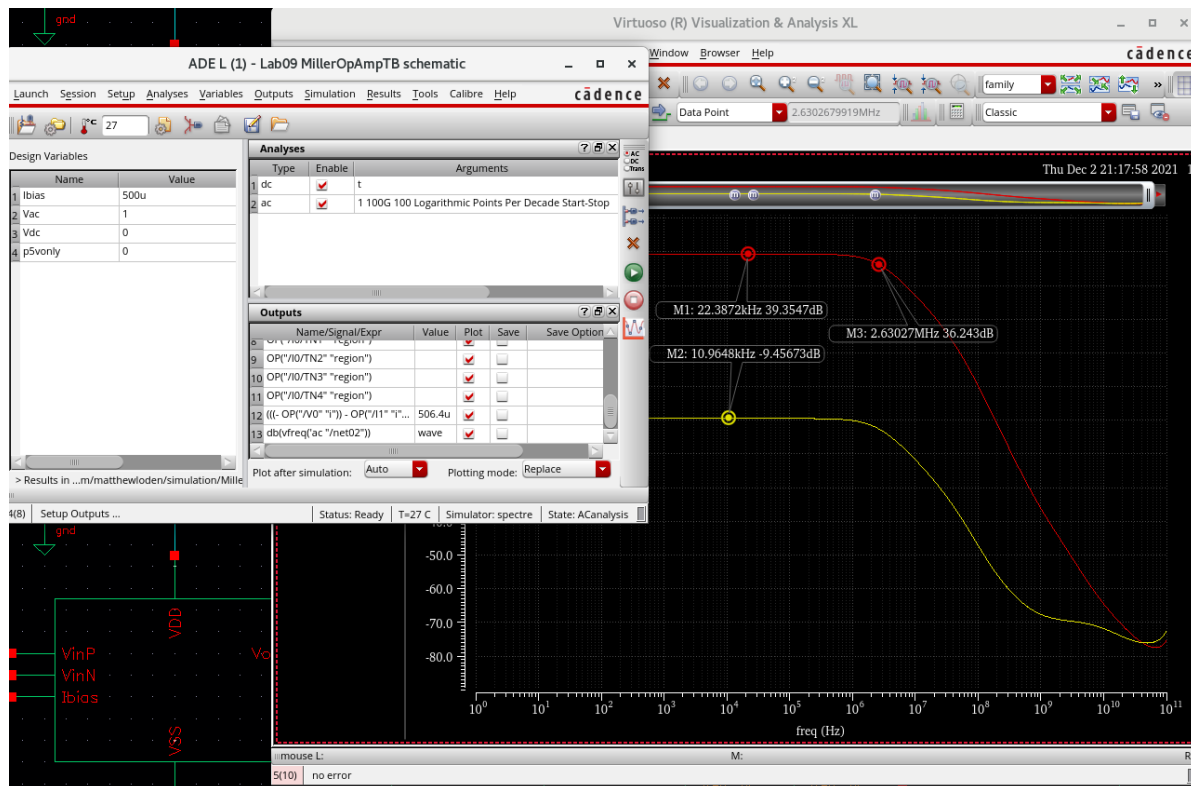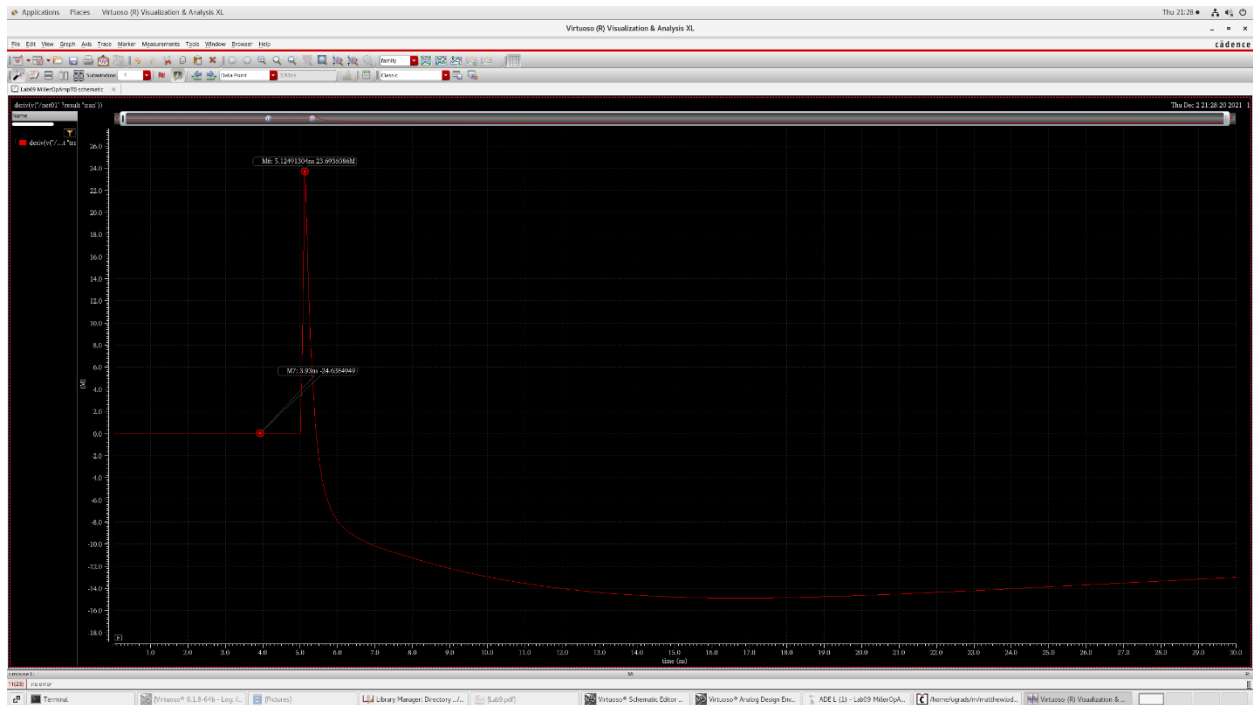Layout:

DRC:

There is a weird error being thrown by the Capacitor and the MT touching FT/FTBAR

LVS:

Calibre - RVE v2020.1_17.9 : svdb MillerOpAmp

File View Highlight Tools Window Setup Help

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  Schematics
Setup
  Options

Comparison Results ×

Layout Cell / Type	Source Cell	Nets
MillerOpAmp	MillerOpAmp	9L, 9S

Cell MillerOpAmp Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```
          #        ###################
         #  #      #                 #
        #    #     #    CORRECT       #
       #      #    #                 #
        #    #     #                 #
         #  #      #                 #
          #        ###################
```

Warning: Unbalanced smashed mosfets were matched.

LAYOUT CELL NAME: MillerOpAmp
SOURCE CELL NAME: MillerOpAmp

INITIAL NUMBERS OF OBJECTS

	Layout	Source		Component Type
Ports:	6	6		
Nets:	9	9		
Instances:	54	8	*	MN (4 pins)
	160	5	*	MP (4 pins)
	1	1		C (3 pins)
Total Inst:	215	14		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

LVS Report File - MillerOpAmp.lvs.report

File Edit Options Windows

```
  ####################################################
  ##                                                ##
  ##        C A L I B R E   S Y S T E M             ##
  ##                                                ##
  ##          L V S   R E P O R T                   ##
  ##                                                ##
  ####################################################
```

REPORT FILE NAME:	MillerOpAmp.lvs.report
LAYOUT NAME:	/home/ugrads/m/matthewloden/CAL/MillerOpAmp.sp ('MillerOpAmp')
SOURCE NAME:	/home/ugrads/m/matthewloden/LVS/MillerOpAmp.netlist.lvs ('MillerOpAmp')
RULE FILE:	/home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:	Thu Dec 2 21:12:52 2021
CURRENT DIRECTORY:	/home/ugrads/m/matthewloden/CAL
USER NAME:	matthewloden
CALIBRE VERSION:	v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020

OVERALL COMPARISON RESULTS

```
          #        ###################
         #  #      #                 #
        #    #     #    CORRECT       #
       #      #    #                 #
        #    #     #                 #
         #  #      #                 #
          #        ###################
```

Warning: Unbalanced smashed mosfets were matched.

****
                                  CELL SUMMARY
****

Result	Layout	Source
-----------	-----------	--------------
CORRECT	MillerOpAmp	MillerOpAmp

****
                                  LVS PARAMETERS
****

o LVS Setup:

LVS COMPONENT TYPE PROPERTY	element
LVS COMPONENT SUBTYPE PROPERTY	model
LVS PIN NAME PROPERTY	phy_pin
LVS POWER NAME	"VDD" "Vdd" "vdd" "VDD:P" "DVDD" "DVDD:P" "VDD!" "?VDD?" "vdd?" "inh_vdd" "Vcc" "vcc" "?VCC?"
LVS GROUND NAME	"VSS" "Vss" "vss" "VSS:G" "DVSS" "DVSS:P" "?VSS?" "vss?" "GND" "GND:G" " "sub!" "sub?" "inh_gnd" "INH_GND"
LVS CELL SUPPLY	NO

Edit Row 1 Col 1

Post Layout Simulation Data:

Av0:

Adm: 39.35dB   Acm: -9.456dB   Pole 1: 2.6MHz   Pole 2 ~~ 100MHz

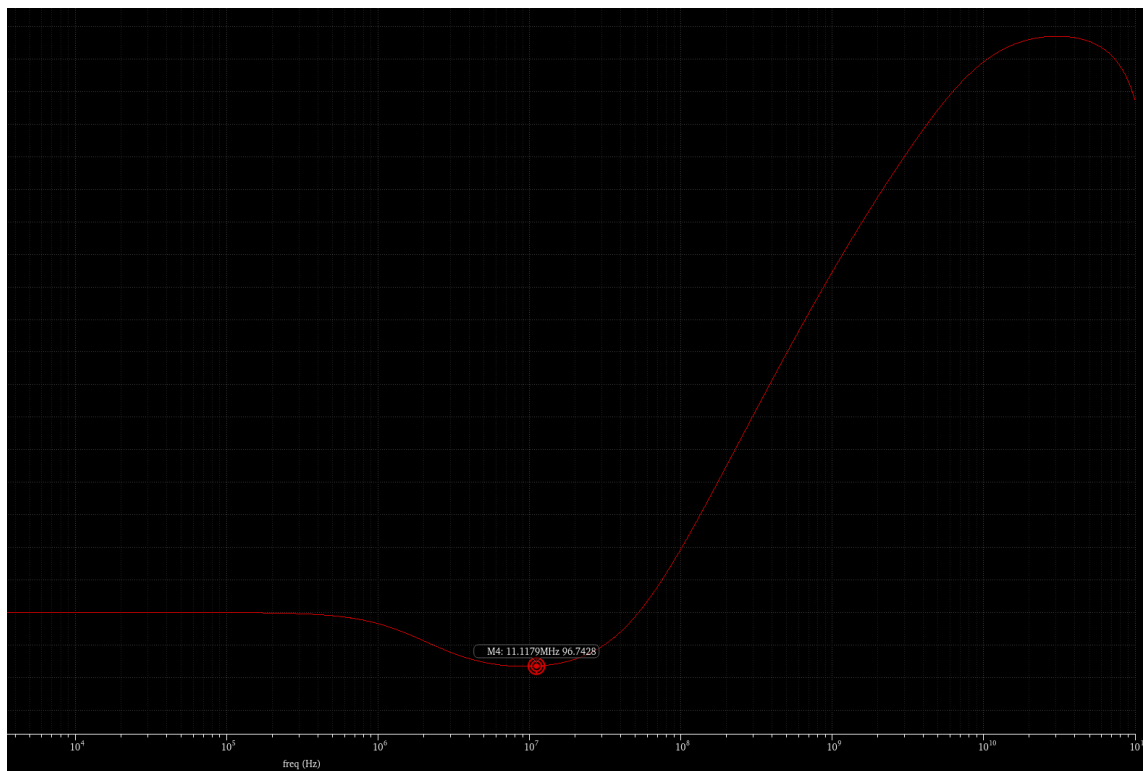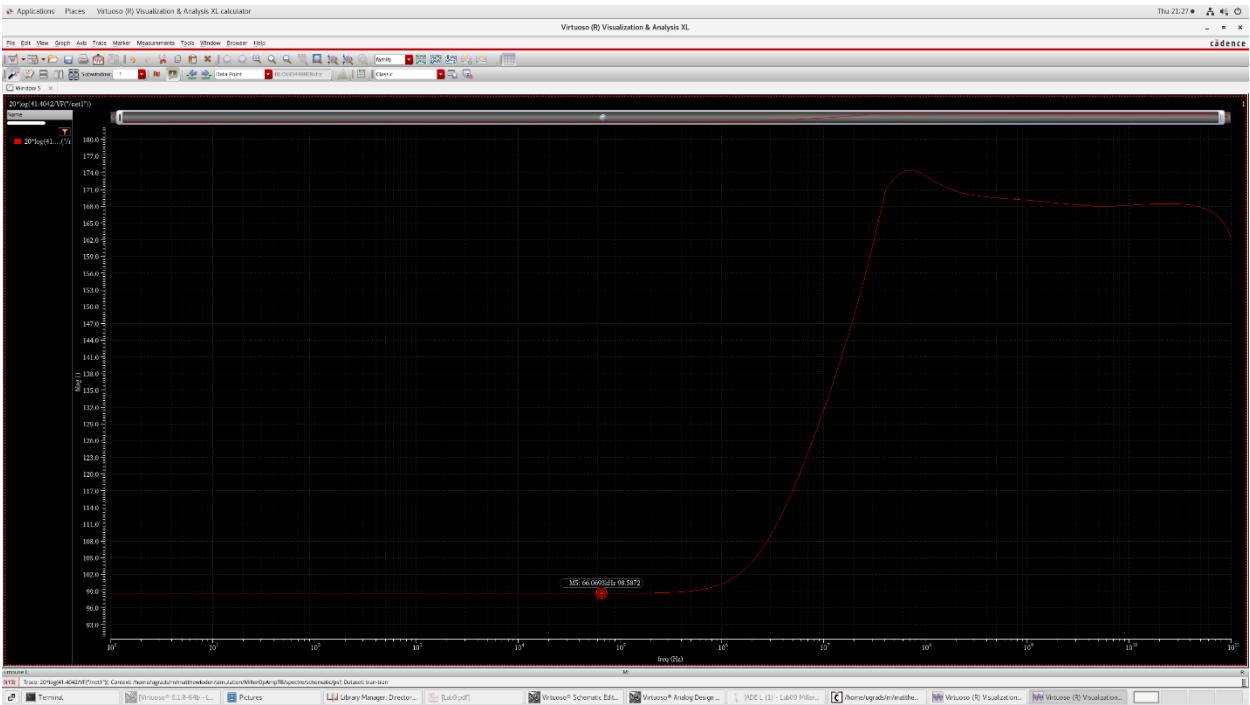CMRR: 48.806dB   GBW: 102.31MHz   Phase Margin ~~ 38.6°

Power Consumed 506.4uW

Slew Rate:

PSRR+:

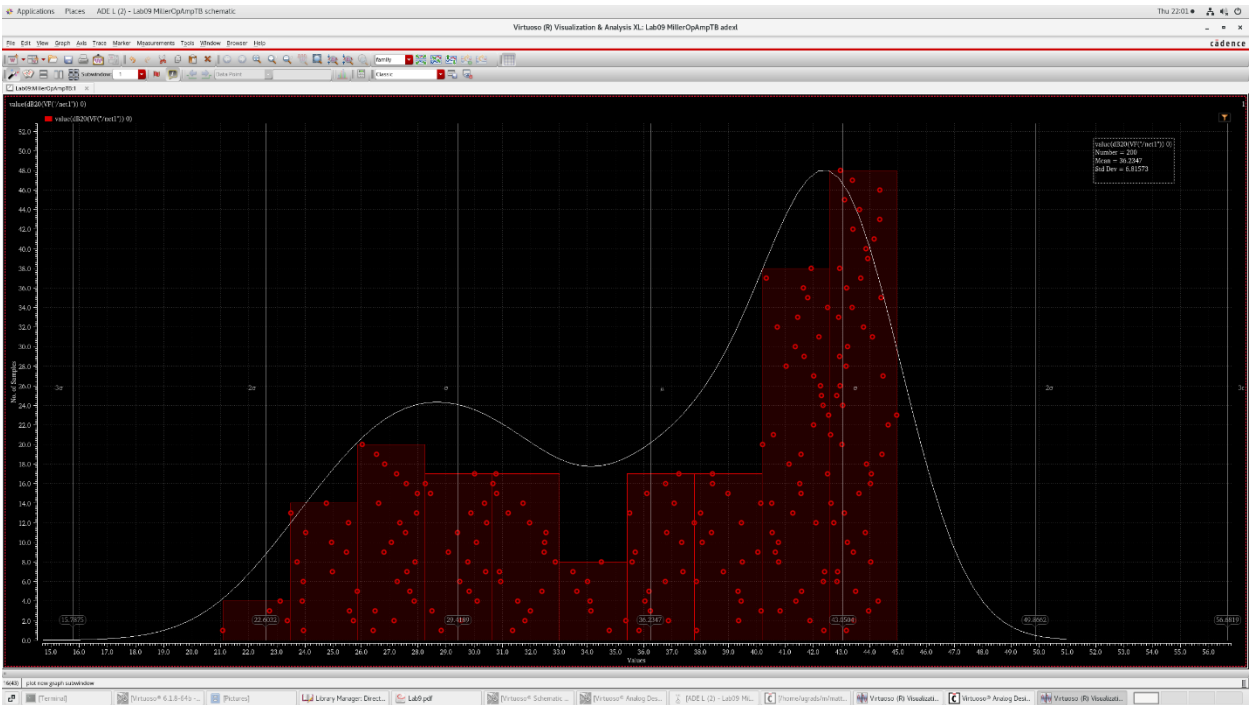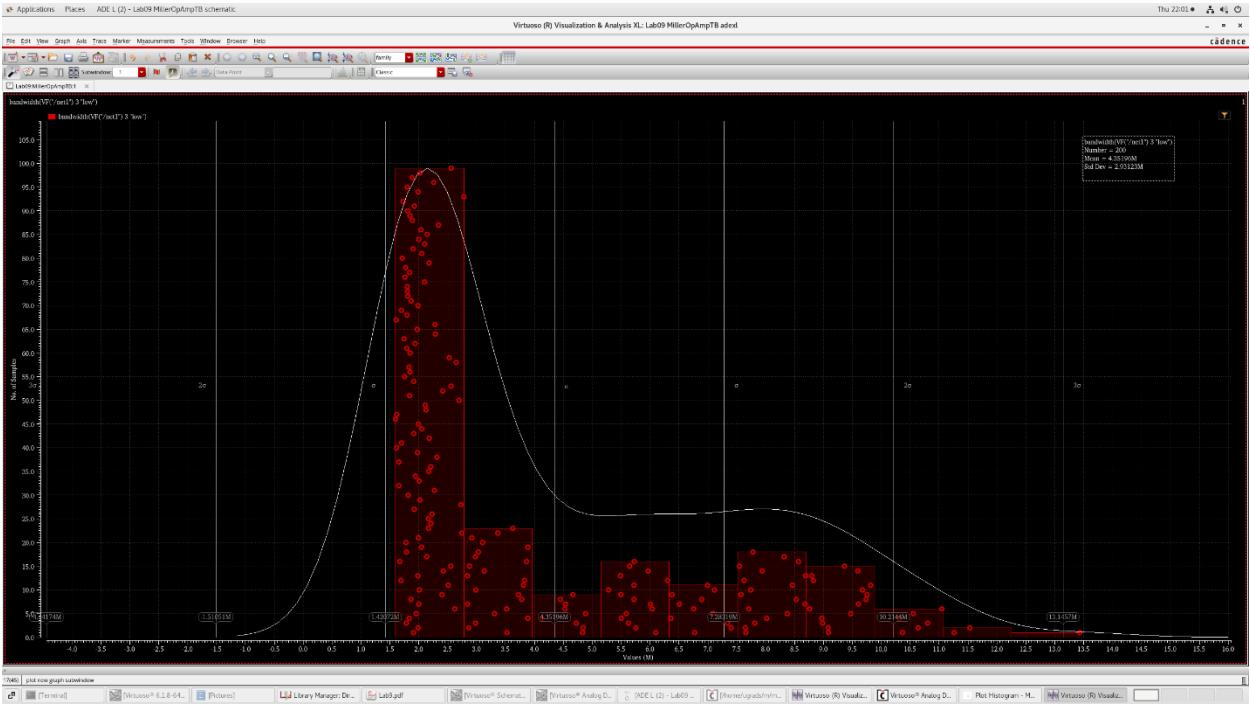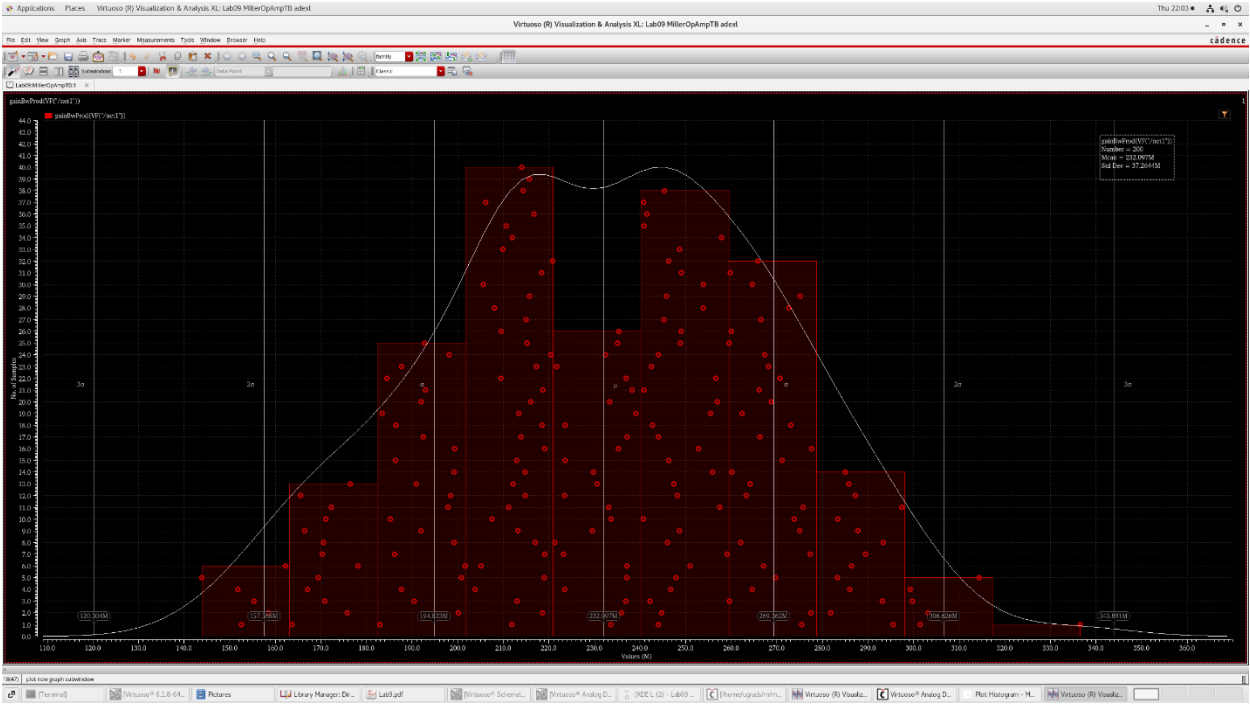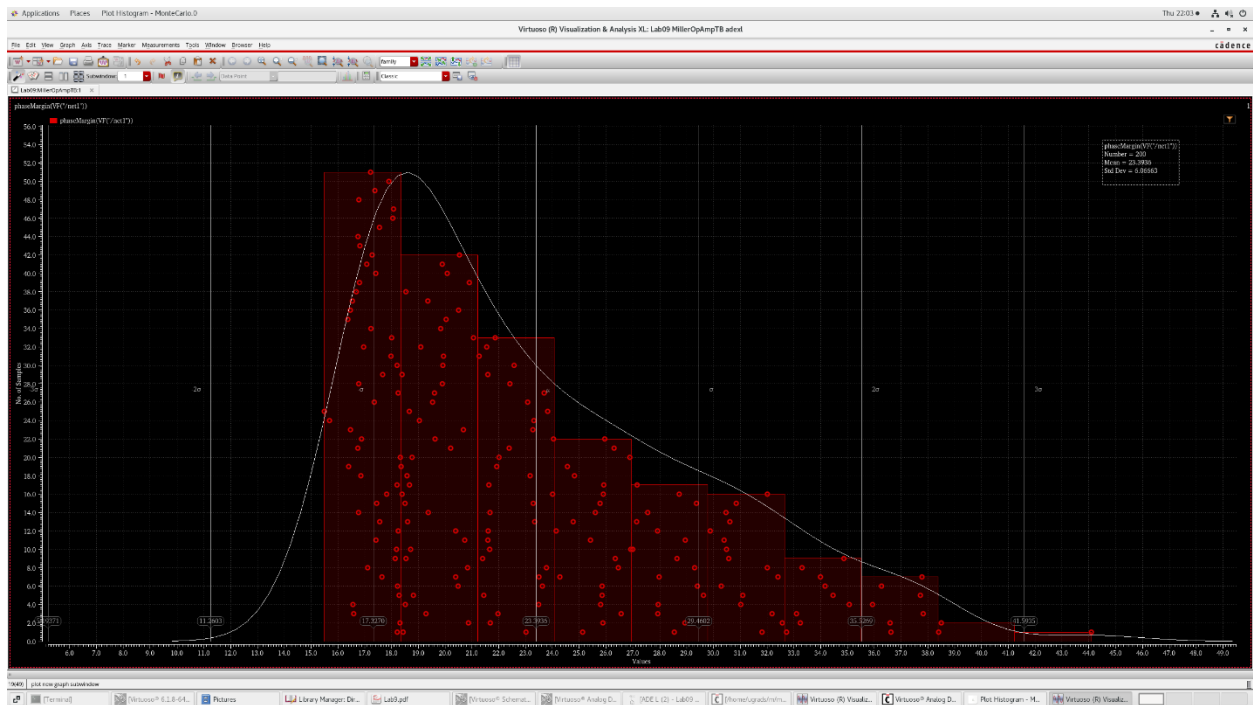PSRR-:

Monte Carlo Analysis:

Av0:

Bandwidth:

Gain Bandwidth:

Phase Margin:

The Values obtained from the Monte Carlo results were somewhat similar to what was estimated in the pre and post layout simulations. The gain and bandwidth values were very similar and were very similar to spec requirements. The main difference came from the phase margin being much lower than spec called for. The phase margin requirement was 45˚ however the simulation data with the math from the lab manual found it to be closer to 40˚. This is in contrast to the value determined by the Monte Carlo analysis which determined the value was much closer to 20˚.