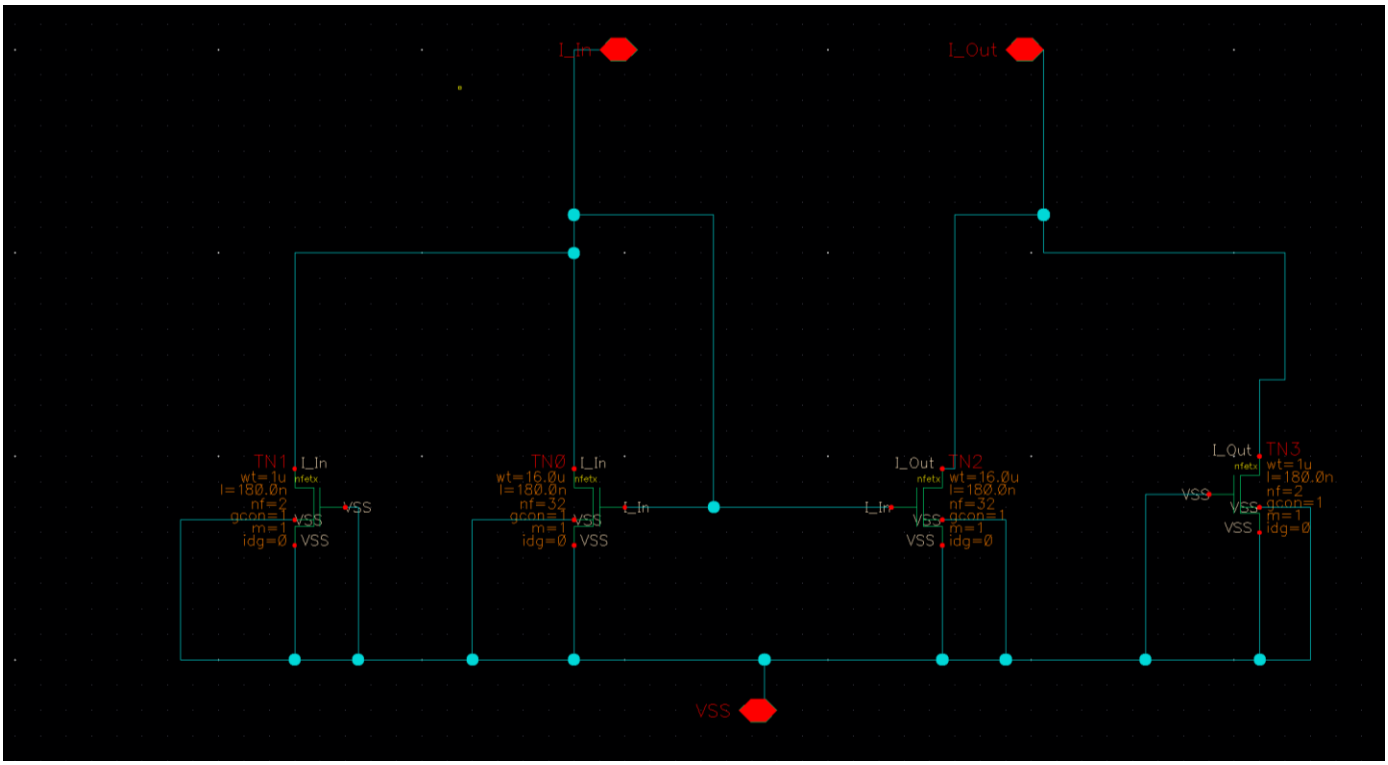
Matthew Loden

ECEN 474 – 502

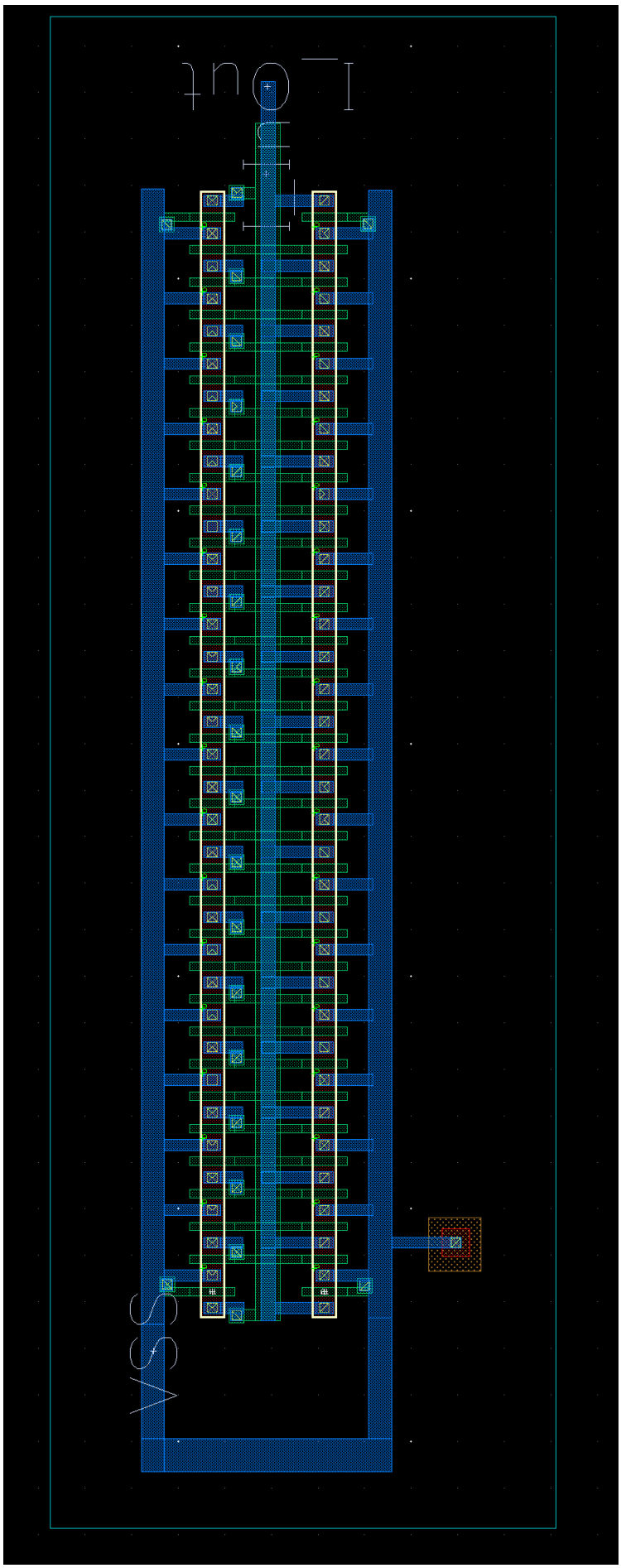
Lab 3: Layout Design Techniques

Current Mirror:

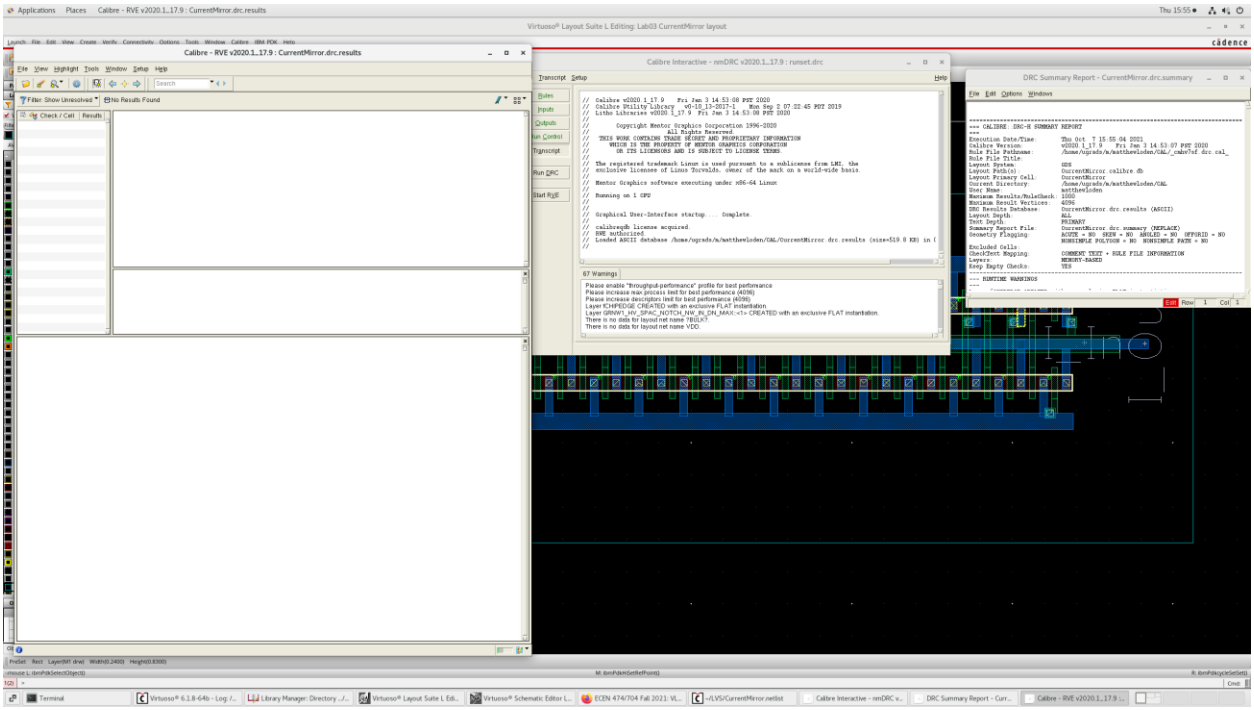
Schematic:



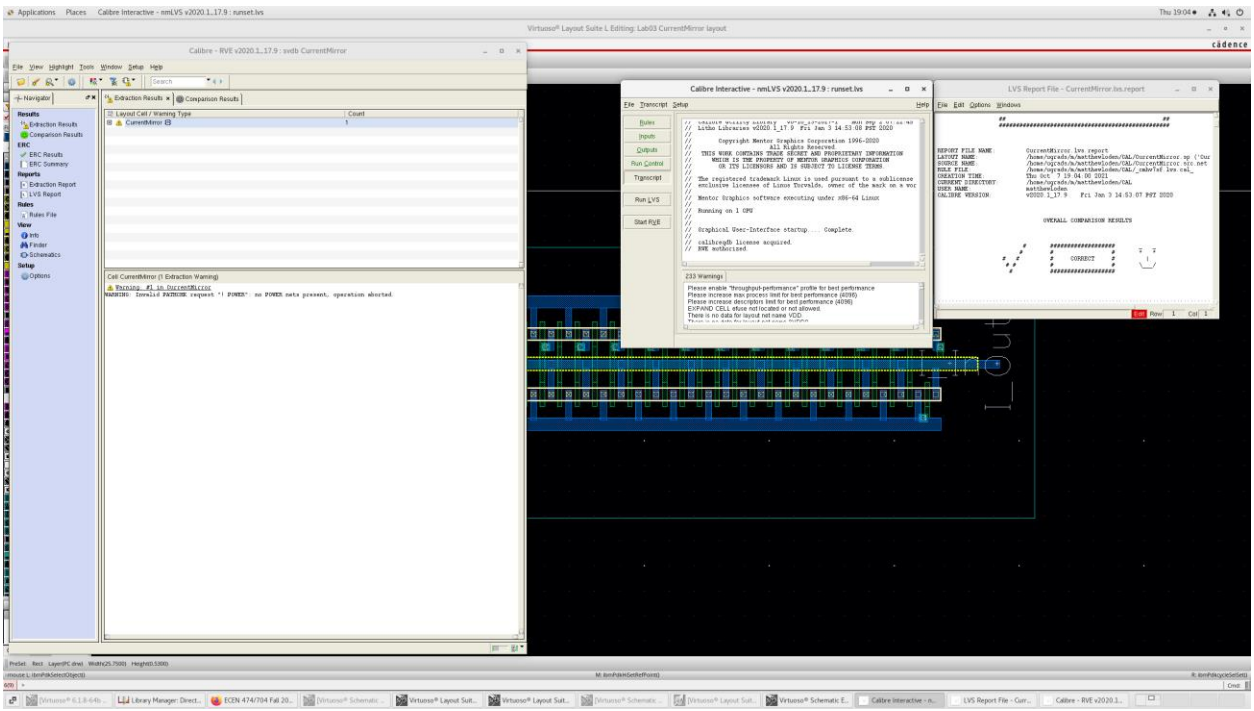
Layout:


I_out
Vss

DRC Check Pass No Errors:



LVS Check Pass:

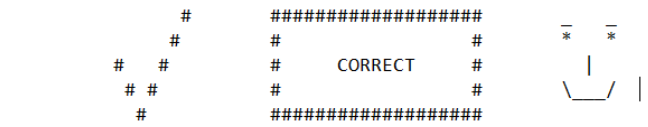


LVS Relevant Text:

```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################
```

REPORT FILE NAME: CurrentMirror.lvs.report
LAYOUT NAME: /home/ugrads/m/matthewloden/CAL/CurrentMirror.sp ('CurrentMirror')
SOURCE NAME: /home/ugrads/m/matthewloden/CAL/CurrentMirror.src.net ('CurrentMirror')
RULE FILE: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME: Thu Oct 7 20:29:23 2021
CURRENT DIRECTORY: /home/ugrads/m/matthewloden/CAL
USER NAME: matthewloden
CALIBRE VERSION: v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020

OVERALL COMPARISON RESULTS



****

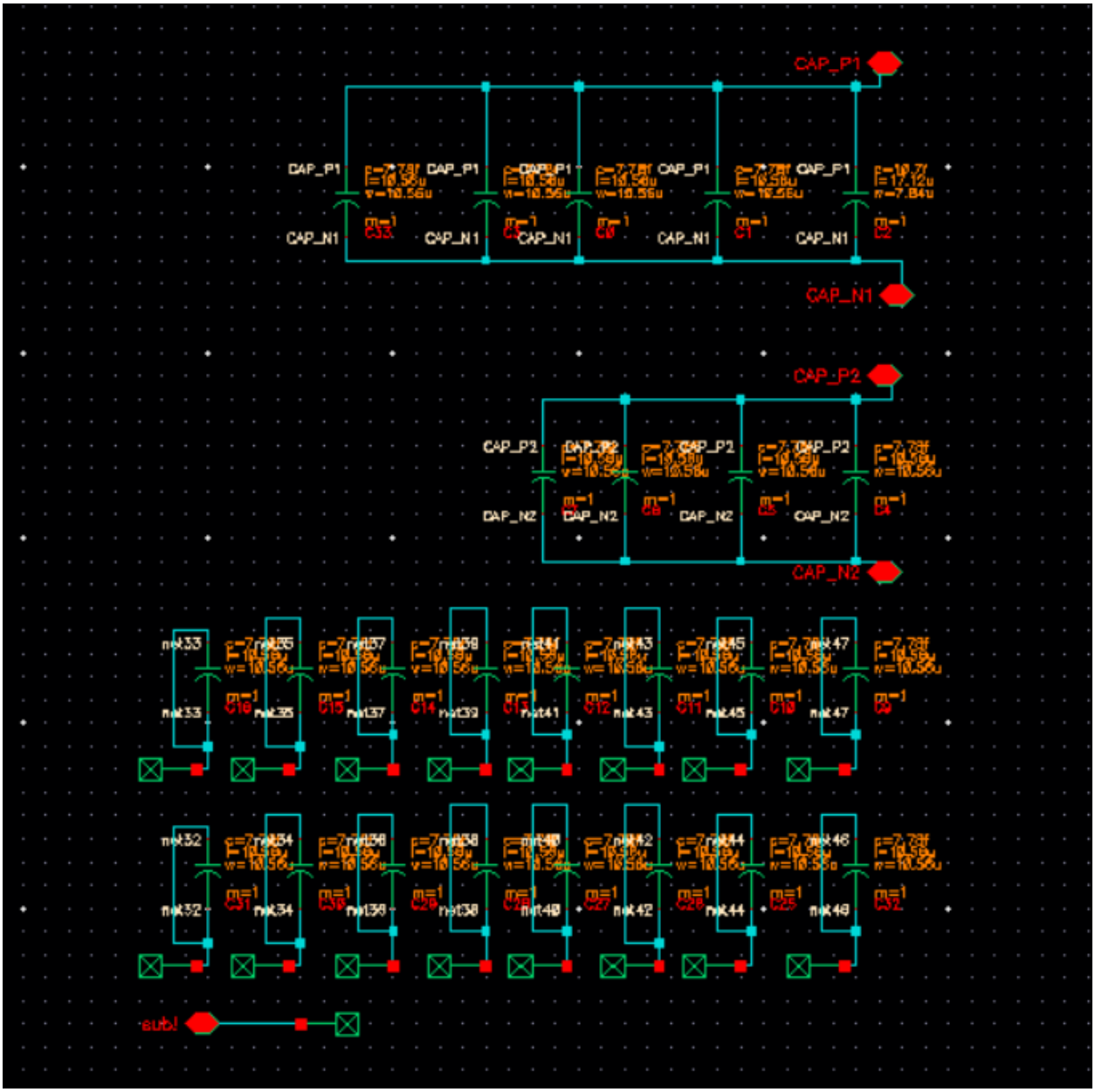
CELL SUMMARY

****

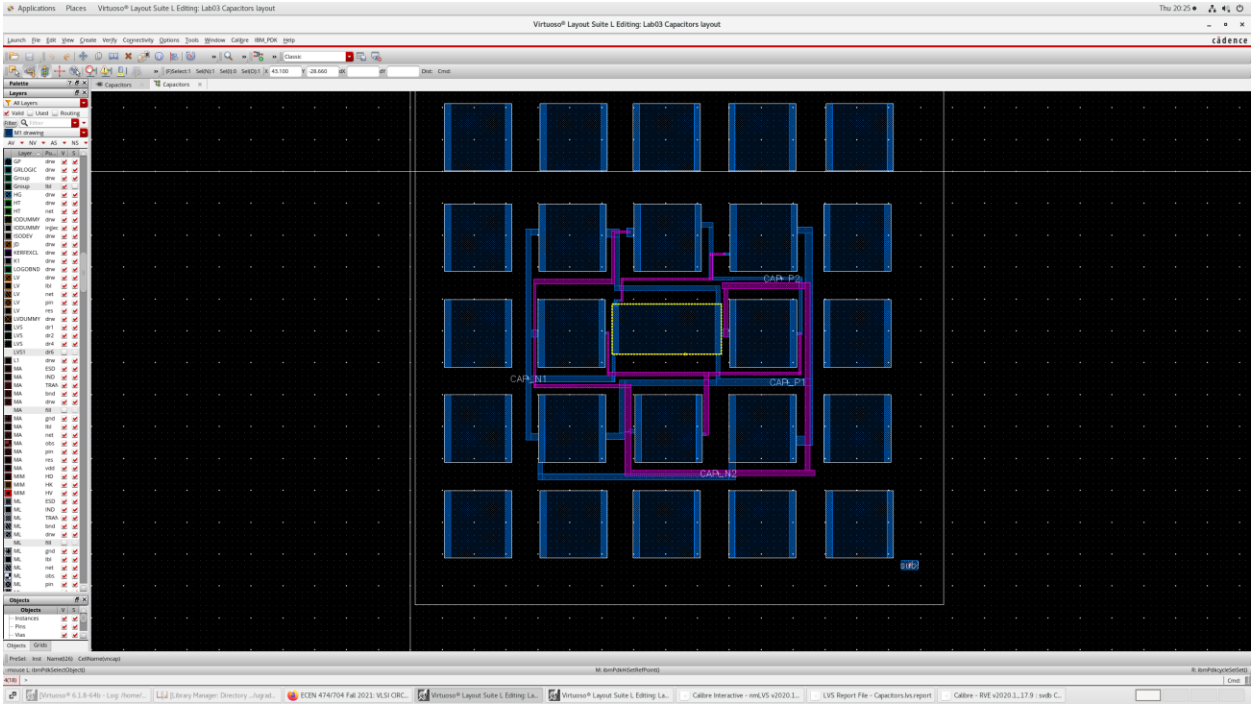
Result	Layout	Source
CORRECT	CurrentMirror	CurrentMirror

Capacitor Work

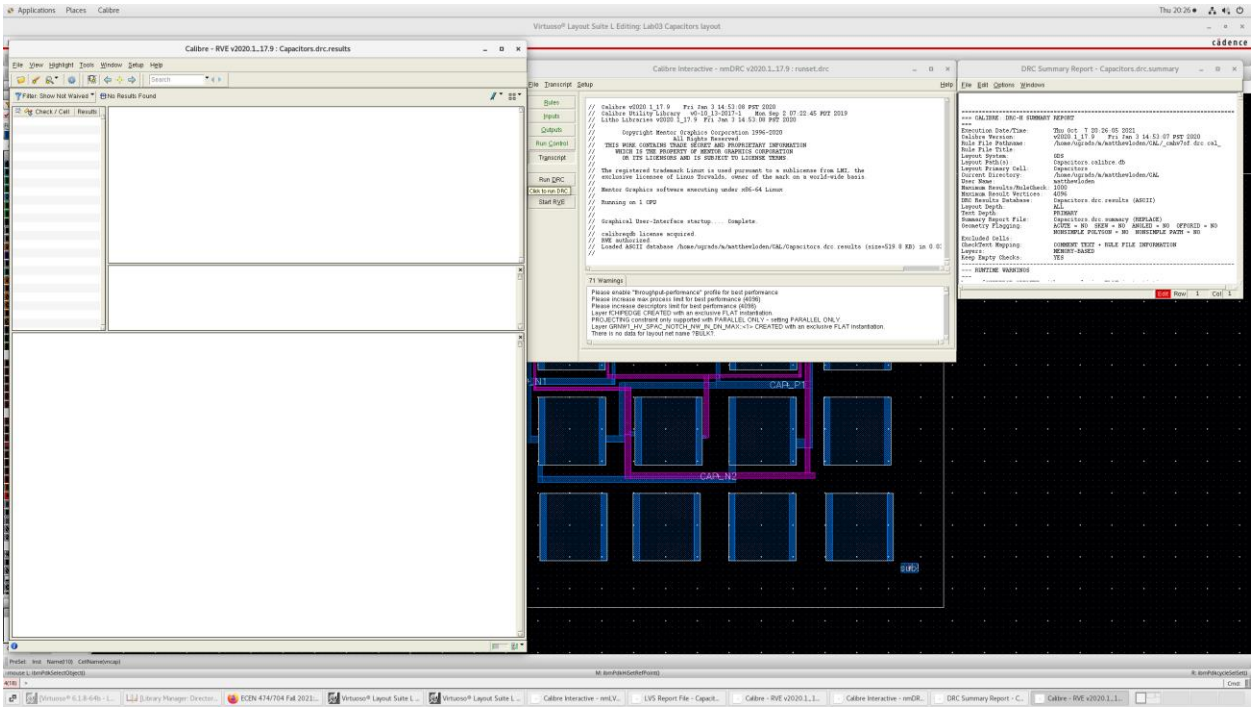
Schematic:



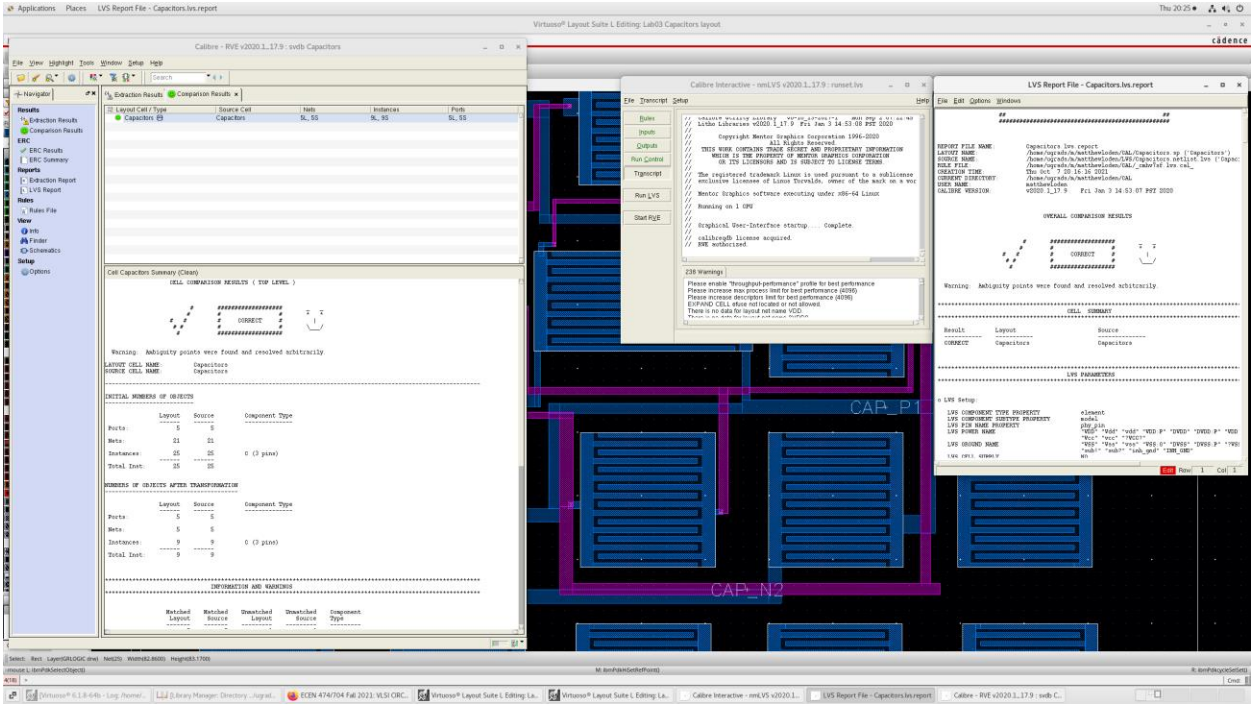
Layout:



DRC Check Pass:



LVS Check Pass:

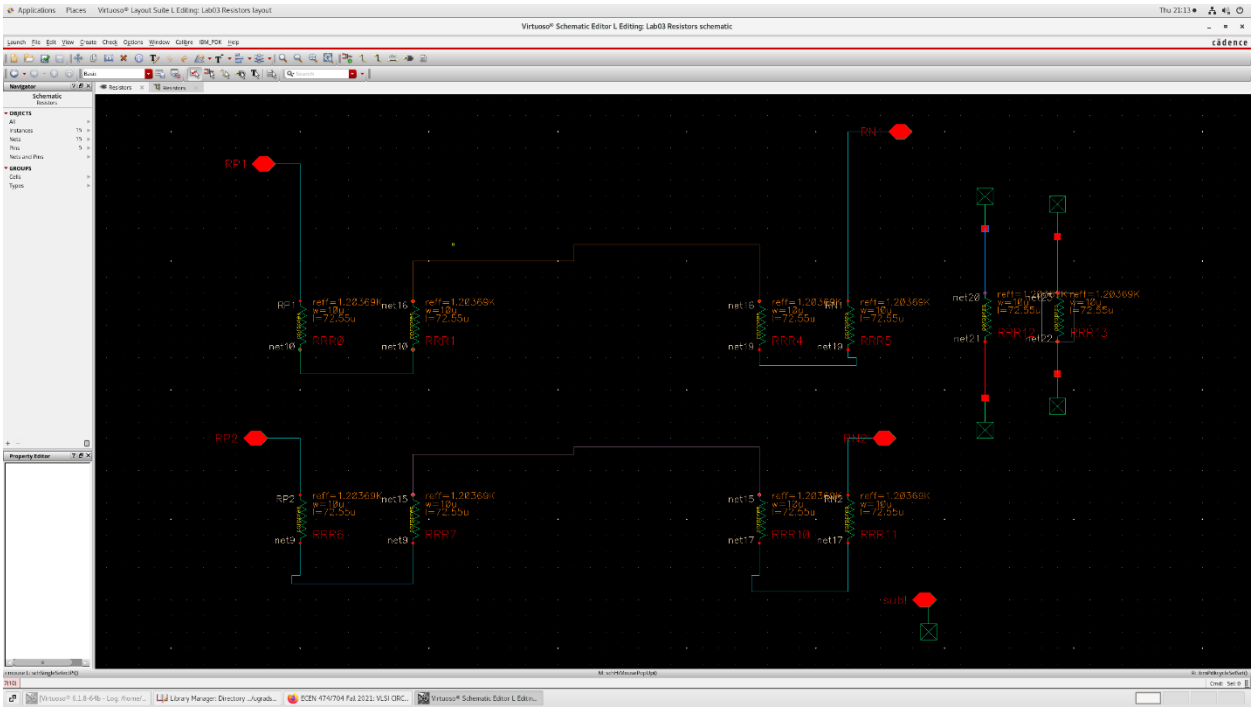


LVS Relevant Text:

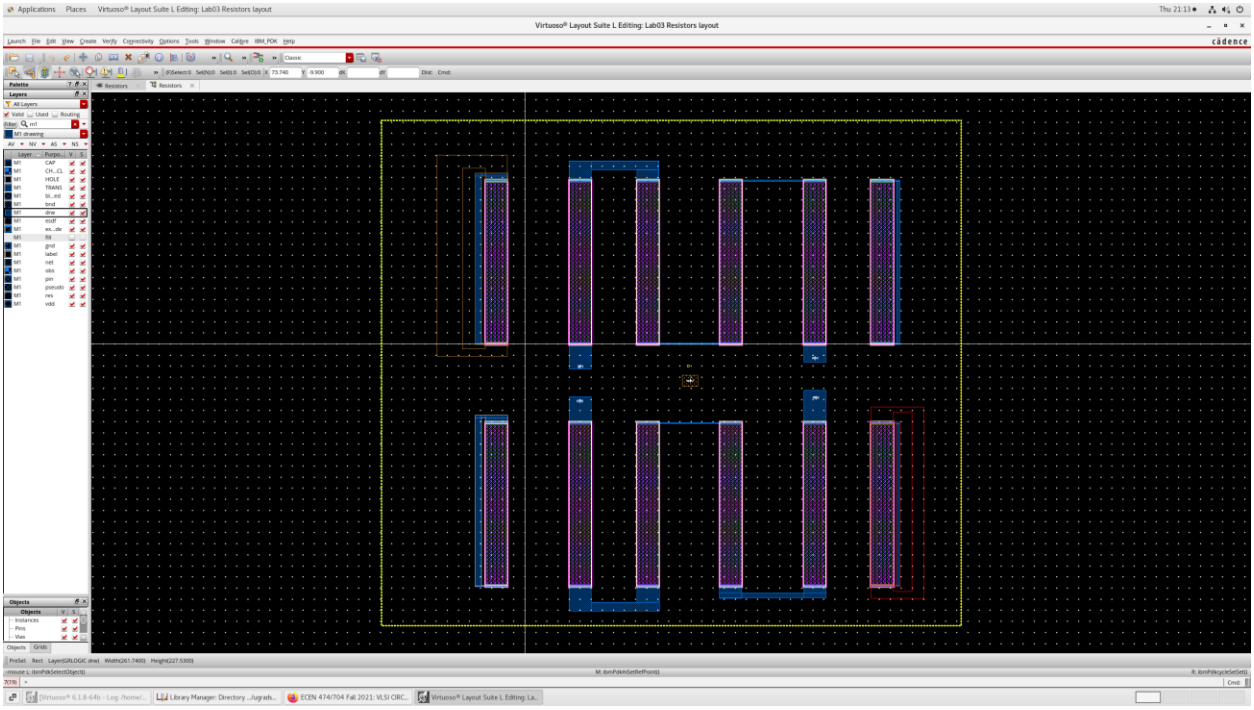
```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################


REPORT FILE NAME:         Capacitors.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/Capacitors.sp ('Capacitors')
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/Capacitors.netlist.lvs ('Capacitors')
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Thu Oct  7 20:16:16 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                     OVERALL COMPARISON RESULTS


                  #       ###################       _   _
                #         #                 #       *   *
              #   #       #     CORRECT     #         |
               # #        #                 #       \___/
                 #        ###################


  Warning:  Ambiguity points were found and resolved arbitrarily.

*****************************************************************************************************
                                  CELL  SUMMARY
*****************************************************************************************************
```

Resistors:

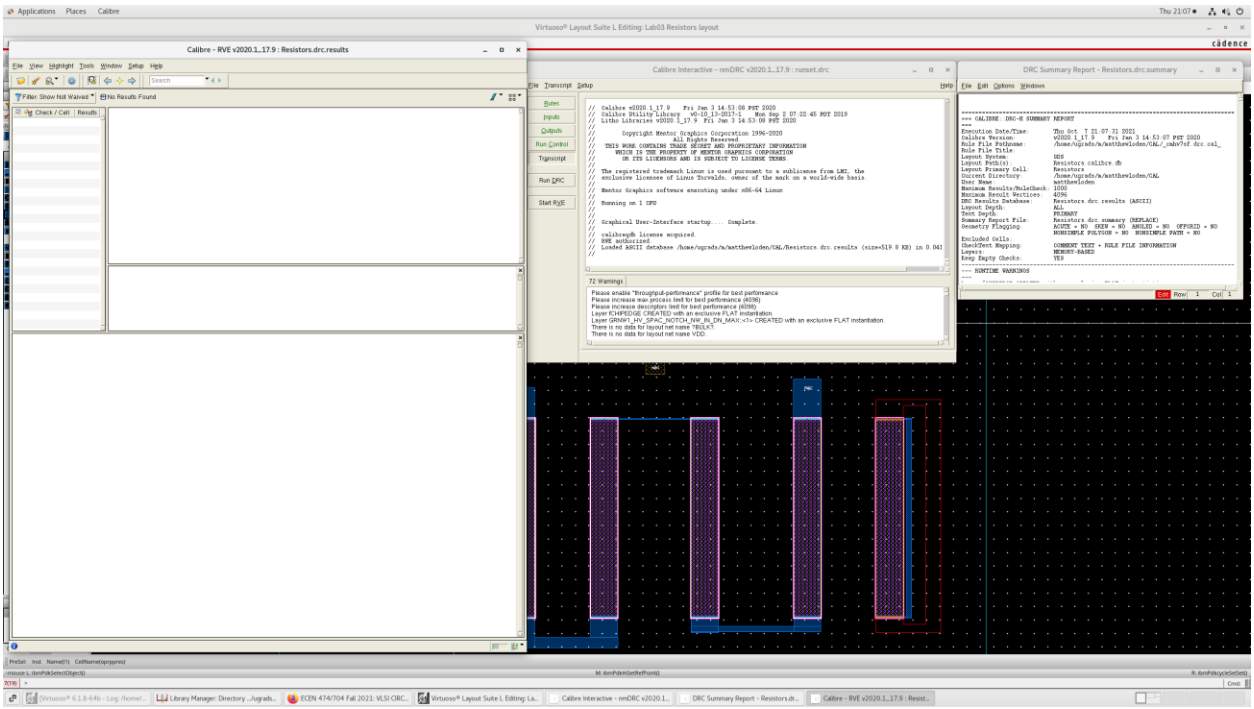
Schematic:



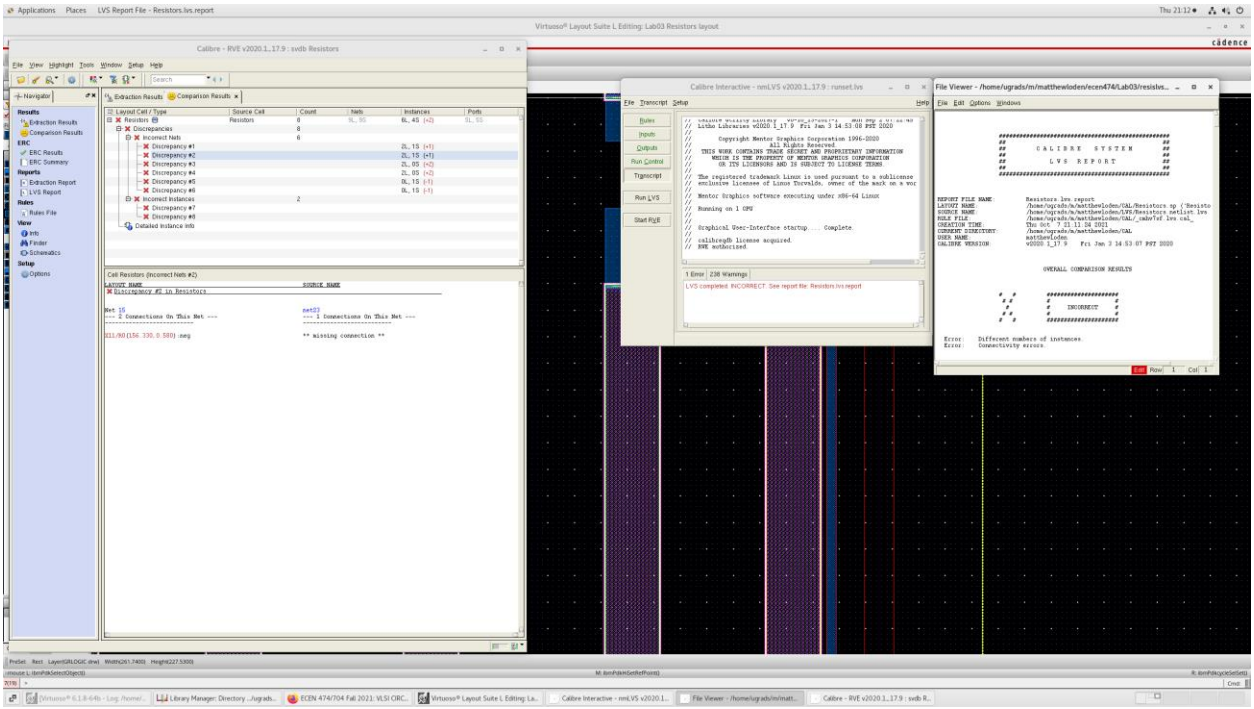
Layout:



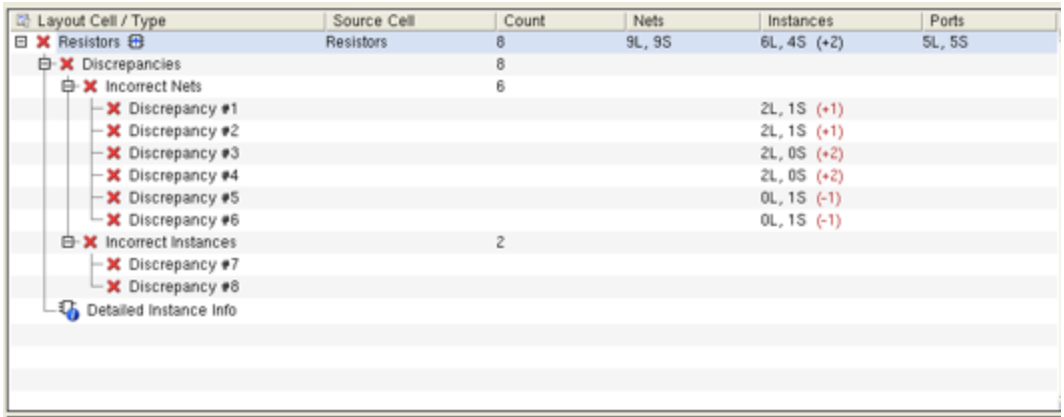
DRC Check Pass:



LVS:



Relevant Error LVS:



Layout Cell / Type	Source Cell	Count	Nets	Instances	Ports
Resistors	Resistors	8	9L, 9S	6L, 4S (+2)	5L, 5S
Discrepancies		8			
Incorrect Nets		6			
Discrepancy #1				2L, 1S (+1)	
Discrepancy #2				2L, 1S (+1)	
Discrepancy #3				2L, 0S (+2)	
Discrepancy #4				2L, 0S (+2)	
Discrepancy #5				0L, 1S (-1)	
Discrepancy #6				0L, 1S (-1)	
Incorrect Instances		2			
Discrepancy #7					
Discrepancy #8					
Detailed Instance Info					

Cell Resistors Summary (8 Discrepancies, Detailed Instance Information)

```
Nets:              15        15

Instances:         12        10    *    R (3 pins)
                 ------    ------
Total Inst:        12        10


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
Ports:               5         5

Nets:                9         9

Instances:           6         4    *    R (3 pins)
                   ------    ------
Total Inst:          6         4

      * = Number of objects in layout different from number in source.


*****************************************************************************************************************
                                    INFORMATION AND WARNINGS
*****************************************************************************************************************


                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source      Layout       Source     Type
                  -------    -------    ---------    ---------    ---------
   Ports:               5          5            0            0
   Nets:                7          7            2            2
   Instances:           4          4            2            0    R(oprppres)
                  -------    -------    ---------    ---------
   Total Inst:          4          4            2            0


o Statistics:

   8 series layout resistors were reduced to 2.  6 connecting nets were deleted.
   8 series source resistors were reduced to 2.  6 connecting nets were deleted.


o Initial Correspondence Points:

   Ports:        sub! RP2 RP1 RN2 RN1
```

```
################################################
##                                            ##
##        C A L I B R E   S Y S T E M         ##
##                                            ##
##            L V S   R E P O R T             ##
##                                            ##
################################################
```

```
REPORT FILE NAME:         Resistors.lvs.report
LAYOUT NAME:              /home/ugrads/m/matthewloden/CAL/Resistors.sp ('Resistors')
SOURCE NAME:              /home/ugrads/m/matthewloden/LVS/Resistors.netlist.lvs ('Resistors')
RULE FILE:                /home/ugrads/m/matthewloden/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Thu Oct  7 21:11:24 2021
CURRENT DIRECTORY:        /home/ugrads/m/matthewloden/CAL
USER NAME:                matthewloden
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020
```

OVERALL COMPARISON RESULTS

```
#   #         ####################
 # #          #                  #
  #           #     INCORRECT    #
 # #          #                  #
#   #         ####################
```

```
  Error:    Different numbers of instances.
  Error:    Connectivity errors.
```

My resistor layout and resultant LVS check did not complete and correctly identify that they were the same information. The main problem I could determine was that the system did not know what to do with my “dummy” resistors I placed on the sides of my device. It is my opinion that these errors came only from these dummy resistors. I’m not sure what I could have done to change the outcome of this problem.