ECEN 474/704 Lab 8: Operational Transconductance Amplifiers

Introduction

The operational transconductance amplifier (OTA) is a basic building block of electronic systems. The function of a transconductor is to convert an input voltage to an output current. The transconductance amplifier can be configured to amplify or integrate either voltages or currents. The versatility of an OTA allows its use in many electronic systems such as filters, analog to digital converters, and oscillators. An OTA is also used as the core amplifier for an operational amplifier. The OTA is an essential element of many analog systems.

The symbol for a single-ended OTA is shown in Figure 8-1. The amplifier has two voltage inputs and a single current output. Fully differential versions have two current outputs, and are commonly used in integrated circuits.

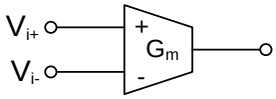

Figure 8-1: The OTA Symbol

The output current of an OTA is proportional to the difference between the input voltages. The relationship between the input voltages and output current is given by:

$$I_o = G_m(V_i^+ - V_i^-)$$

Typical input-output characteristic for an OTA is shown in Figure 8-2. Notice that this characteristic is similar to the input-output characteristic for the differential amplifier. For a given maximum output current, the width of the OTA's linear region is inversely related to the magnitude of the transconductance. The larger the linear region, the smaller the transconductance and vice versa.

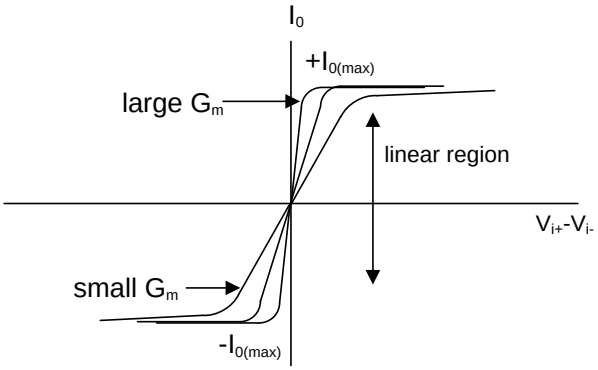

Figure 8-2: Typical Input-Output Characteristics for an OTA

The input and output resistances must be large in an OTA. Infinite input impedance allows maximum transfer of the source voltage to the input of the OTA. Maximum transfer of output current to the load occurs when the output resistance is infinite. Schematic of a basic OTA is shown in Figure 8-3.

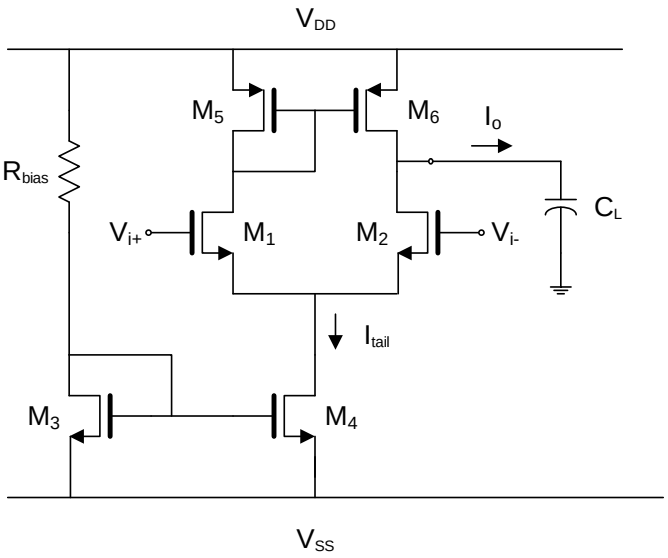

Figure 8-3: Differential Amplifier used as an OTA

A quick analysis of this amplifier shows that the transconductance is given by:

$$G_m = g_{m1,2}$$

The input resistance is large due to the inputs being at the gate terminals of the MOSFET differential pair. Notice that the output resistance is also large.

$$R_{out} = r_{02} || r_{06}$$

The gain-bandwidth product (GBW) is given approximately by:

$$GBW = \frac{g_{m1,2}}{C_L}$$

An improvement of the differential amplifier in Figure 8-3 is to use self-biased loads. The circuit in Figure 8-4 is called a symmetric OTA or the three current-mirror OTA. This circuit is constructed from all the basic elements discussed in the previous labs. The input stage is a differential pair, the sub-circuits composed of $M_{1,3}$ and $M_{2,4}$ are self-biased inverters, and the transistors $M_{3,5}$, $M_{4,6}$, $M_{7,8}$ and $M_{9,10}$ are simple current mirrors.

When designing the symmetrical OTA, transistors M_1=M_2, M_3=M_4, M_5=M_6 and M_7=M_8. This reduces the number of designable parameters to four transistor sizes and the tail current. An analysis of this amplifier shows the transconductance is given by:

$$G_m = K g_{m1,2} \quad , \qquad K = \frac{g_{m5,6}}{g_{m3,4}}$$

The input resistance is large due to the MOSFET input stage. The output resistance is given by:

$$R_{out} = r_{06} || r_{08}$$

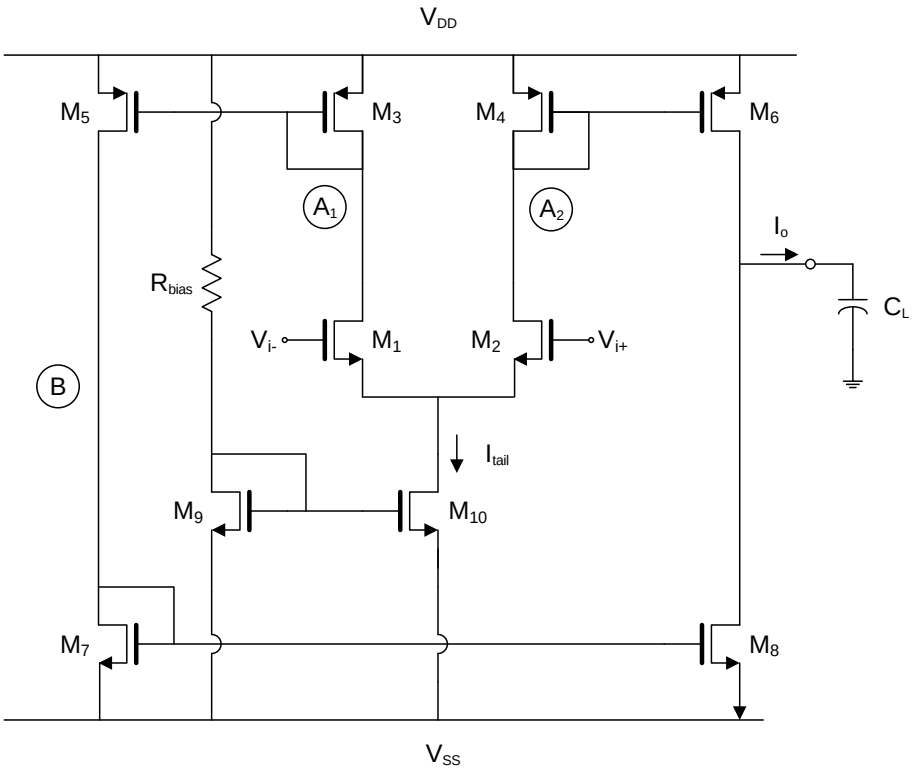

Figure 8-4: The Three Current-Mirror OTA

The gain-bandwidth product is given approximately by:

$$GBW = K\frac{g_{m1,2}}{C_L}$$

Analysis shows that the symmetric OTA has a larger transconductance, slew rate and GBW than the OTA of Figure 8-3. These specifications are made larger by increasing *K*.

Design Description

The design of an OTA begins with a consideration of the design specifications. The typical design specifications for an OTA include transconductance, slew rate, output resistance, GBW, noise, phase margin, power dissipation and output loading. The transconductance of the symmetric OTA was listed previously and is repeated here for convenience:

$$G_m = Kg_{m1,2} = K\sqrt{2KP_N\left(\frac{W}{L}\right)_{1,2} I_{tail}} \quad , \qquad K = \frac{g_{m5,6}}{g_{m3,4}}$$

In the above equation, notice that the DC current in transistors $M_{5,6}$ is *K* times larger than the currents in transistors $M_{3,4}$. The transconductance can be set by the tail current source, current mirror ratio, or size of the input transistors. The transconductance is usually the most important parameter, and it is fortunate that it can be determined by several parameters. Automatic tuning circuits sometimes vary the bias current in order to adjust the transconductance to the desired value.

The slew rate of the OTA is given by:

$$SR = K\frac{I_{tail}}{C_L}$$

Notice the slew rate is larger than the slew rate of the differential amplifier. The increased slew rate comes with the disadvantage of an increase in current which leads to an increase in power consumption. The current drawn from the power supply (not including the bias current source) is given by:

$$I_{DD} = \frac{1}{2}I_{tail} + \frac{1}{2}I_{tail} + \frac{1}{2}KI_{tail} + \frac{1}{2}KI_{tail} = (K+1)I_{tail}$$

The output resistance was provided earlier and is repeated below as:

$$R_{out} = r_{06}||r_{08}$$

The gain-bandwidth product is given by:

$$GBW = A_{v0}p_1 = (G_m R_{out})\left(\frac{1}{R_{out}C_L}\right) = \frac{G_m}{C_L}$$

Another design consideration is noise. The noise performance is improved when the voltage gain of the first stage is large. The voltage gain of the first stage is given by:

$$A_{v1} = \frac{g_{m1,2}}{g_{m3,4}} = \sqrt{\frac{2KP_N\left(\frac{W}{L}\right)_{1,2}\frac{I_{tail}}{2}}{2KP_P\left(\frac{W}{L}\right)_{3,4}\frac{I_{tail}}{2}}} = \sqrt{\frac{KP_N\left(\frac{W}{L}\right)_{1,2}}{KP_P\left(\frac{W}{L}\right)_{1,2}}}$$

The phase margin is a measure of stability for the amplifier. In most cases, the load capacitance is much larger than the capacitance at the other nodes. When this is the case, the OTA has a dominant pole at the output node and two non-dominant poles at the other two nodes. Due to the symmetric behavior at the input stage, the amplifier also has a right half plane zero. For most symmetric OTA designs, the non-dominant poles and zero are much larger than the gain-bandwidth product and degrade the phase margin by less than 10º each. This gives a typical phase margin of greater than 60º. The transfer function of the OTA is given by:

$$H(s) = \frac{\frac{A_{v0}p_1p_2p_3}{z}(s-z)}{(s+p_1)(s+p_2)(s+p_3)}$$

where p_1 is the dominant pole located at the output node:

$$p_1 = \frac{1}{R_{out}C_L}$$

p_2 is the non-dominant pole located at nodes A_1 and A_2:

$$p_2 = \frac{1}{R_A C_A} \approx \frac{g_{m3,4}}{C_A}$$

p_3 is the non-dominant pole located at node B:

$$p_3 = \frac{1}{R_B C_B} \approx \frac{g_{m7}}{C_B}$$

z is the zero due to the pole-zero double formed by the symmetric input stage:

$$z = 2p_2$$

The phase margin is given by:

$$PM = 180° - \tan^{-1}(A_{v0}) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{2p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right)$$

$$PM \approx 90° - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{2p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right)$$

The above design description shows that many performance figures are inversely related. For example, increasing slew rate results in an increase in power dissipation.

Prelab

Design the three current mirror OTA of Figure 8-4 to obtain the following specifications:

G_m	500 µA/V
Slew Rate	> 10 V/µs
Load Capacitance	20 pF
Power	< 1 mW (not including bias current source)
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V

Lab Report

1. Simulate the designs from the prelab, measure (include formulas used) and plot (use markers):

   a) Transconductance versus frequency
   b) Slew rate
   c) Power consumption
   d) Voltage gain versus frequency
   e) Dominant pole frequency
   f) Phase margin
   g) Gain-bandwidth product

   Use any analysis necessary to obtain the most accurate measurements. Include these results in the lab report.

2. Create three cell views for your OTA. The symbol, schematic and layout. Layout your final design and use good layout techniques and include the LVS report (again NetID and time stamp required for credit). Indicate which transistors should be matched in your lab report. Extract the layout and repeat the measurements from part 1. Be sure to include parasitic capacitances in the extraction.