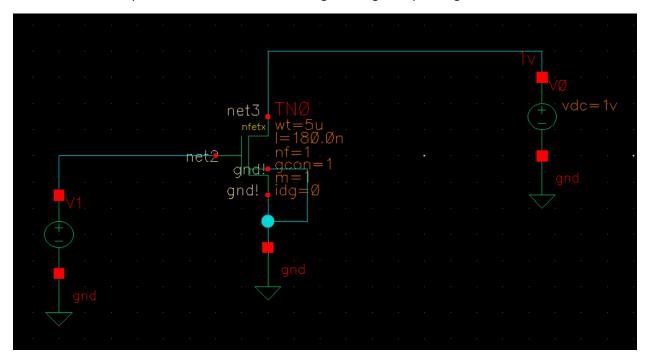
ECEN 474

Lab01

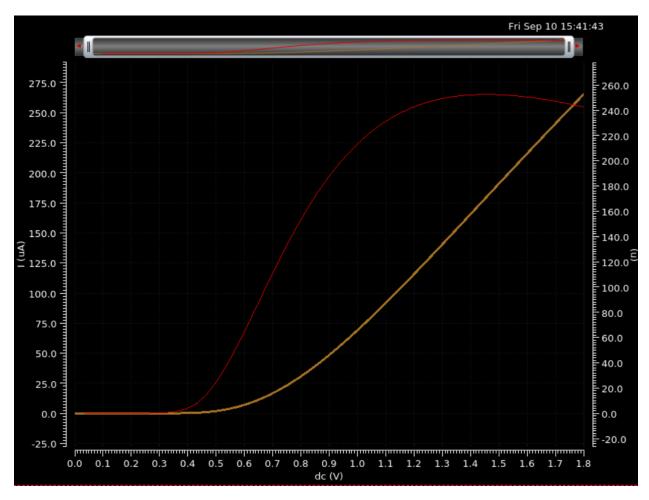
Part 1: NMOS w/ Length = 180 nm

Schematic Used for part 1-3 values of width and length changed depending on a,b,c:

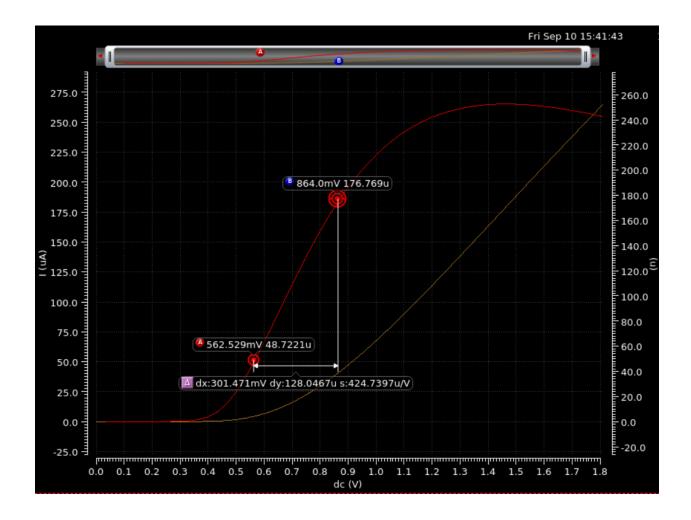


a.)

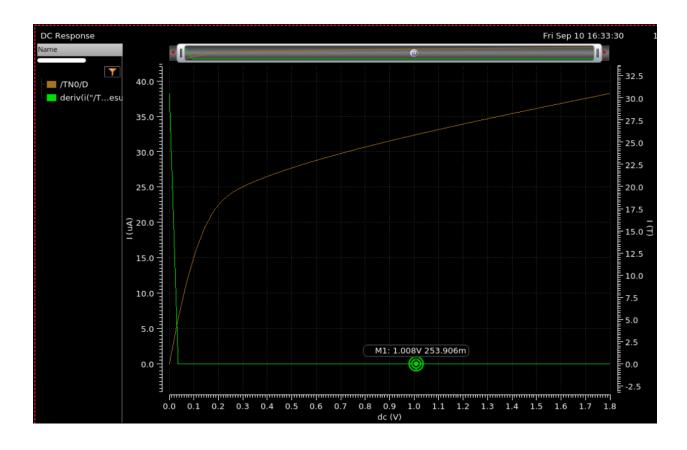
Id plot:



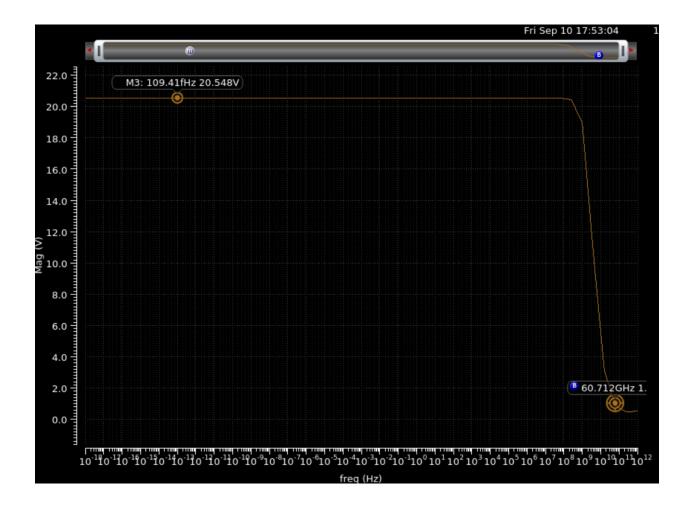
Slope:

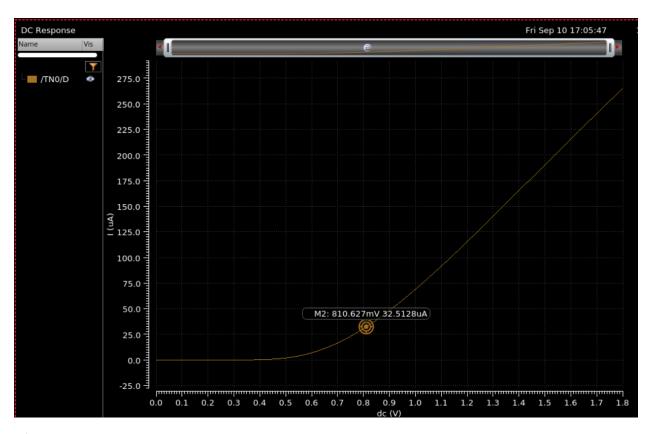


dν



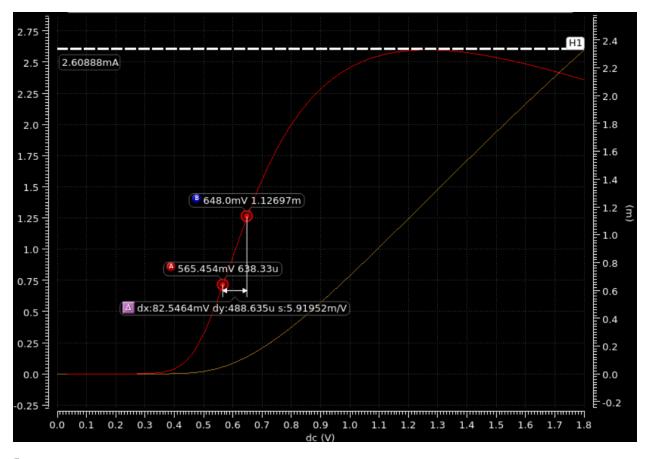
c.)



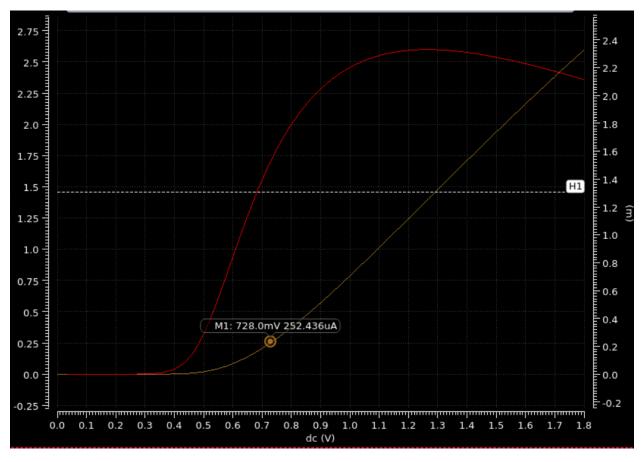


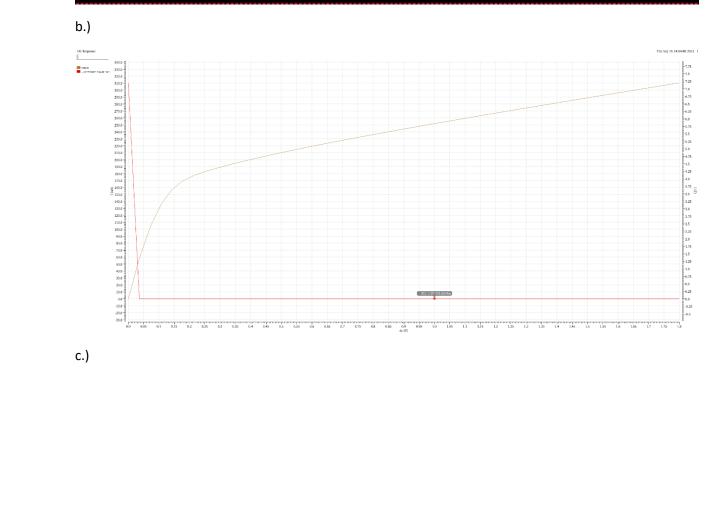
a.)

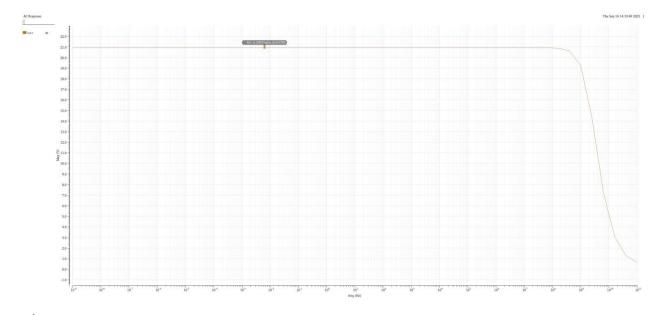
ID Plot

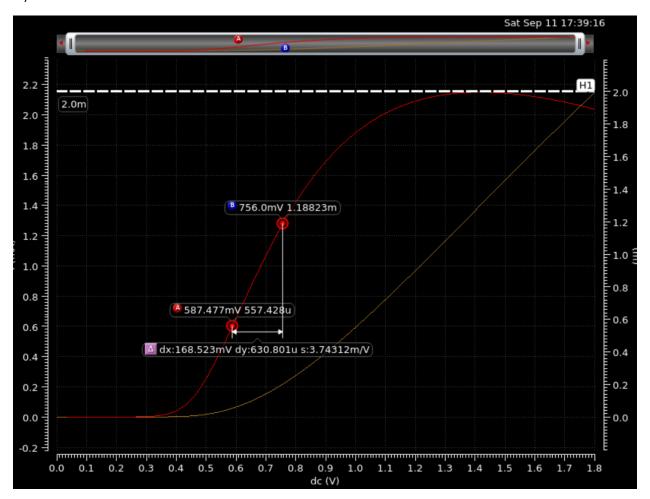


For part c

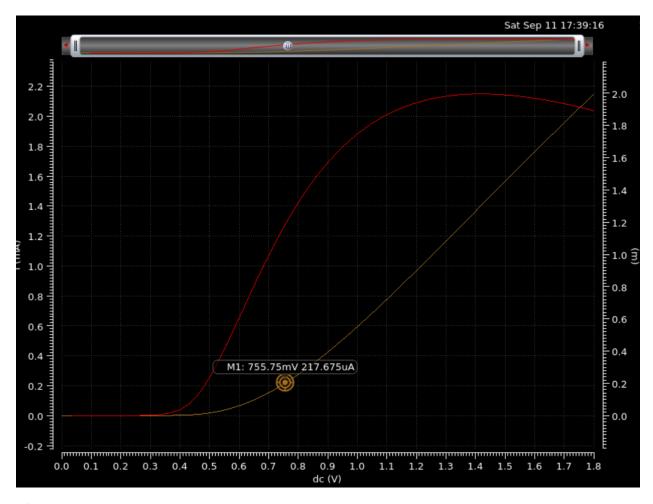


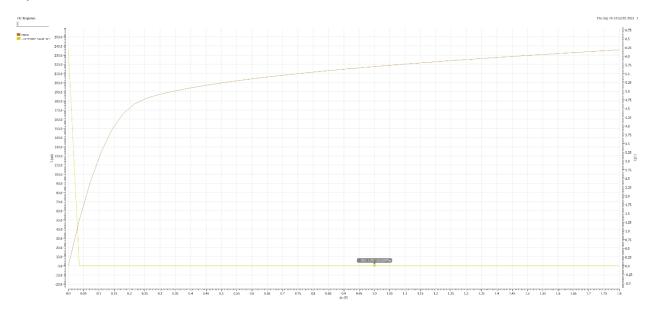




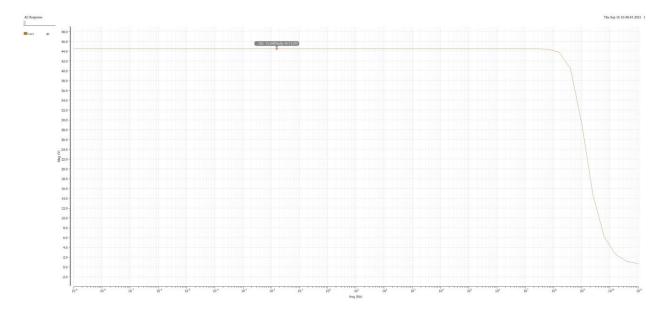


For part c.)





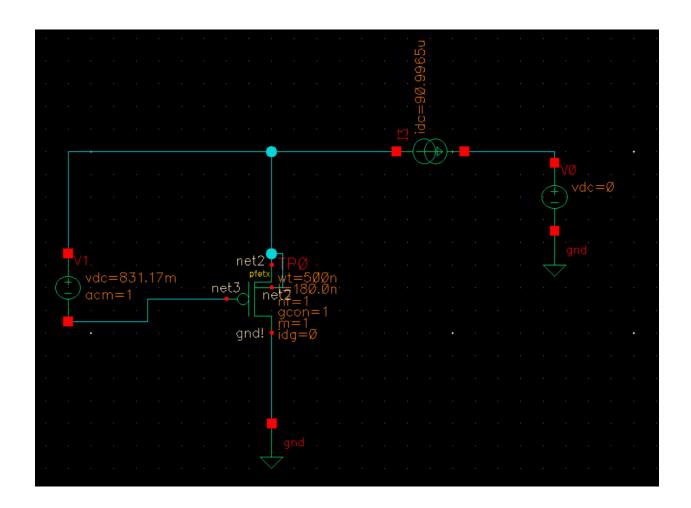
c.)

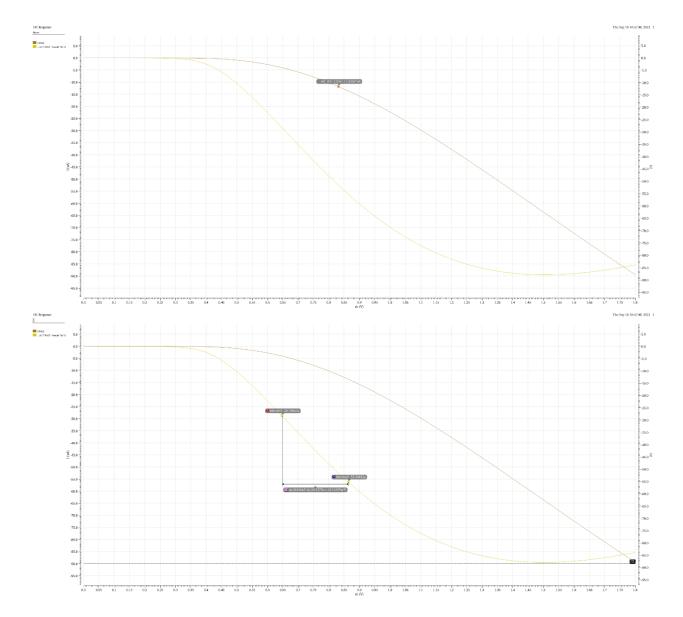


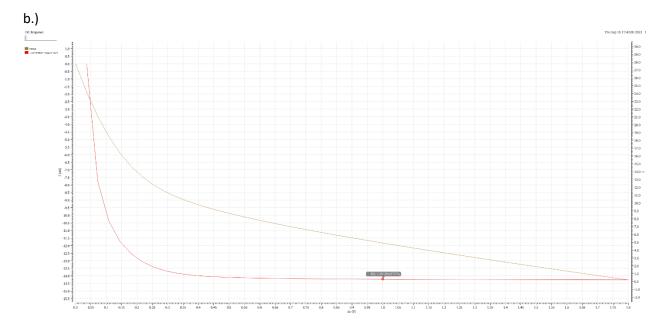
End NMOS transistor section

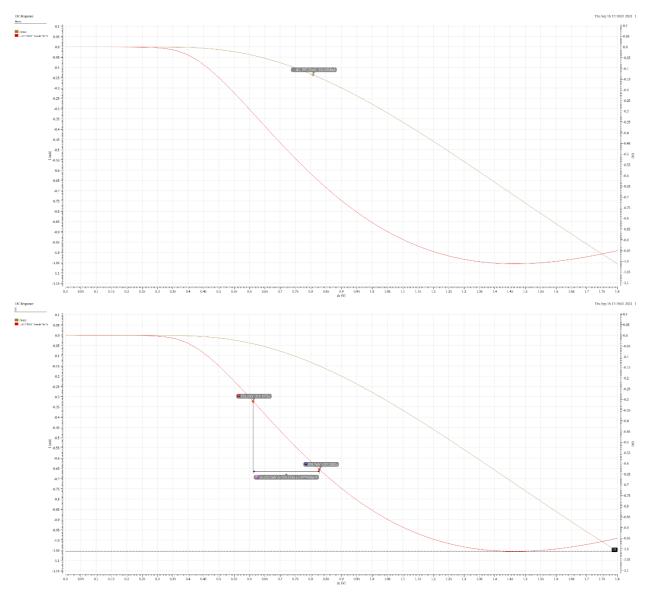
The NMOS transistors had differences depending on the width and length of the transistor. The initial change in width resulted in a significant increase in the amount of current through the system for the larger transistor. The change in length created a much larger gain for the system.

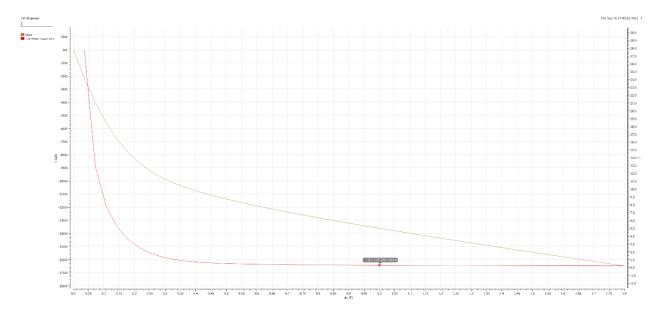
PMOS Information Schematic

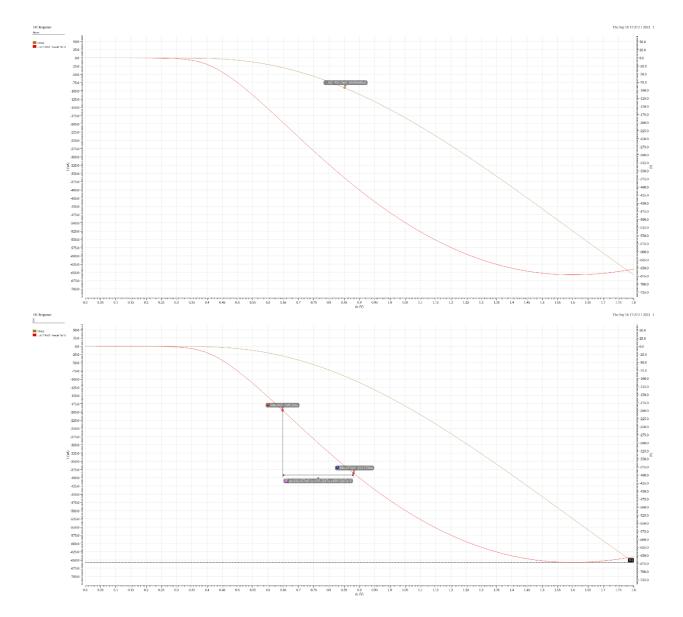


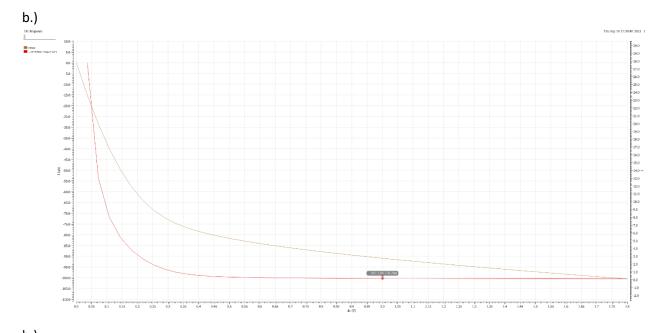


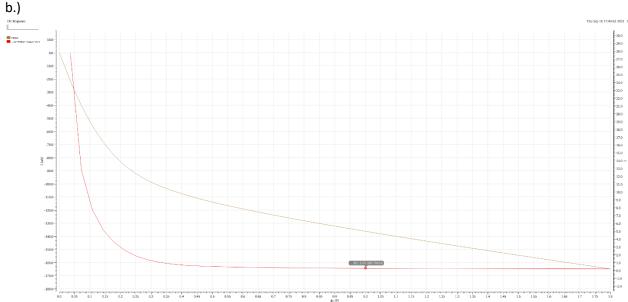












Unfourtunatly My computer lost the ability to run ADE_L commands for some reason so I was not able to capture the values for part c for the PMOS transistors...

The PMOS devices were all similarly different from each other mirroring the NMOS devices differences we found in the previous section. The main difference between the PMOS and NMOS was that the amount of current typically gained was smaller than the equivalent gains found in the NMOS. The

changes to the width were such that the larger transistors had a much higher current gain than the smaller transistor. The length change created a much larger gain of the system while keeping the lambda value almost identical.