ECEN 474/704 Lab 5: Current Mirrors

Introduction

Current mirrors are fundamental building blocks of analog integrated circuits. Operational amplifiers, operational transconductance amplifiers and biasing networks are examples of circuits that are composed of current mirrors. Analog integrated circuit implementation techniques such as current-mode and switch-current use current mirrors as the basic circuit element. The design and layout of current mirrors is therefore an important aspect of successful analog circuit design.

In the simplest form, a current mirror is composed of only two transistors as shown in Figure 5-1. Transistor M_1 is diode connected and acts as the low-impedance input of the current mirror. The drain of M_2 is the output of the current mirror.

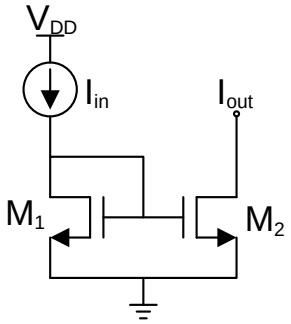

Figure 5-1: Simple Current Mirror

Since the gate-to-source voltage is the same for both transistors, according to the first-order MOSFET model, the drain currents will be equal. This assumes that the transistor sizes are equal as well as the process parameters.

A current mirror is used to mirror the input current into the output branch. A current (I_{in}) entering the diode-connected transistor establishes a gate voltage (V_{GS}), which causes I_{out} to flow through the output transistor. Notice that the input transistor will show a low small-signal resistance ($1/g_m$) and the output transistor will exhibit a high small-signal resistance (r_0).

If the ratio of the transistors is changed, then the current-mirror acts as a current amplifier. The gain of the amplifier is given by:

$$A_i = \frac{W_2/L_2}{W_1/L_1}$$

The above analysis assumes ideal operation of the current mirror, meaning that the drain currents are independent of V_{DS}. However, due to channel length modulation we know that this is not true. The following equation illustrates the dependence of drain current on V_{DS}:

$$I_D = \frac{1}{2} KP \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

The excess current due to differences in V_{DS1} and V_{DS2} will cause a difference between I_{D1} and I_{D2}. To reduce "lambda" effects, the drain-to-source voltage of the two transistors needs to be held equal.

Another non-ideality of current mirrors is the limited range of V_{DS2}. M_1 remains in saturation for all input currents due to its diode connected configuration and M_2 will enter the triode region if its drain-to-source voltage drops too low, resulting in the output current being much less than what is desired. The minimum output voltage required for the current mirror is sometimes referred to as the compliance voltage. For the simple current mirror, the compliance voltage is $V_{DS,sat2}$.

The ratio of the input to output currents is also process dependent. Because of this process dependency, good layout techniques such as interdigitized and common-centroid methods are used to layout current mirrors.

As previously mentioned, to obtain good matching between input and output currents, the drain-to-source voltages of M_1 and M_2 must be held equal. One way to achieve this is by using a cascode current mirror which is shown in Figure 5-2.

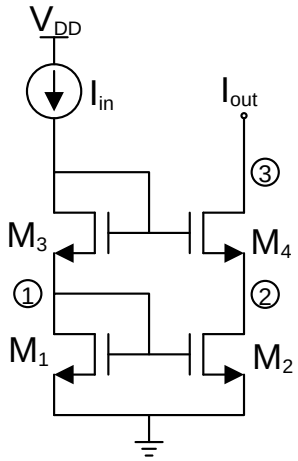

Figure 5-2: Cascode Current Mirror

Transistors M_1 and M_2 determine the ratio of the input and output currents. M_3 biases M_4 which is used to control the drain voltage of M_2. If designed correctly, V_{DS1} is approximately equal to V_{DS2}. The benefits of the cascode current mirror are better matching of output currents and larger output resistance. The disadvantage is that a larger compliance voltage is needed to keep both M_2 and M_4 in saturation. To find the compliance voltage, loop and node analysis will be used as follows:

- **Node 1:** The voltage here is $V_{GS1} = V_T + V_{DS,sat1}$.
- **Node 2:** For good matching between input and output currents, we want V_{DS1} and V_{DS2} to be equal. Thus, the voltage at Node 2 is also $V_T + V_{DS,sat1}$.
- **Node 3:** The minimum compliance voltage will be the minimum voltage to keep M_4 in saturation. This will be $V_T + V_{DS,sat1} + V_{DS,sat2}$.

Adding the cascode transistor does not just increase the required compliance voltage by one $V_{DS,sat}$, it also increases the threshold voltage. If the overdrive voltage is 200 mV for all transistors with threshold voltages of 700 mV, the output voltage will have to be greater than 1.1 V. This makes cascode current mirrors not desirable for modern processes, since the required supply voltage is already small.

In order to have the good current matching capabilities of the cascode current mirror, while not having such a large compliance voltage, we can use the low voltage cascode current mirror as shown in Figure 5-3. If designed correctly, M_1 and M_2 will be biased such that they are at the edge of saturation with $V_{DS} \approx V_{DS,sat}$, therefore the compliance voltage drops to $V_{DS,sat2} + V_{DS,sat4}$. This is one whole threshold voltage less than

the regular cascode current mirror of Figure 5-2. M_B will usually have a small W/L ratio, and should have a $V_{DS,sat} = V_{DS,sat1} + V_{DS,sat3}$.

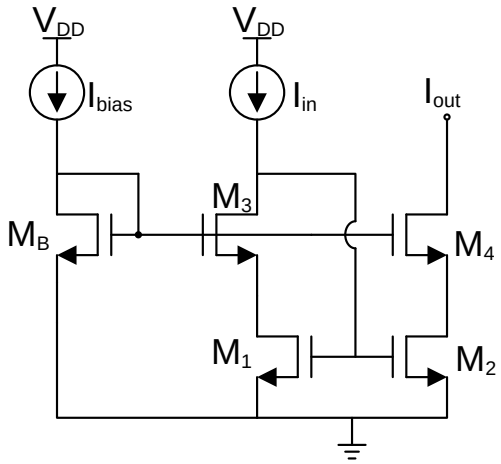

Figure 5-3: Low Voltage Cascode Current Mirror

Simulating Current Mirrors

Once a current mirror has been designed using hand calculations, use the test configuration in Figure 5-4, where I_{in} is the reference DC current and V_{out} is a DC voltage source that will be varied in a DC sweep simulation. After running the simulation, I_{D2} can be plotted by choosing *Results→Direct Plot→DC*, then clicking on the (-) terminal of the voltage source V_{out}. The resulting I_{D2} versus V_{out} plot should resemble Figure 5-5. The compliance voltage will be the point on the plots where I_{out} begins to change rapidly, indicating that the output transistor is entering the linear region of operation.

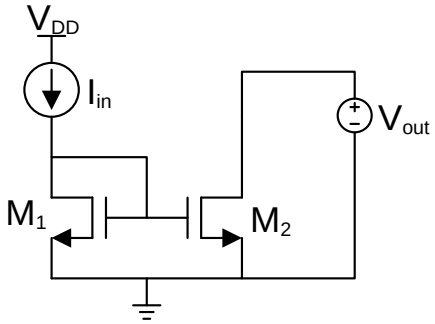

Figure 5-4: Current Mirror Test Configuration

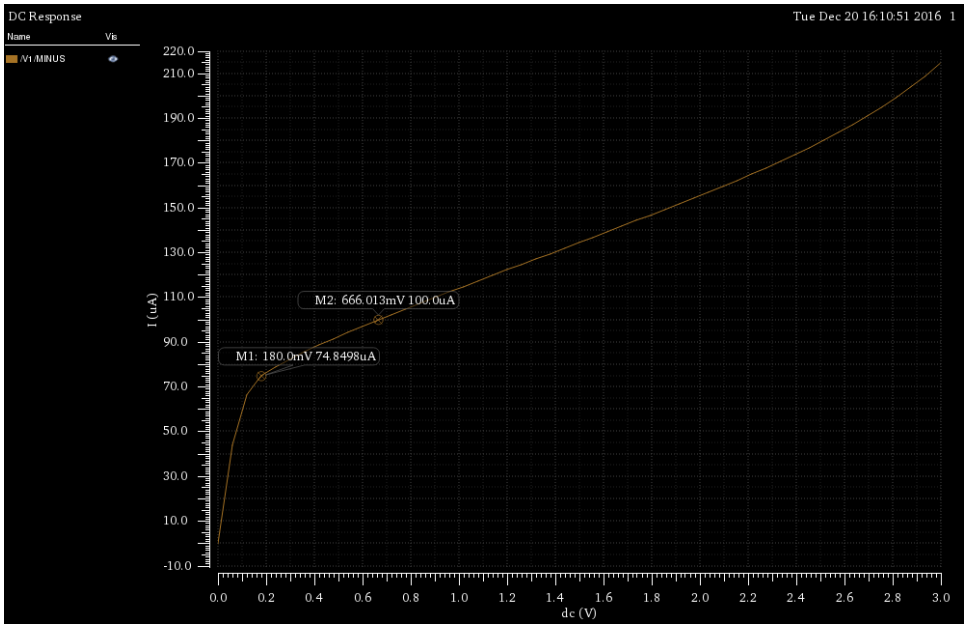

Figure 5-5: Current Mirror Simulation Results for Compliance Voltage

In order to find the output impedance, AC simulation needs to be run. First, assign V_{out} a DC voltage greater than $V_{DS,sat}$ (say 1 V) with an AC voltage of 1 V. Then, go to *Launch→ADE L* and click on *"AC, DC, Trans"* button (or *Analyses→Choose*). Click on *"ac"*, set *Start* to *1* and *Stop* to *100G* for the *Sweep Range.* Change *Sweep Type* to *Logarithmic* and set *Points Per Decade* to *100,* then click *OK* and run simulation.

To plot the output impedance, go to *Tools→Calculator.* First, click on *"vf"* on the Calculator and then the output node (wire) on the schematic. Second, click on *"if"* on the Calculator and then the (-) terminal of the voltage source V_{out} on the schematic. Finally, click on *"/"* on the calculator, and then *Tools→Plot.* The output impedance plot should resemble Figure 5-6. In this example the output impedance is about 24 kΩ at low frequencies and then begins to decrease around 100 MHz.

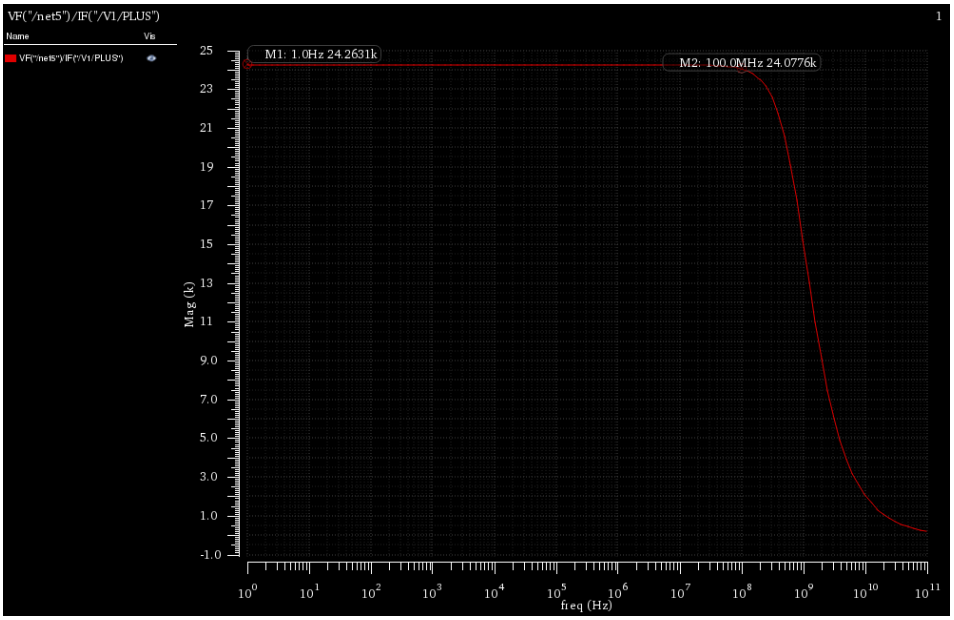

Figure 5-6: Plot of Current Mirror Output Impedance

Prelab

1. Make a table which lists the three current mirror topologies described in this lab. Rate each topology using good, medium and bad for the following design considerations: R_{out}, accuracy, complexity, and compliance voltage.

2. Design a simple 1:1 current mirror that has a compliance voltage of 100 mV to 150 mV. The output current should be 100 µA. Determine W/L for each transistor and what the expected output impedance should be.

3. Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 1 MΩ. Assume a 50 µA input current.

Lab Report

1. Simple current mirror
   a) Design in Cadence the simple current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   b) Generate the plots of Figure 5-5 and Figure 5-6 for this design. Determine the compliance voltage, low frequency output impedance, and comment on accuracy.
   c) Layout the current mirror. Run post layout simulations. Include plots of both layout and schematic simulation in your lab report.

2. Low-voltage current mirror
   a) Design in Cadence the low-voltage cascode current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   b) Generate the plots of Figure 5-5 and Figure 5-6 for this design. Determine the compliance voltage, low frequency output impedance and comment on the accuracy.
   c) Layout the current mirror. Run post layout simulations. Include plots of both layout and schematic simulations in your lab report.

3. Be sure to include in your report the LVS results showing that the layout matches the schematic (again NetID and time stamp required for credit).