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ECEN 326-501

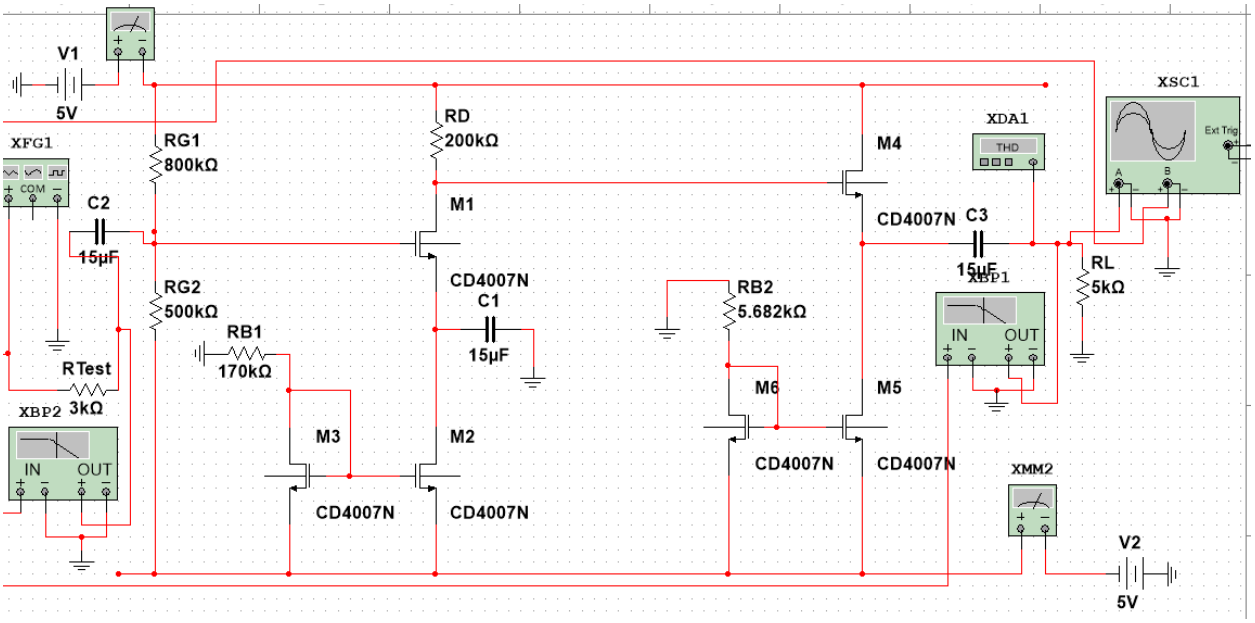
Lab 3: Design of a Two Stage MOS Amplifier

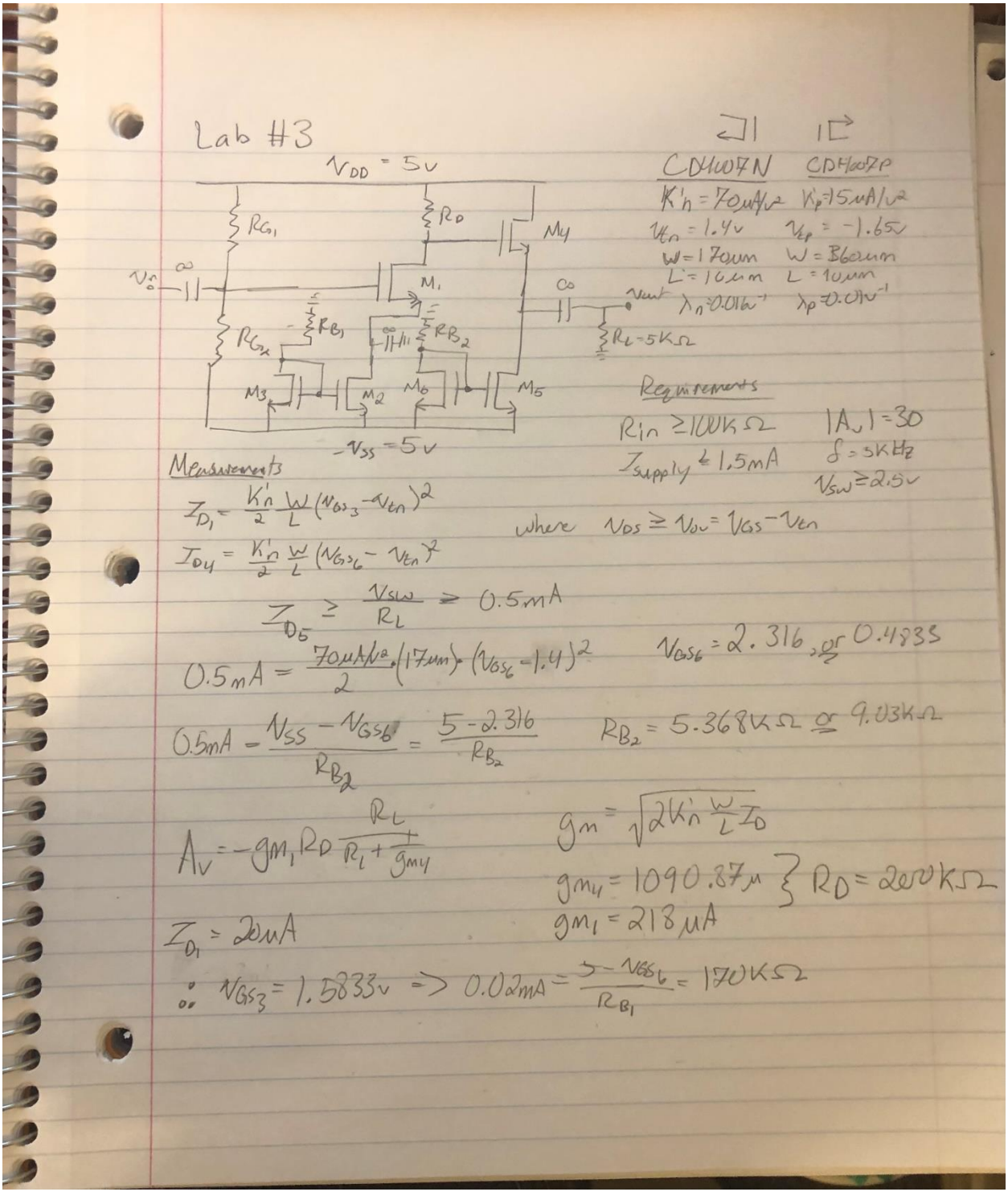
Purpose:

In this lab, we constructed a two stage MOS amplifier to demonstrate the differences between the BJT amplifier we created in the previous labs. We also want to study the effects of a current mirror using the MOS transistor.

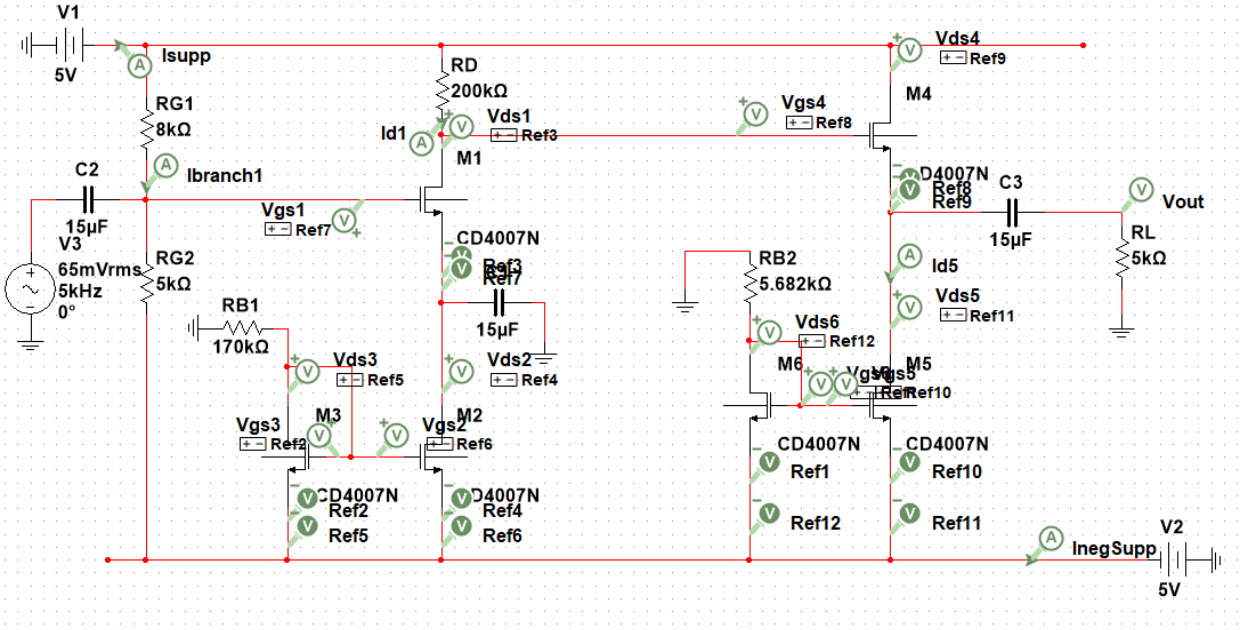
Calculations:

Design (Changed the design to fix my input resistance after we talked in lab):





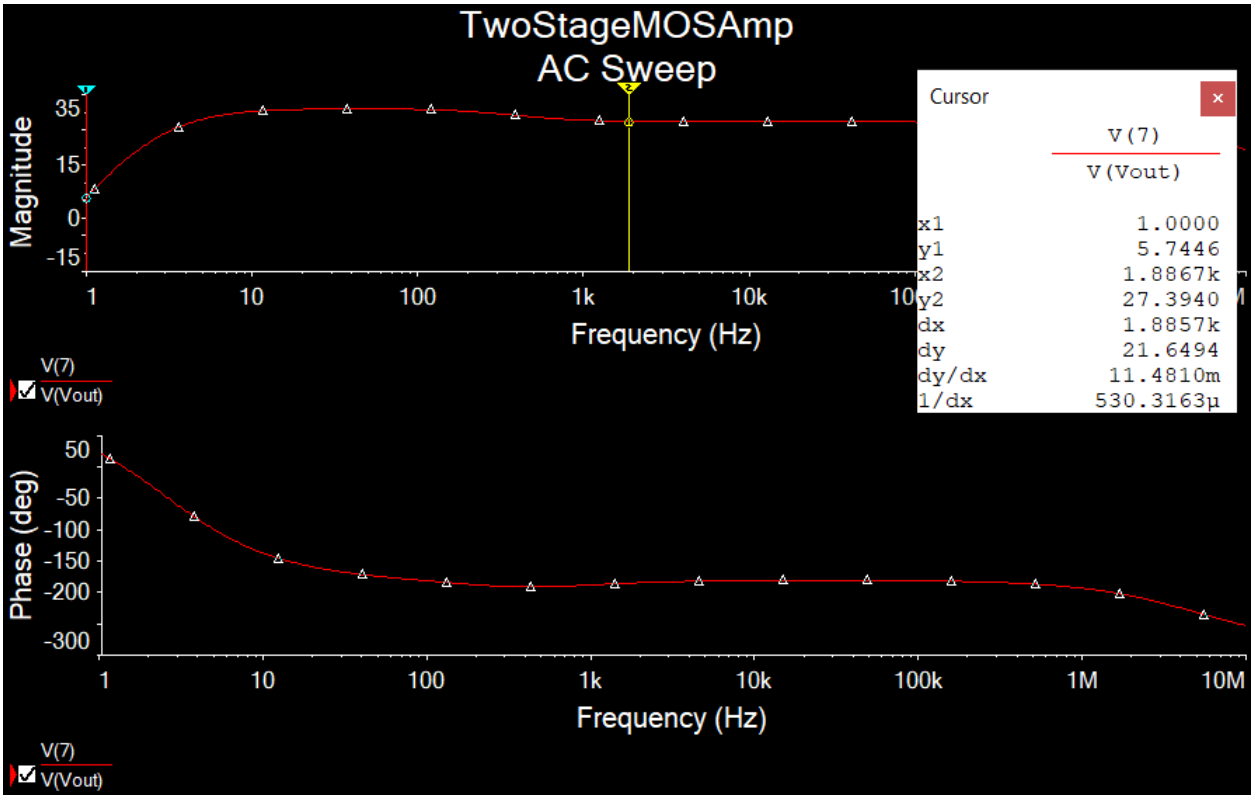
Simulations:



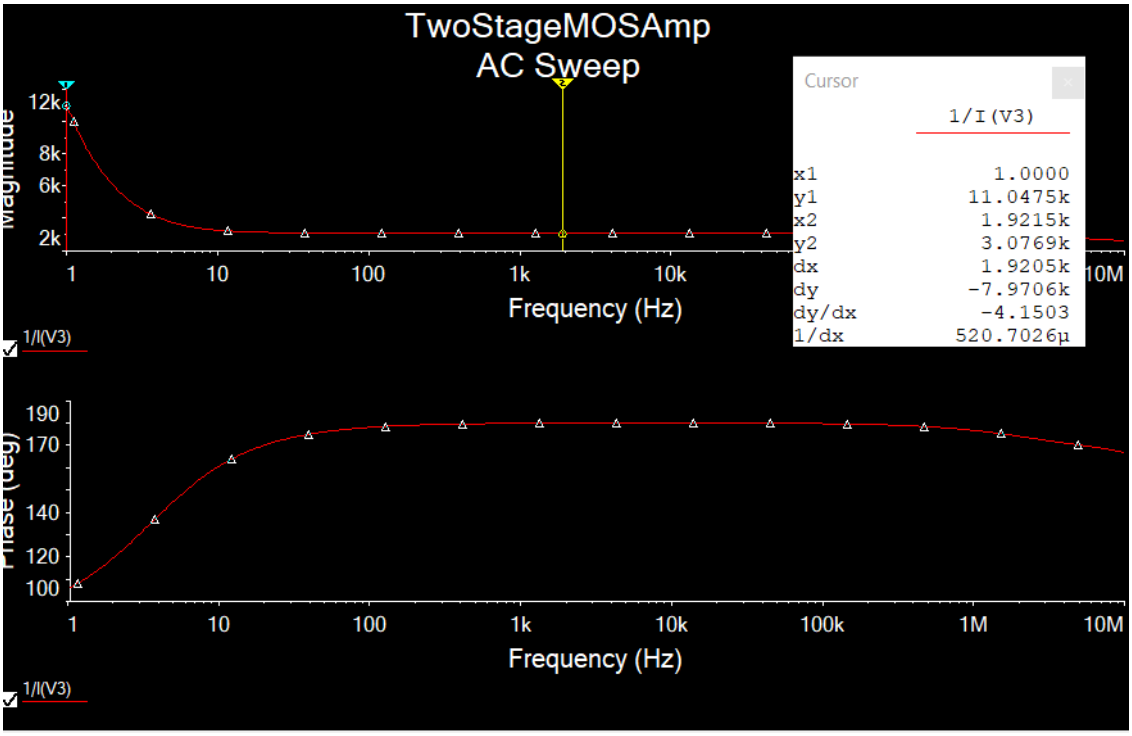
DcOp:

	Variable	Operating point value
1	-I(RG1:2) | I(Ibranch1)	769.23077 u
2	-I(RD:2) | I(Id1)	20.82017 u
3	-I(vM4.PinVoltageS--2:S)-I(C3:1) | I(Id5)	494.19961 u
4	I(V2:2) | I(InegSupp)	1.78646 m
5	-I(V1:1) | I(Isupp)	1.28425 m
6	V(10) - V(3) | V(Vds1)	3.54734
7	V(3) - V(6) | V(Vds2)	2.28862
8	V(9) - V(6) | V(Vds3)	1.56112
9	V(5) - V(2) | V(Vds4)	6.40585
10	V(2) - V(6) | V(Vds5)	3.59415
11	V(1) - V(6) | V(Vds6)	2.26140
12	V(4) - V(3) | V(Vgs1)	1.55753
13	V(9) - V(6) | V(Vgs2)	1.56112
14	V(9) - V(6) | V(Vgs3)	1.56112
15	V(10) - V(2) | V(Vgs4)	2.24182
16	V(1) - V(6) | V(Vgs5)	2.26140
17	V(1) - V(6) | V(Vgs6)	2.26140
18	V(7) | V(Vout)	0.00000e+00

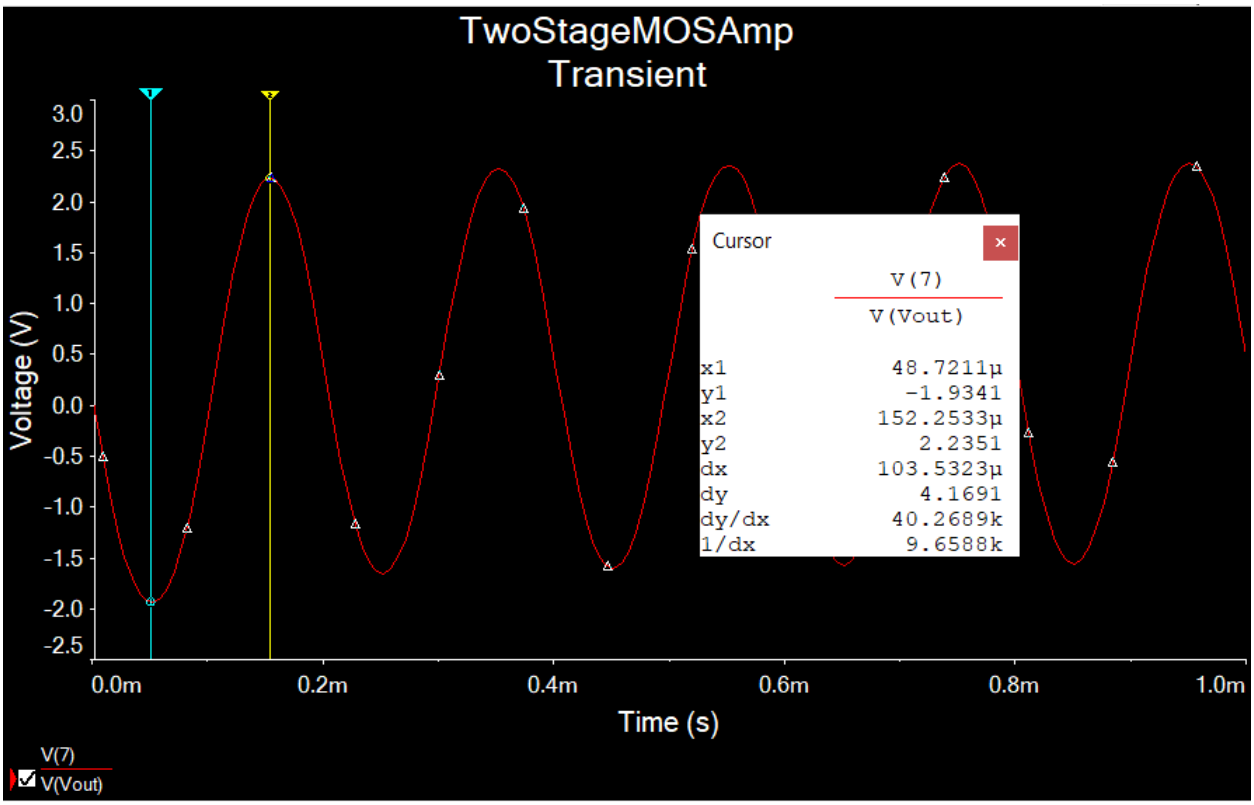
Gain:


TwoStageMOSAmp
AC Sweep
Magnitude
35
15
0
-15
1
10
100
1k
10k
Frequency (Hz)
Cursor
V(7)
V(Vout)
x1 1.0000
y1 5.7446
x2 1.8867k
y2 27.3940
dx 1.8857k
dy 21.6494
dy/dx 11.4810m
1/dx 530.3163µ
V(7)
V(Vout)
Phase (deg)
50
-50
-100
-150
-200
-300
1
10
100
1k
10k
100k
1M
10M
Frequency (Hz)
V(7)
V(Vout)

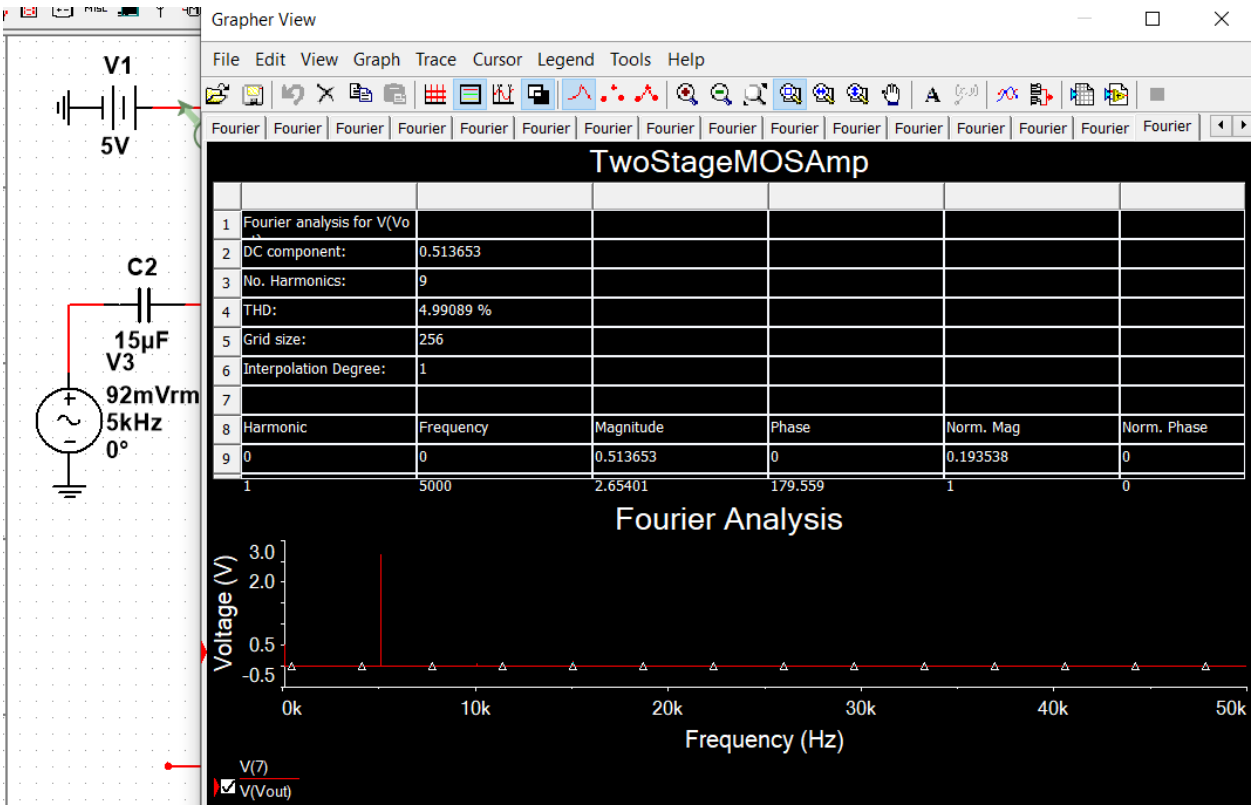
Rin:


TwoStageMOSAmp
AC Sweep
12k
8k
6k
2k
1
10
100
1k
10k
Frequency (Hz)
Cursor
1/I(V3)
x1 1.0000
y1 11.0475k
x2 1.9215k
y2 3.0769k
dx 1.9205k
dy -7.9706k
dy/dx -4.1503
1/dx 520.7026µ
1/I(V3)
190
170
140
120
100
1
10
100
1k
10k
100k
1M
10M
Frequency (Hz)
1/I(V3)

Transient:

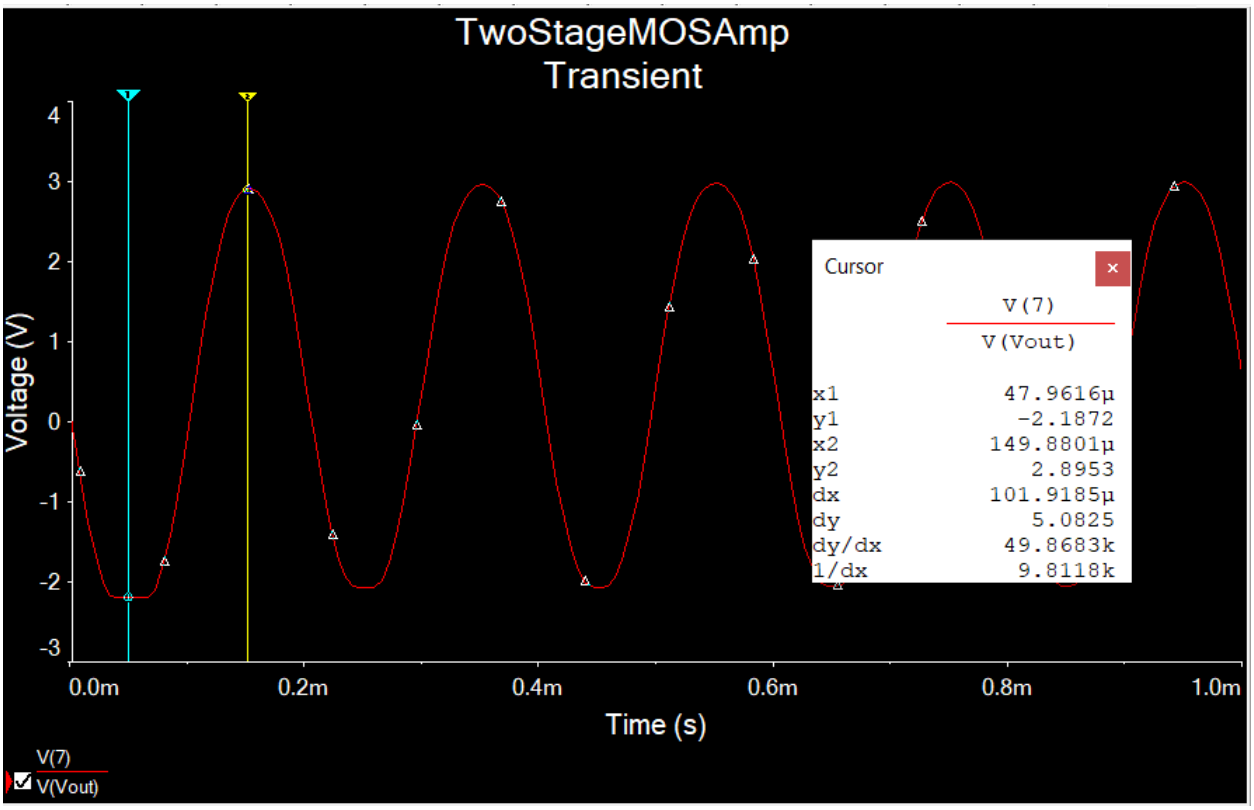


5% THD:



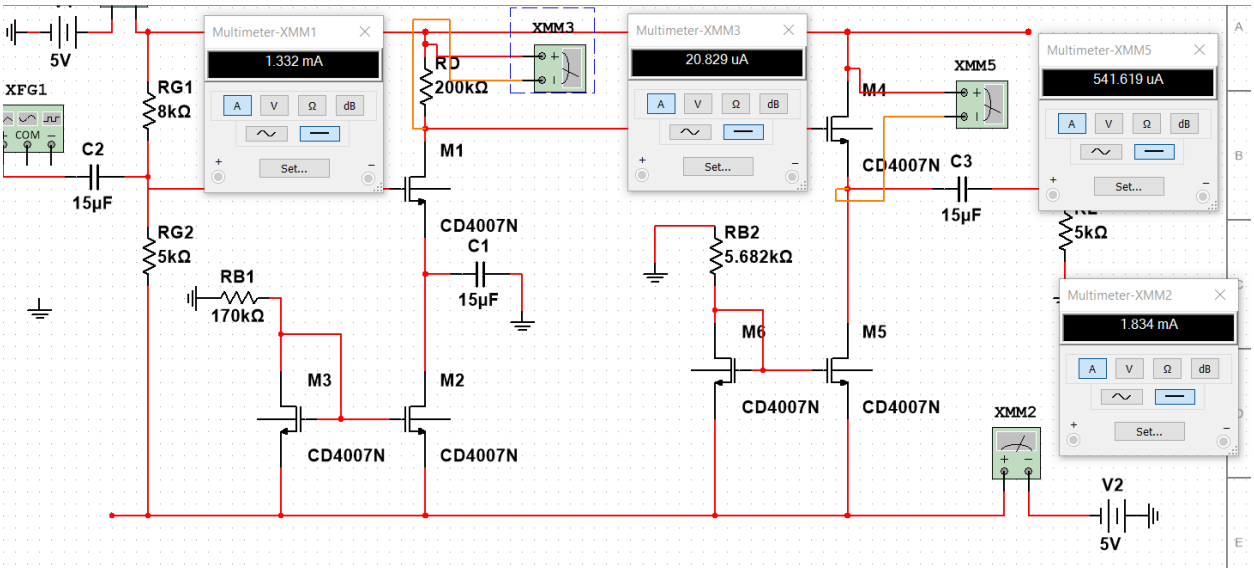
@92mV

Waveform @5%

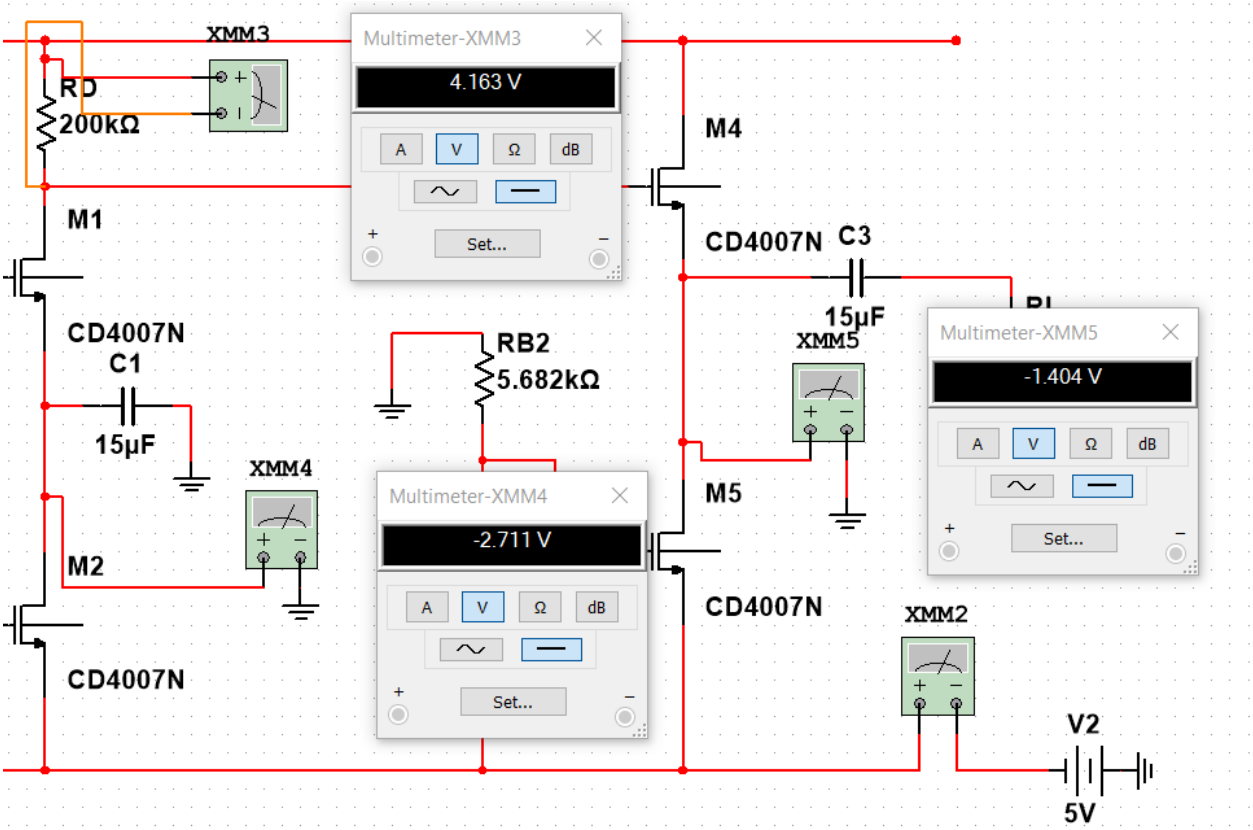


Measurements:

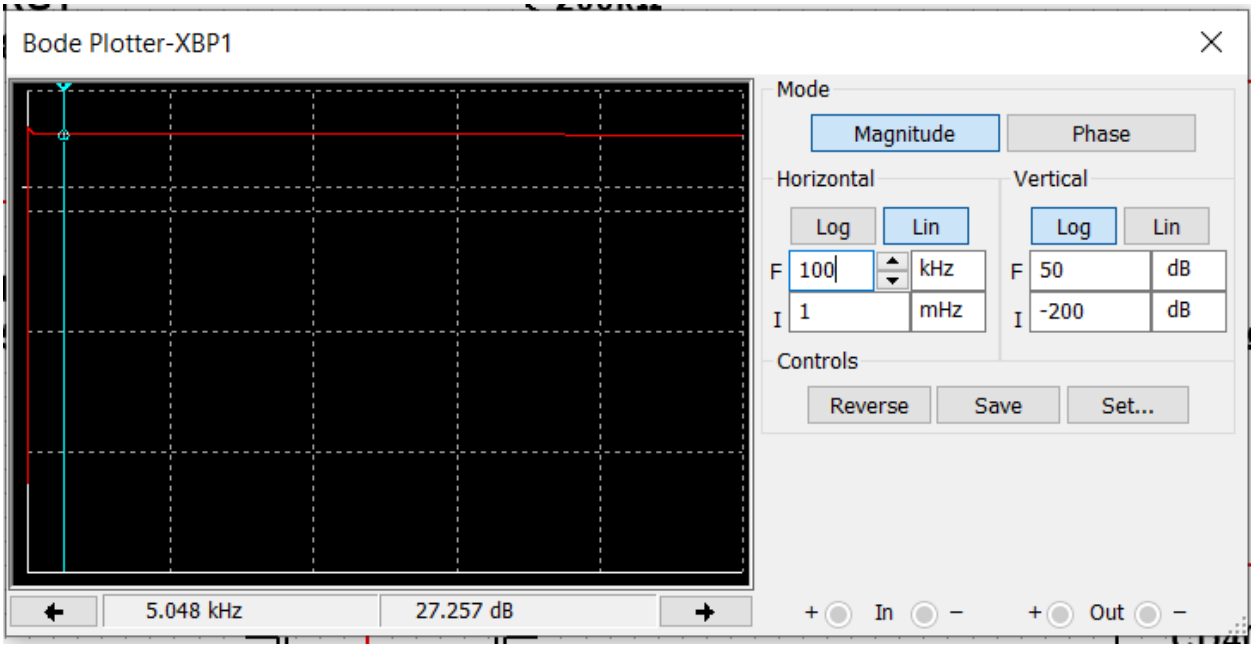
Currents:



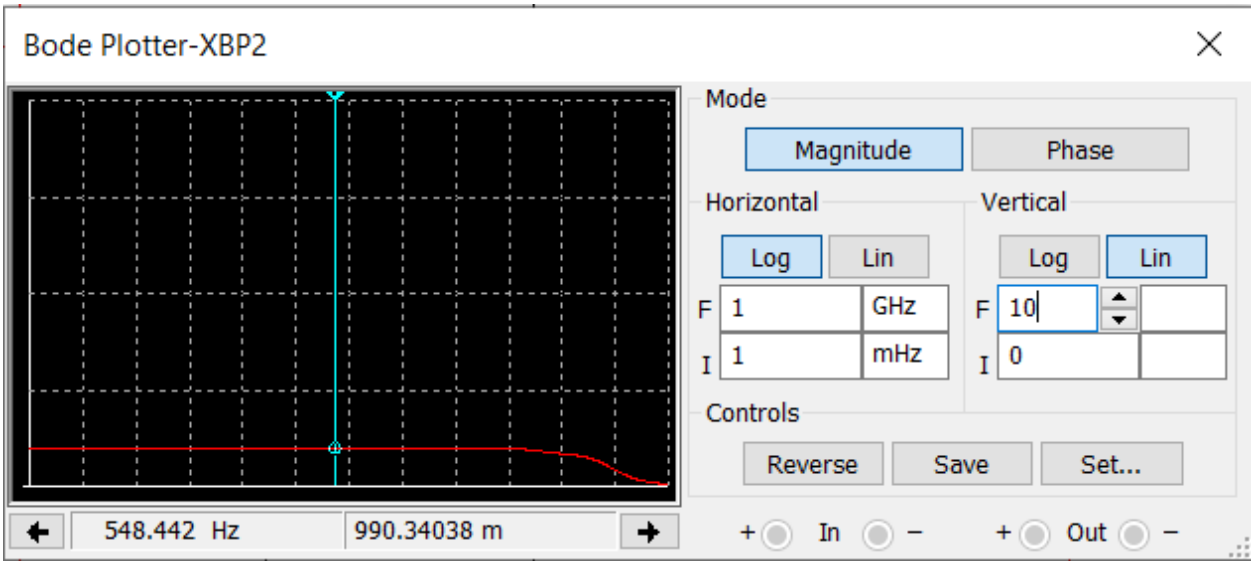
Voltages:



Gain:

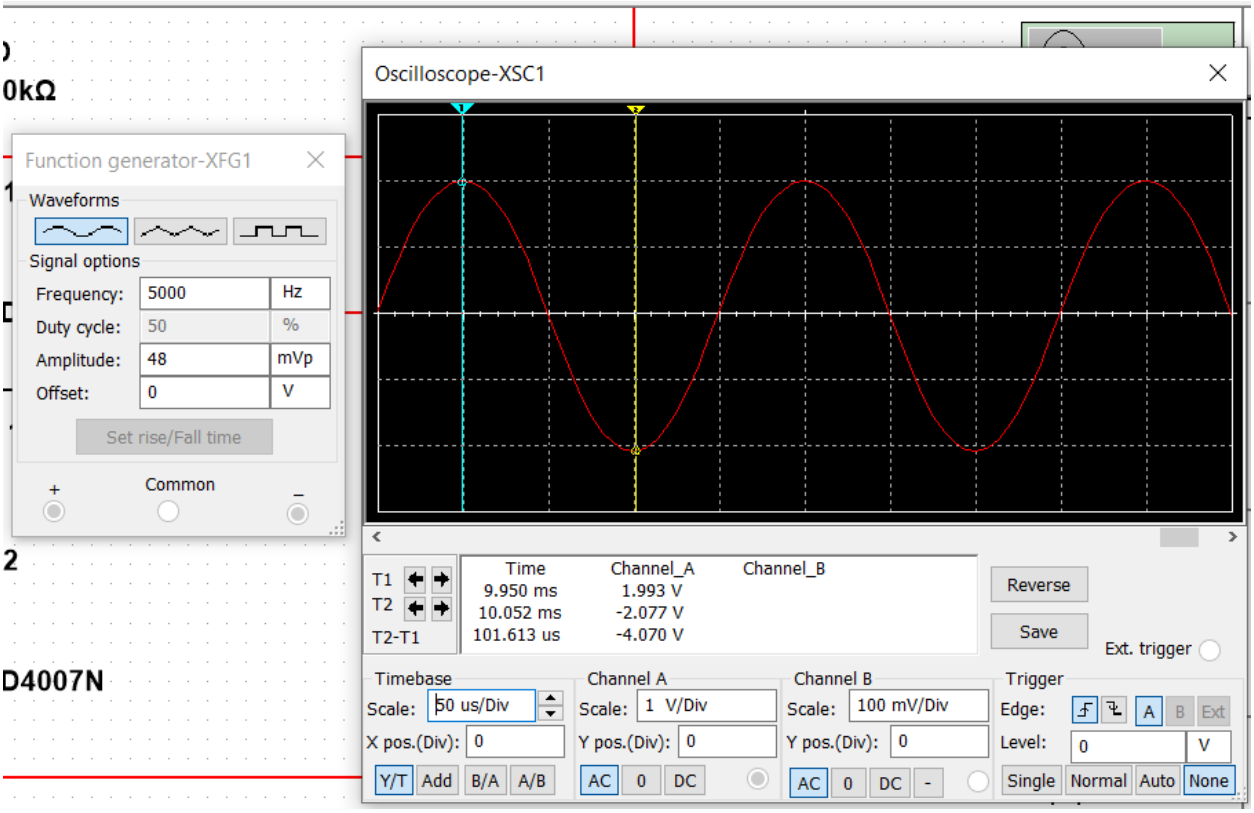


Rin ratio (Rtest = 3k):

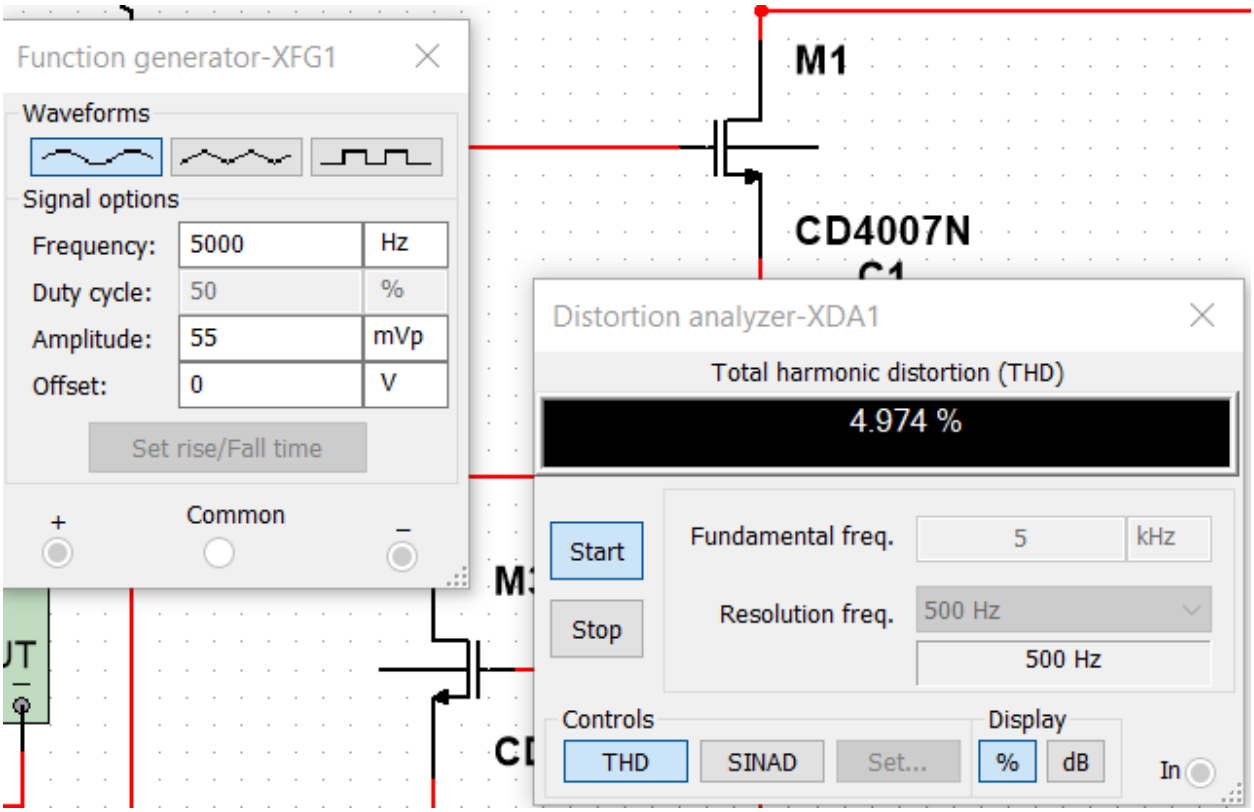


0.99034038=Rin/(Rin + Rtest) => Rin = 297k

Unclipped Output:



5% THD:



Results Explained and Tabulated (Updated after my fix to the initial gate resistors change):

	Calculated	Simulated	Measured
ID1	20uA	20.8uA	20.8uA
ID4	500uA	494.19uA	541uA
Isupply(+)	<1.5mA	522.7uA	593.6uA
Isupply(-)	<1.5mA	1.025mA	1mA
VD1	4v	4.164v	4.641v
VD2	-2.5v	-2.711v	-2.711v
VD5	-1.4v	-1.405v	-1.404v
VGS3	1.5833v	1.5611	1.561v
VGS6	2.316v	2.2614	2.261v
Gain	30dB	27.39dB	27.25dB
Rin	>100k	307.87k	297k
V(0-peak)swing	2.5v	2.89v	2.035v

The biggest challenge I had was getting the input resistance to match the calculated values. I know that increasing the gate resistors would cause my input impedance to increase dramatically at the cost of my supply current. I have gone back and fixed this mistake in my design after I talked with you about my mistake. My input impedance is much higher now and meets the requirements for this lab. A surprise was that the current into the circuit was slightly smaller than

the current out of the circuit. I believe this can be normal however I’m not positive. The negative supply current channel was also 0.2mA higher than I thought it should be for the design which I believe comes from extra current gained from the input voltage.