Matthew Loden

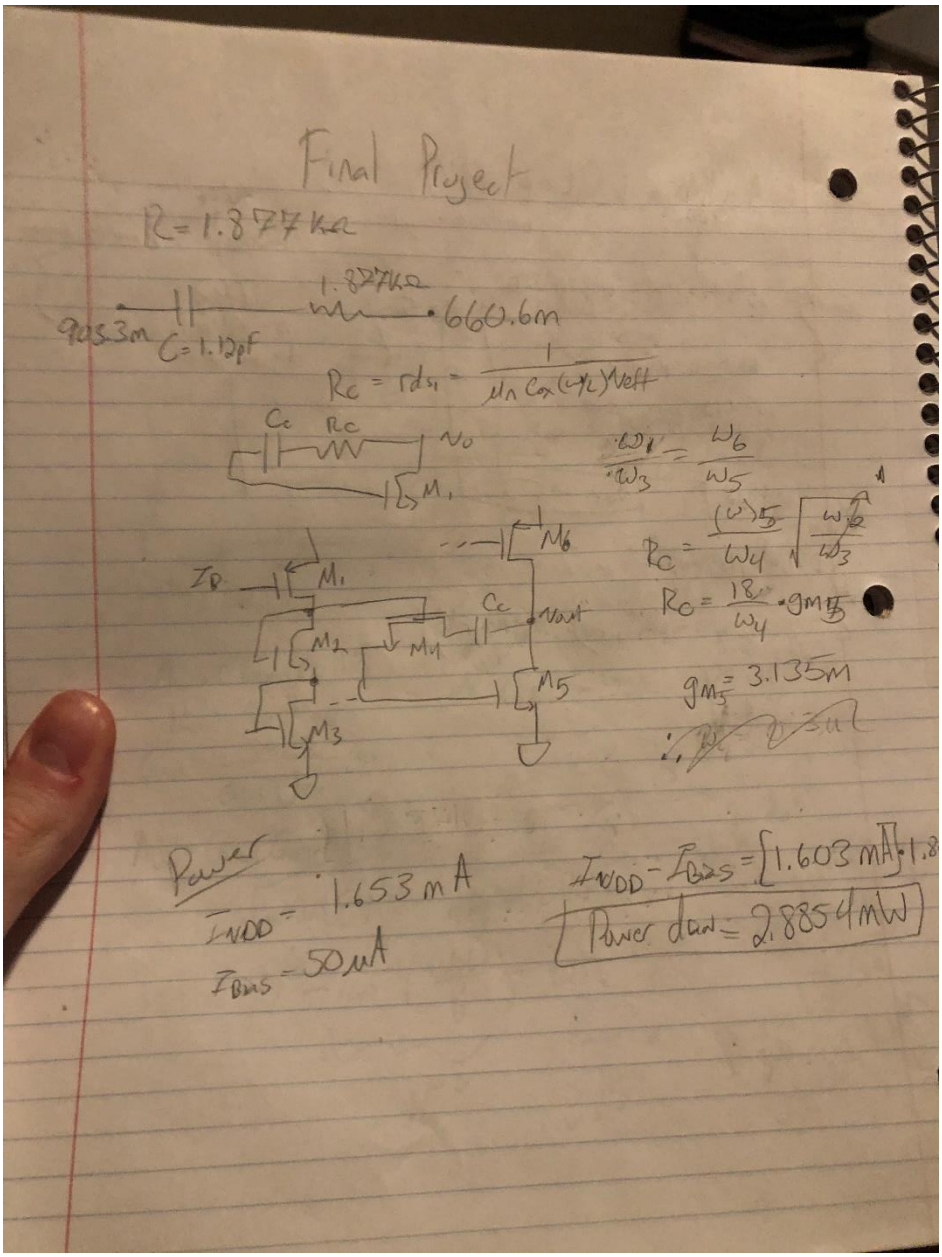
ECEN 474

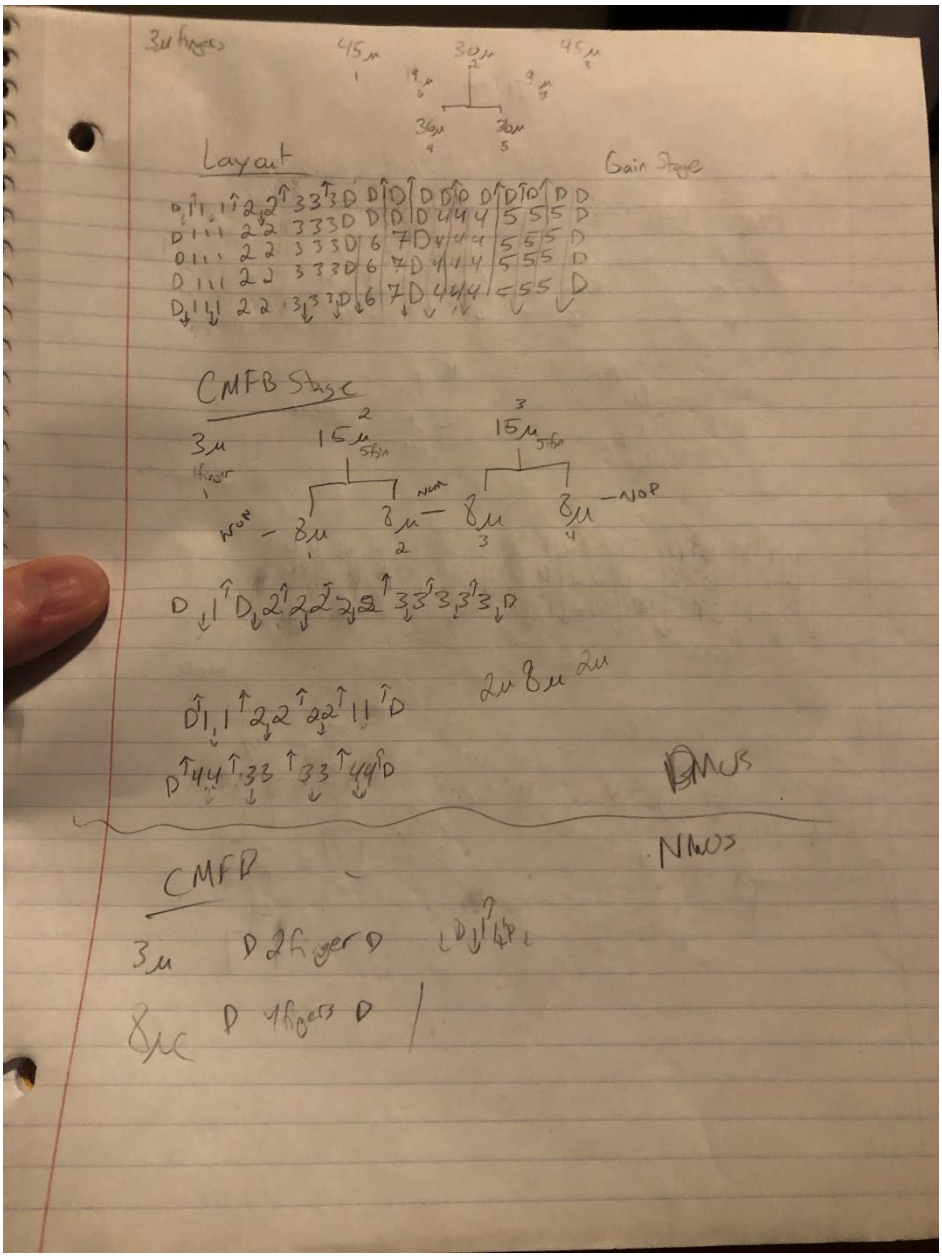
# 474 Final Project: Operational Amplifier with Common Mode Feedback

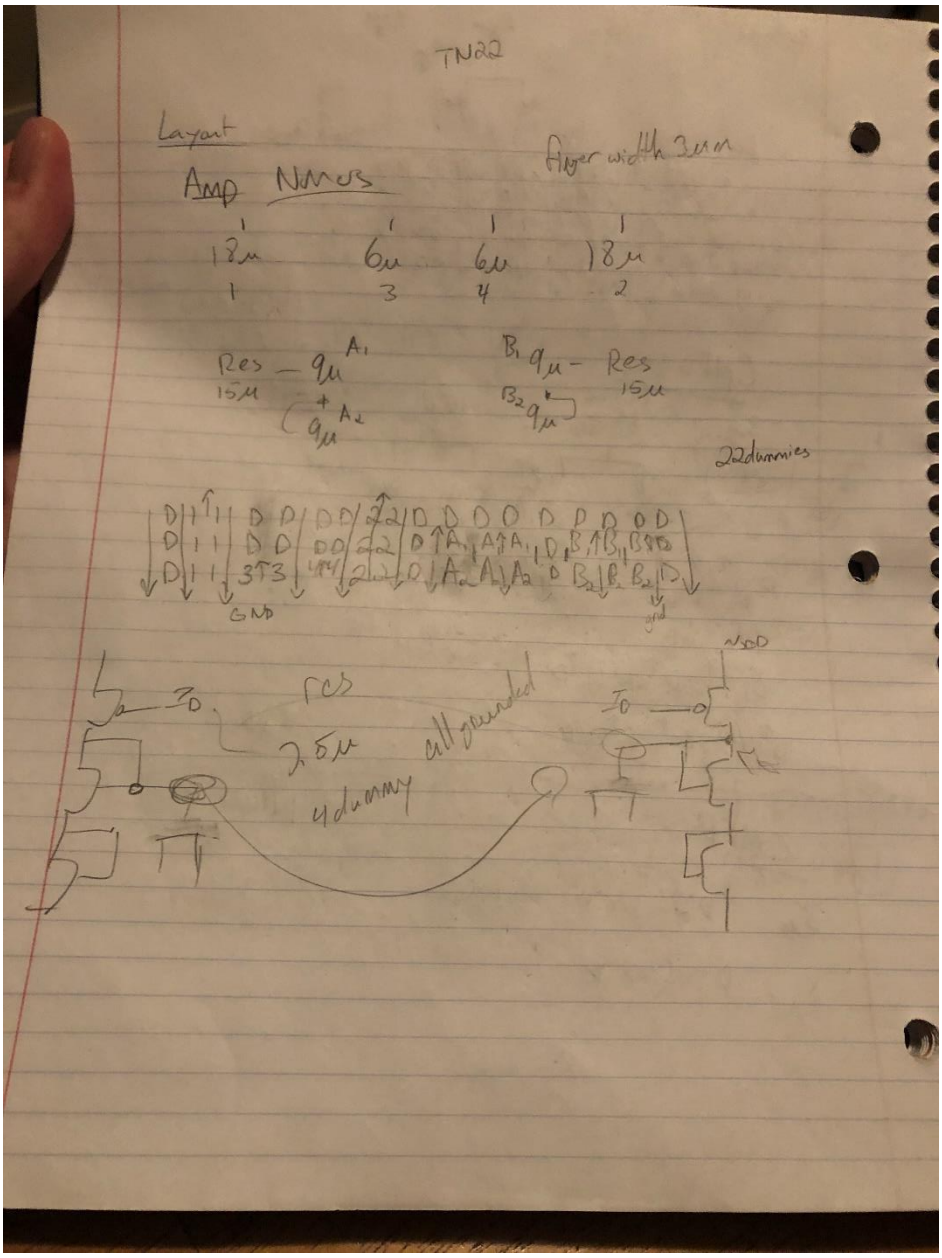
Pre-Design Calculations/Layout Calculations

This lab asked us to create an Operational Amplifier with common mode feedback. As an undergraduate, I was provided with the circuit which would act as a two-stage gain amplifier and the common mode feedback component. The first design choices I made were in relationship to the current mirrors necessary to operate the gain stage. The gain stage needed 20uA of power to be mirrored along its length however the only input was the 50uA from the Pins. To do this, I calculated the necessary sizing and currents through a circuit mirror amplifier to meet this requirement.

My current mirror calculations are shown below:



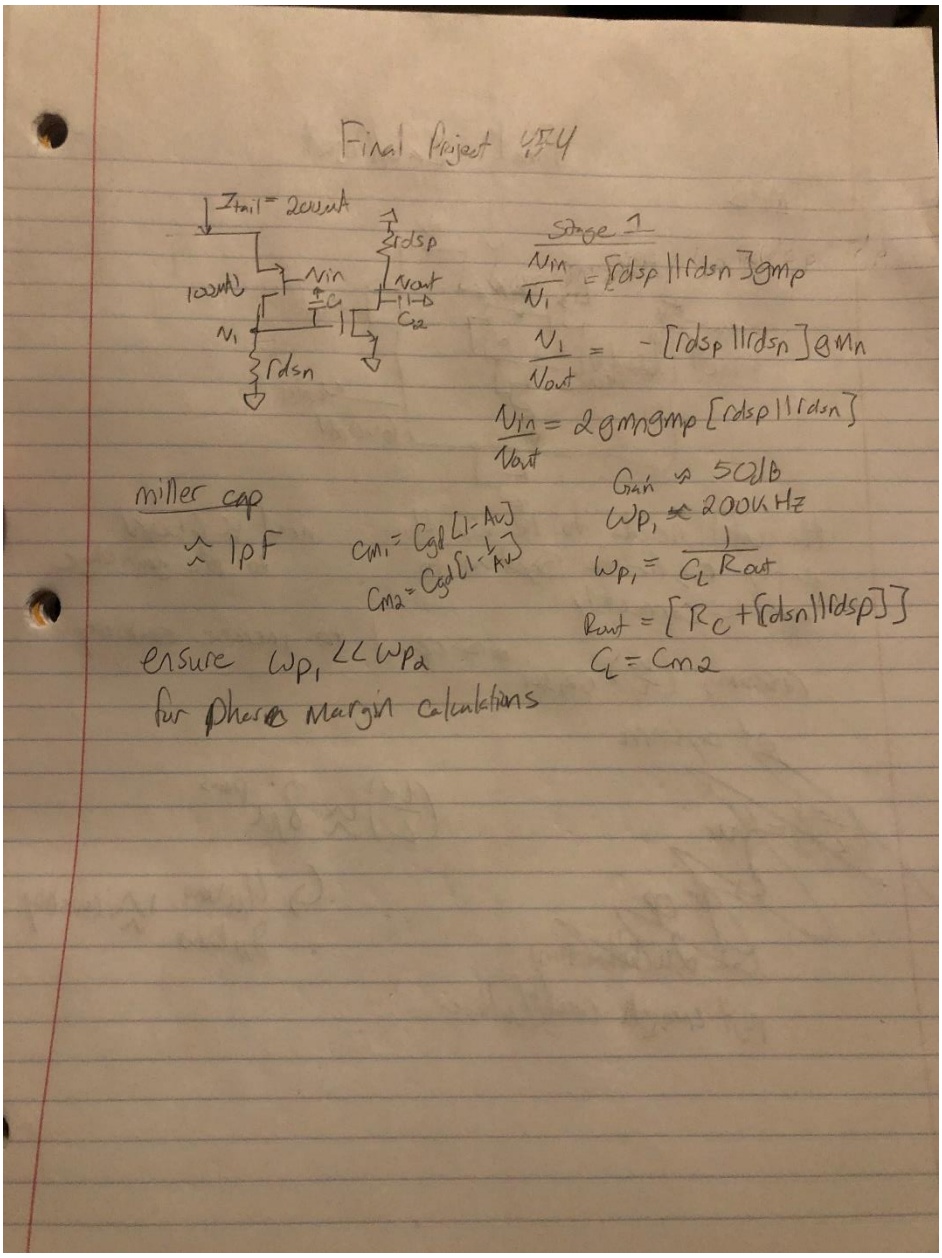

3u fingers
45u
30u
45u
36u
36u
Layout
Gain Stage
CMFB Stage
3u
15u
15u
8u
8u
8u
NMOS
CMFB
3u
8u




It should be noted that slight adjustments needed to be made here for the simulation to work as expected.

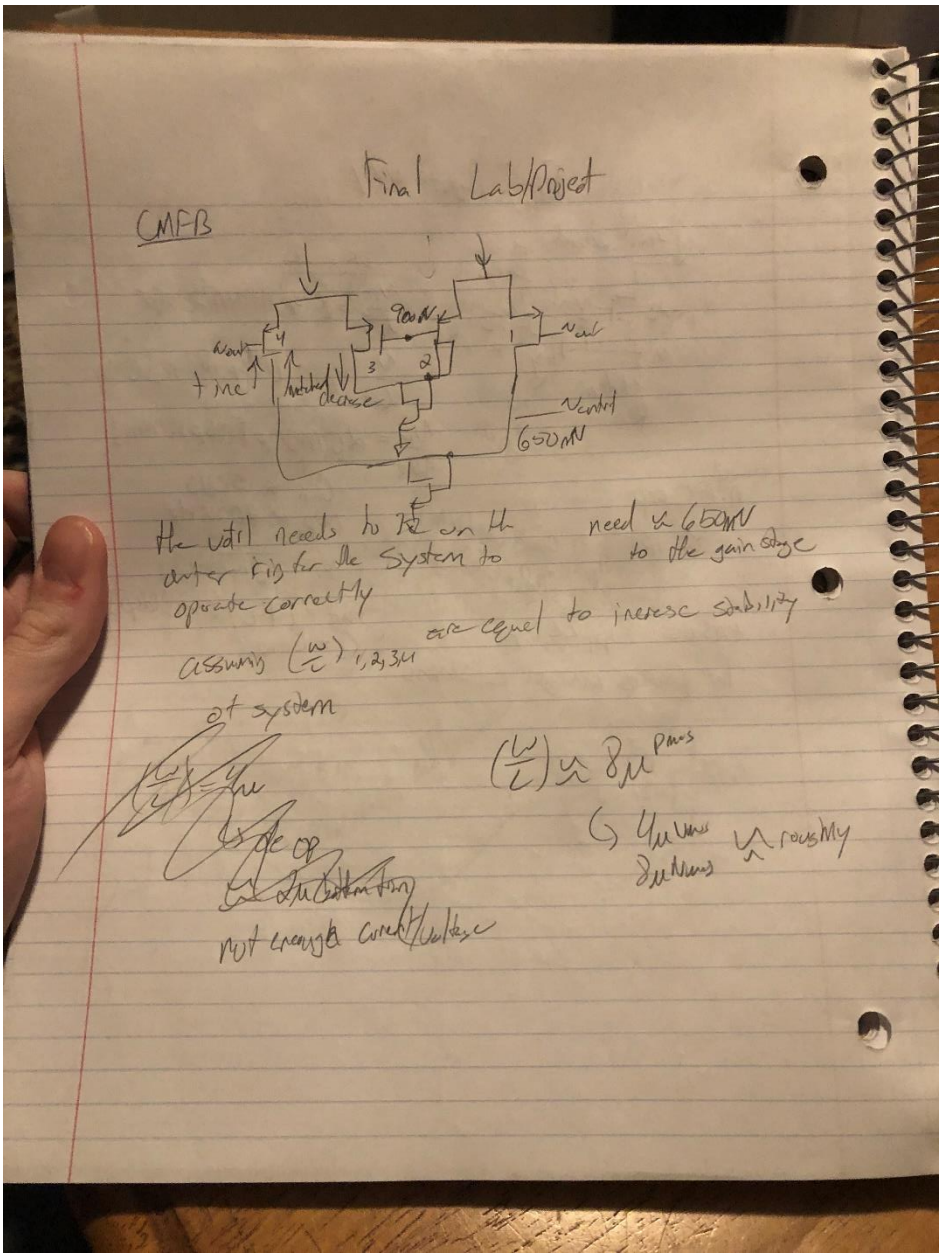
The next expectation was to create the fully differential amplifier. This required me to change how the bottom of the amplifier behaved and include another branch to make the circuit behave in a differential way. The second branch was copied over from the first and a dummy resistor was added on both sides. This resistor would later be revisited and changed into a transistor acting as a resistor. The primary change here was the removal of the diode connected Mosfets on the bottom rail and the inclusion of the voltage bias from the common mode feedback circuit.

My Gain calculations are shown below:




The common mode feedback was designed next with phase margin goals. To meet phase margin, I needed to ensure that proper voltage was supplied to the amplifier stage when needed. The inner rail which was provided for us was diminishing differences in our circuit and the outer rail was amplifying the differences. Due to my output nodes being chosen to be on the same side, my amplifier was an inverting amplifier so for the common mode feedback to work, the outer rail of the circuit had to be chosen to be the feedback voltage.

My calculations for the common mode feedback are shown below:



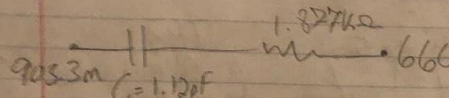

There was some more significant toying with the numbers here as the voltage feedback would change the gain and phase margin more significantly than several other factors.

The last step of design was the resistor that needed to be replaced with a transistor setup. Using the formulas found in the notes provided, I was able to determine the sizing of the transistors. This calculation was most prone to problems however this was compensated by steadily raising the transistor values until desired differential phase margin was reached.

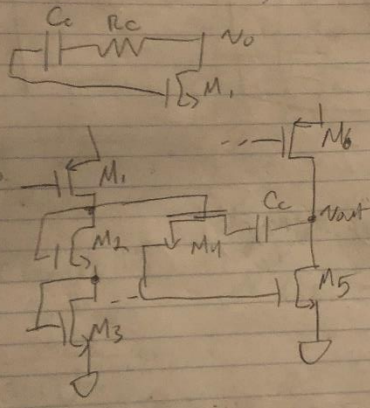
My resistor calculations are shown below:

# Final Project

$R = 1.877\,k\Omega$




$R_C = r_{ds1} = \frac{1}{\mu_n C_{ox} (W/L) V_{eff}}$




$\frac{W_1}{W_3} = \frac{W_6}{W_5}$

$R_C = \frac{(W)_5}{W_4} \sqrt{\frac{W_6}{W_3}}$

$R_C = \frac{18}{W_4} \cdot g_{m5}$

$g_{m5} = 3.135m$

$\therefore$

**Power**

$I_{VDD} = 1.653\,mA$

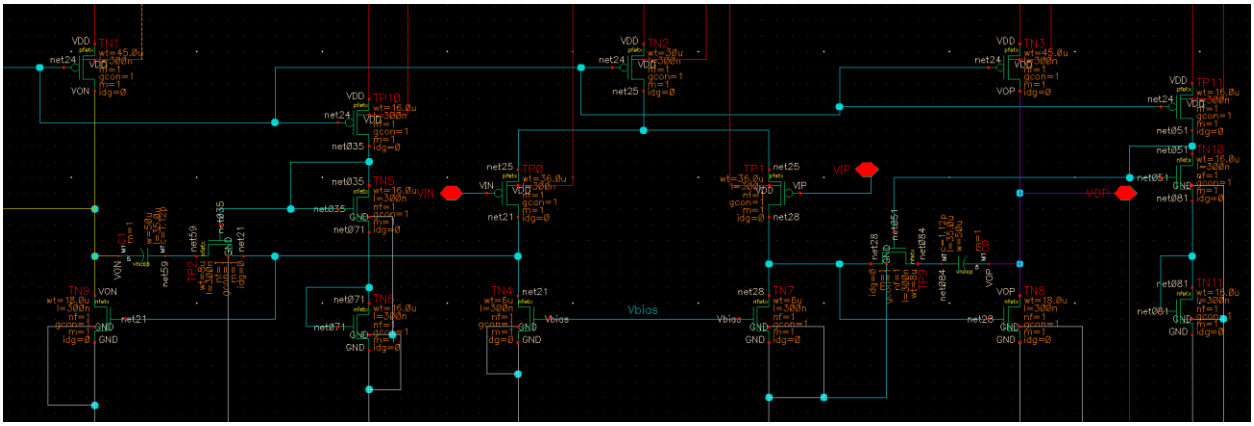
$I_{BIAS} = 50\,\mu A$

$I_{VDD} - I_{BIAS} = [1.603\,mA] \cdot 1.8$

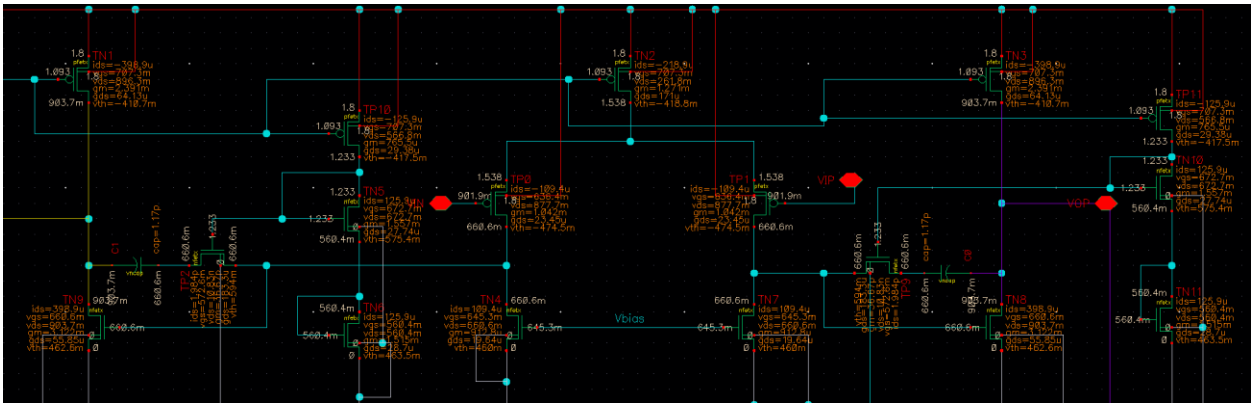
Power dissipation = 2.8854 mW

Schematic Design:

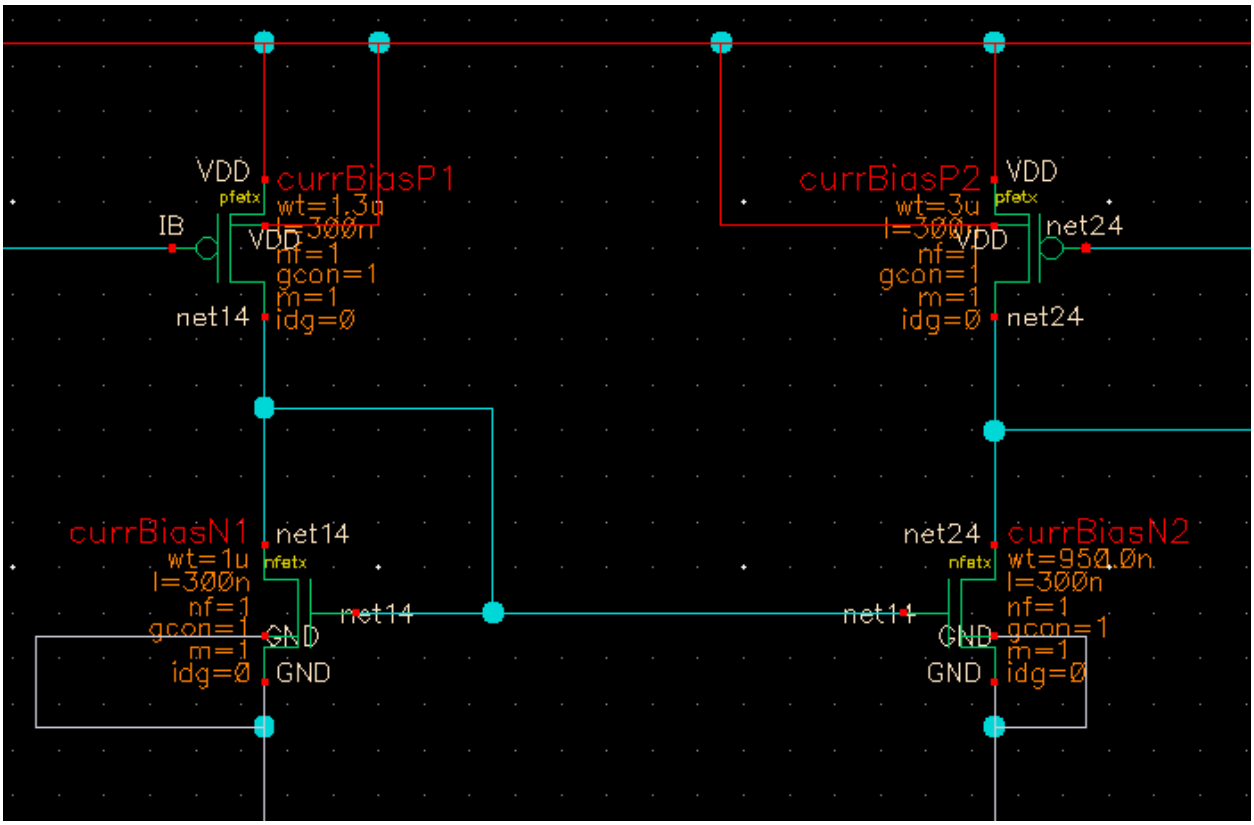
Gain Stage



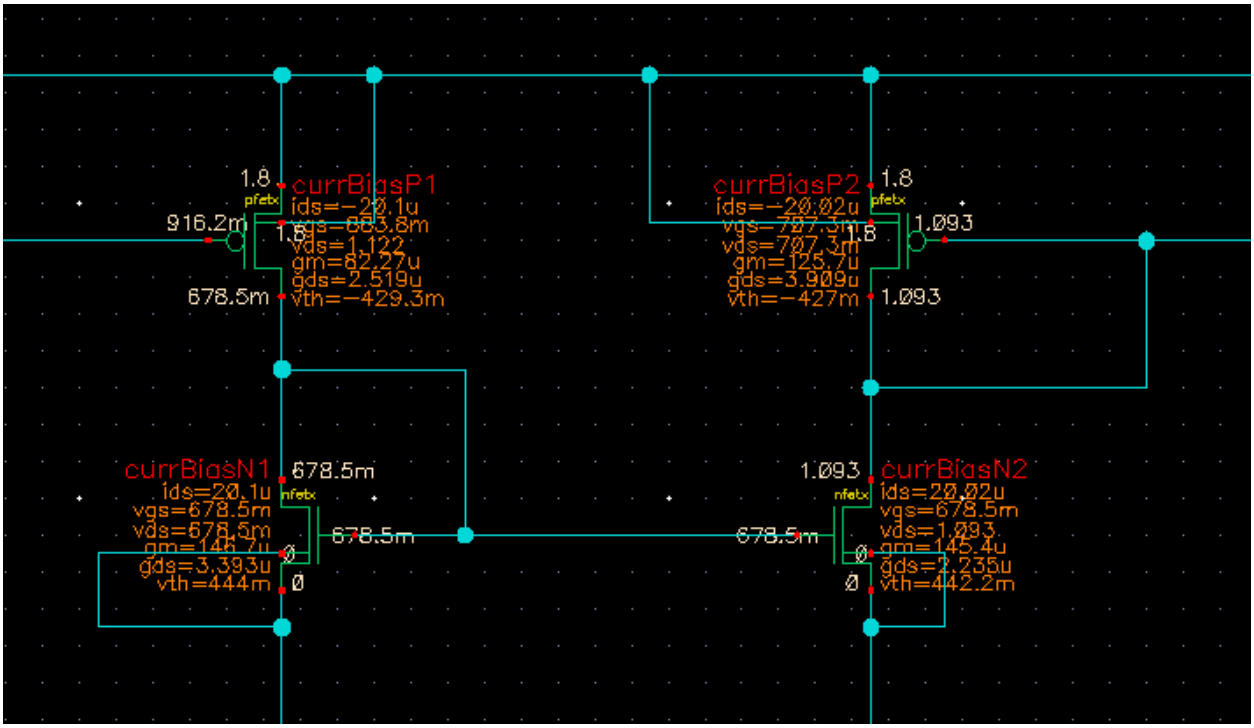
DC Operation Point



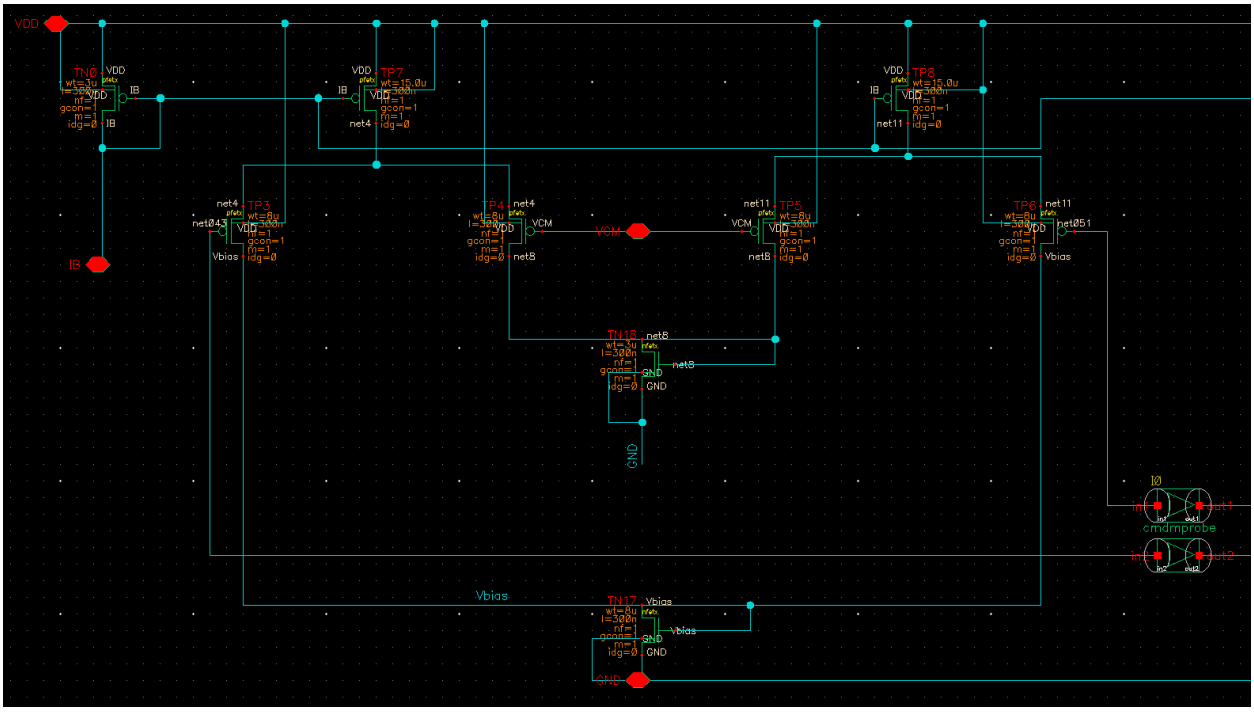
Current Mirror Stage



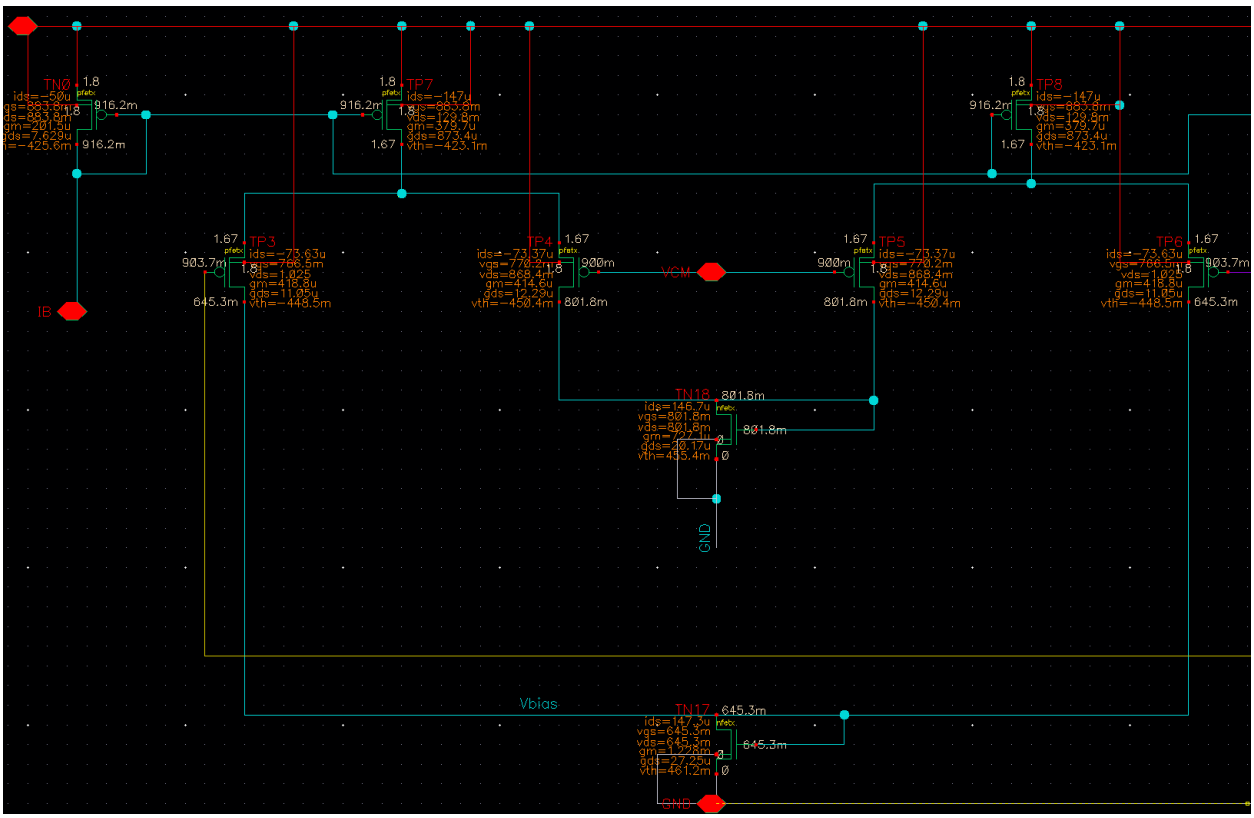

Dc Operation Point




Common Mode Feedback Stage

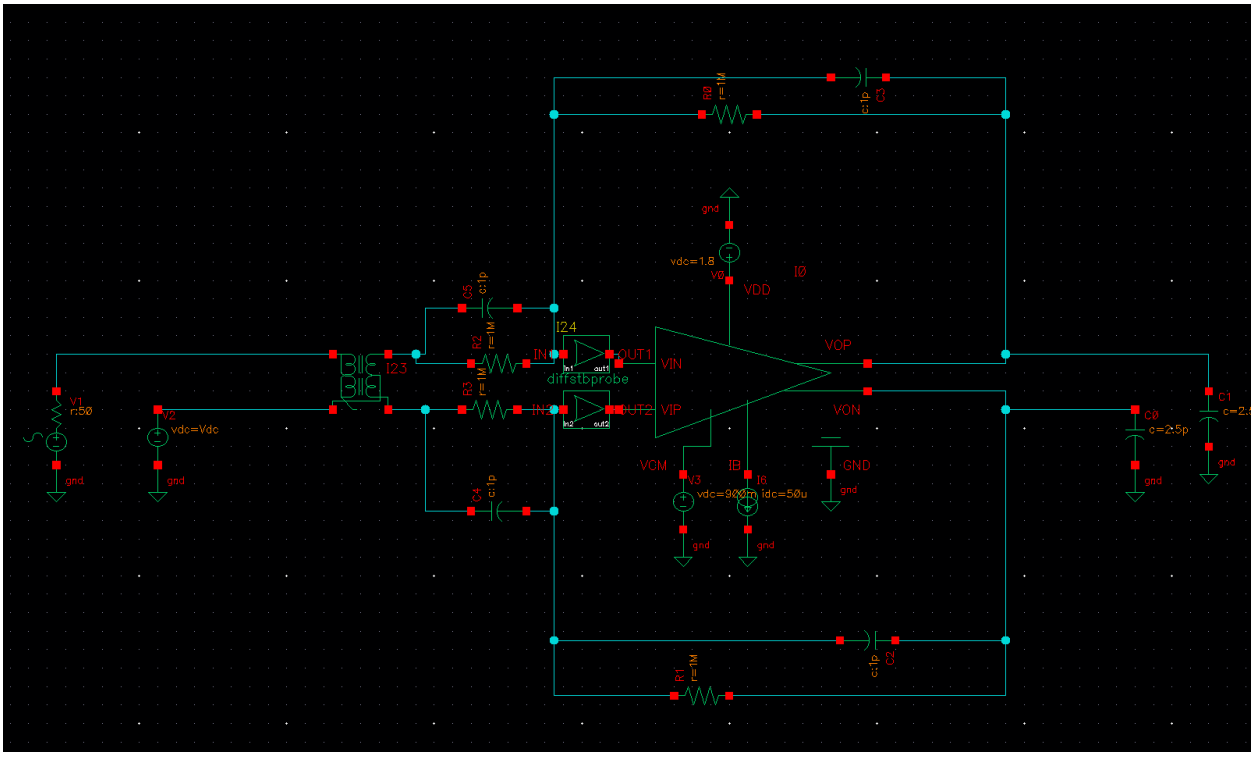



Dc Operation Point

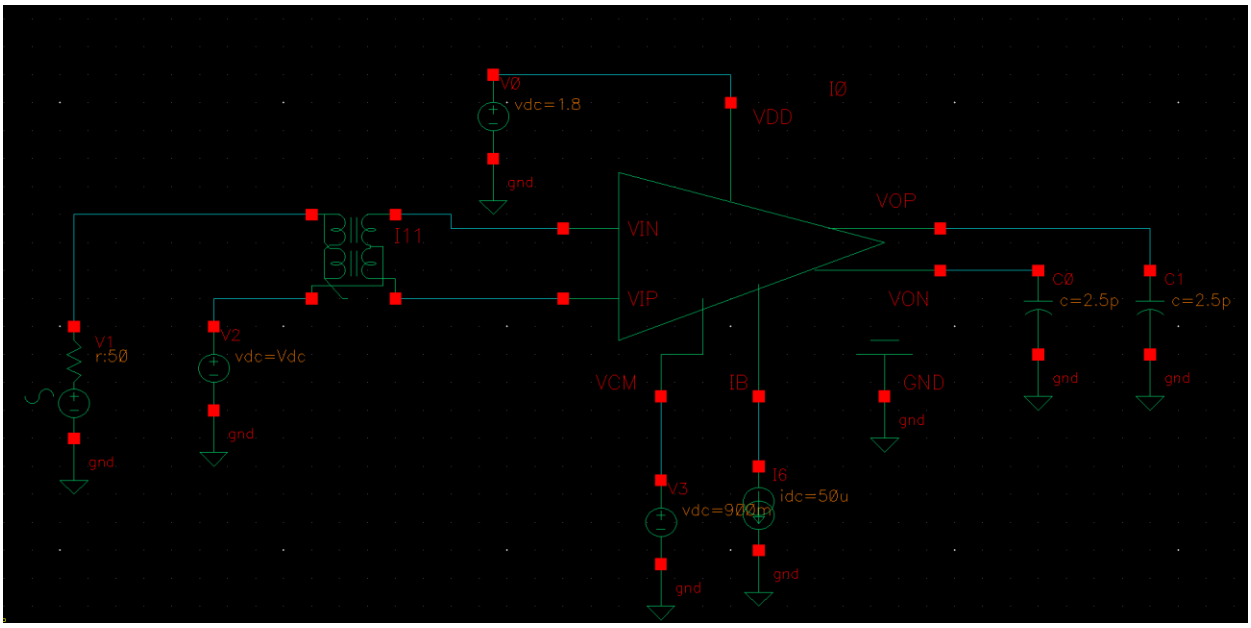


Testbenches Used

Closed Loop:

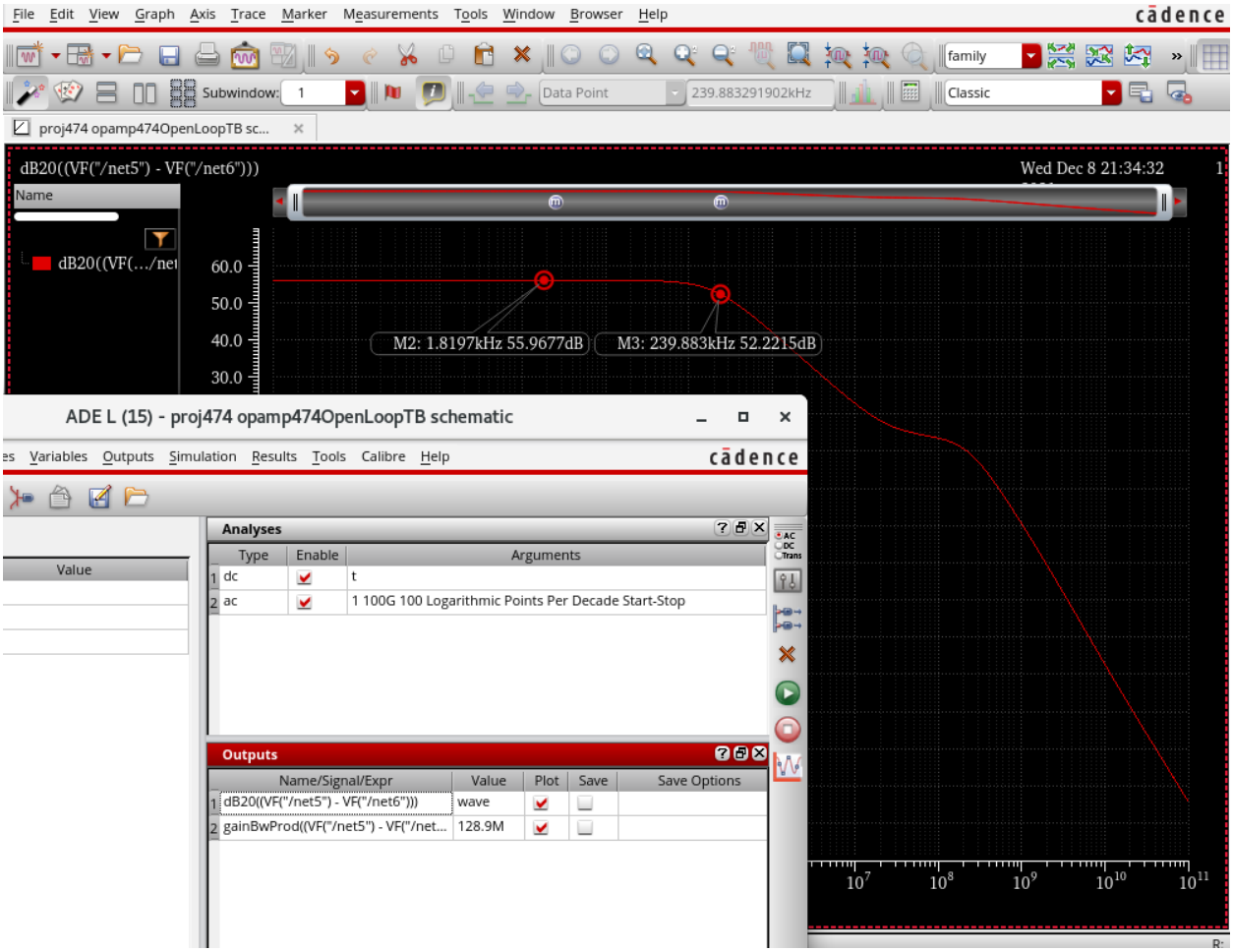



Open Loop:



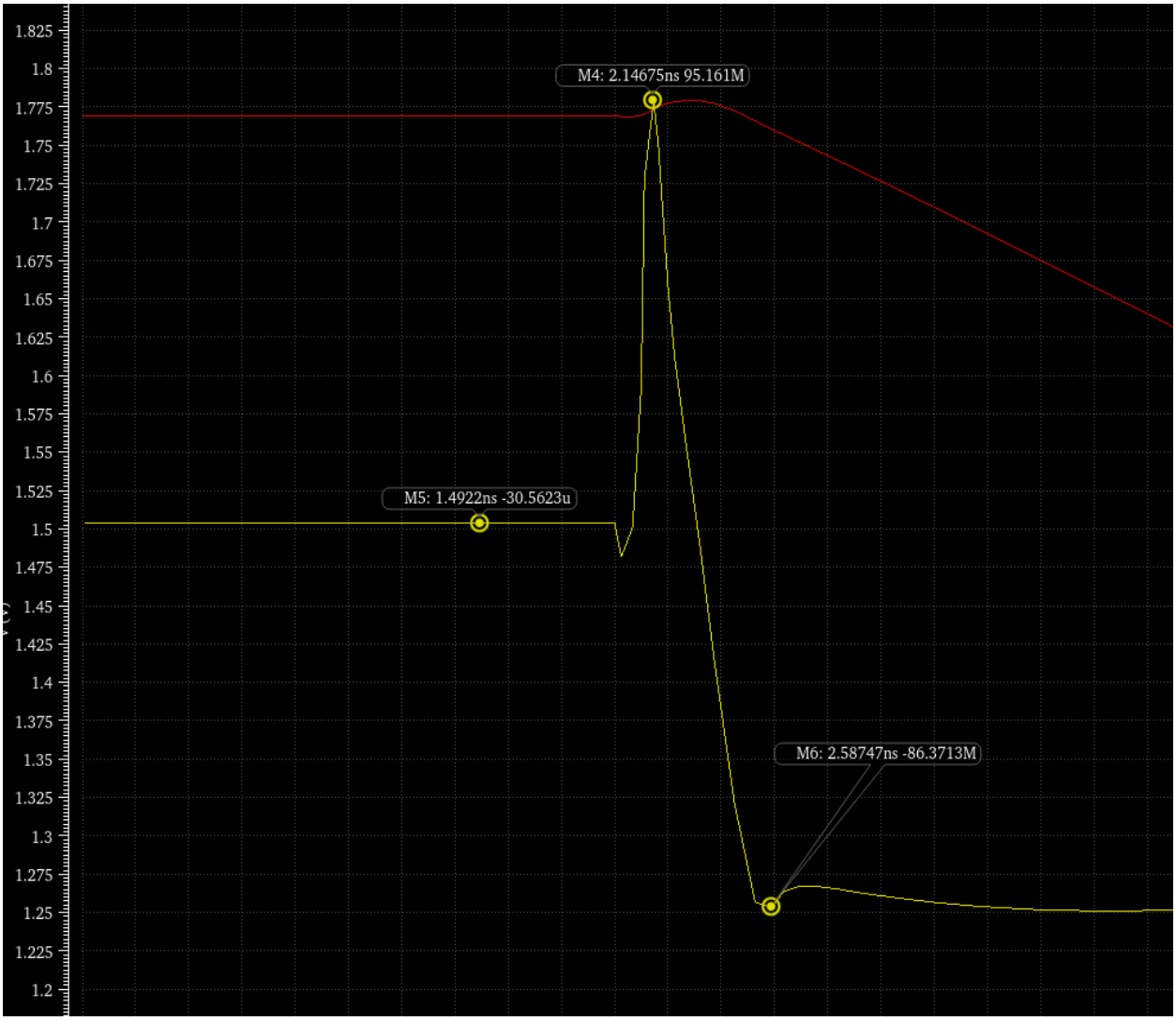
Operating Analysis of Circuit:

AC Gain:



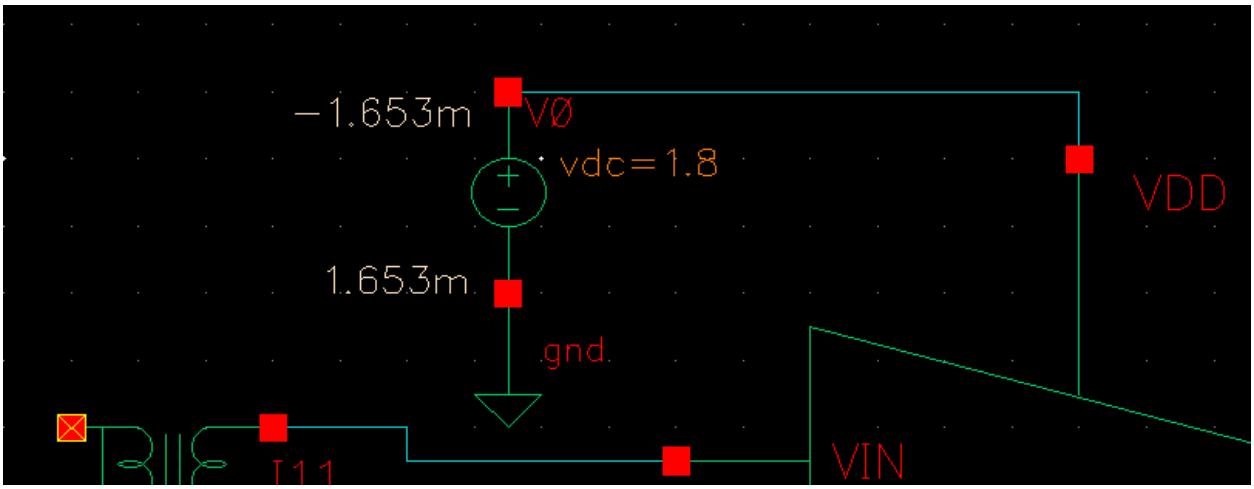

Gain: 55.9677dB Dominant Pole: 239.88kHz GBW Product: 128.9MHz

Slew Rate:



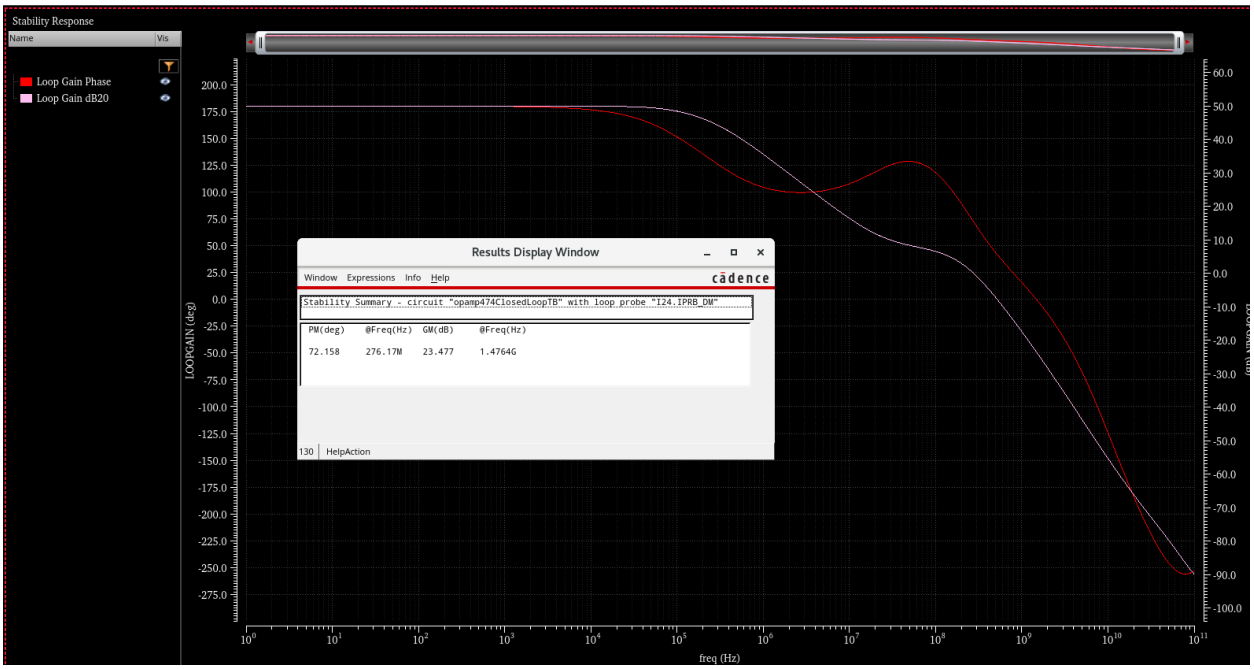

Slew Rate = 86.37M

Power Draw:



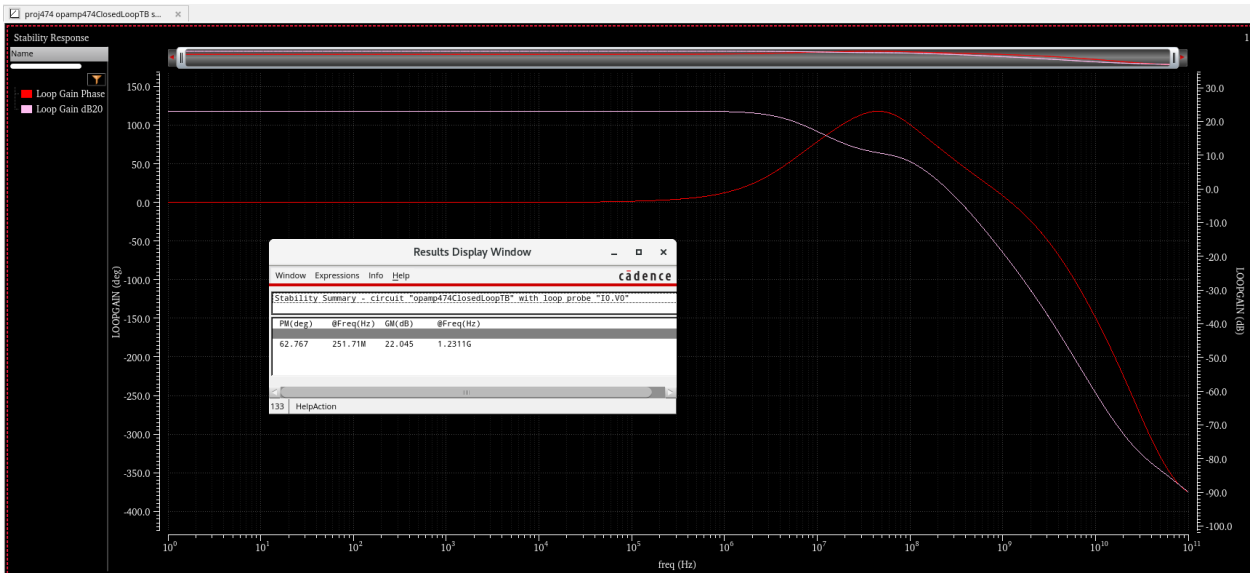

Power Draw = (1.653mA-50uA)*1.8v = 2.8854mW

Differential Phase Margin:



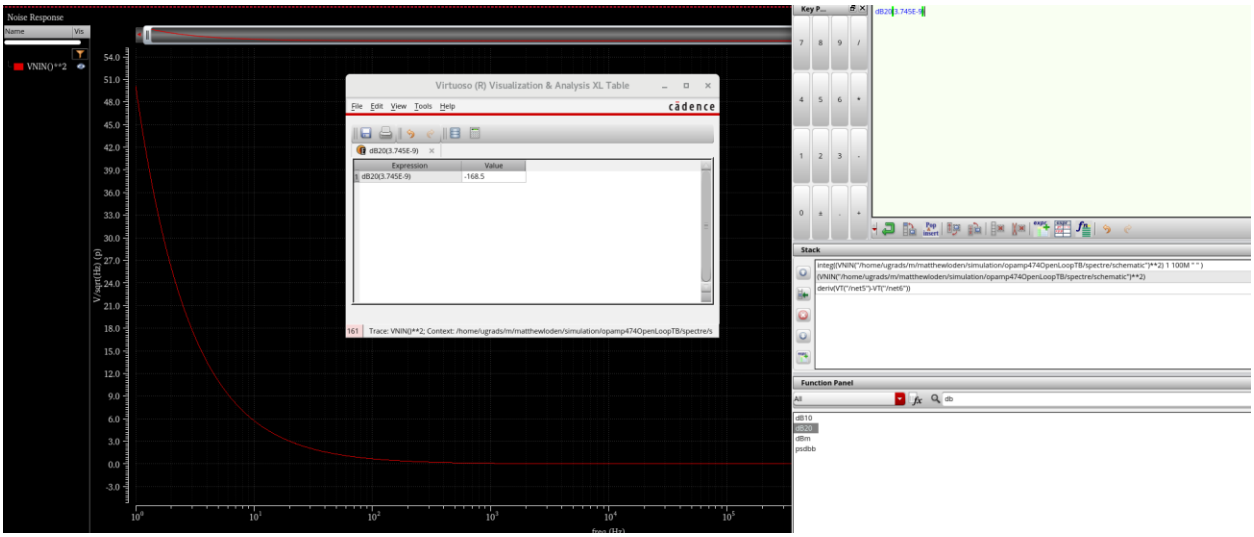

Differential Phase Margin = 72˚

Common Mode Feedback Phase Margin:



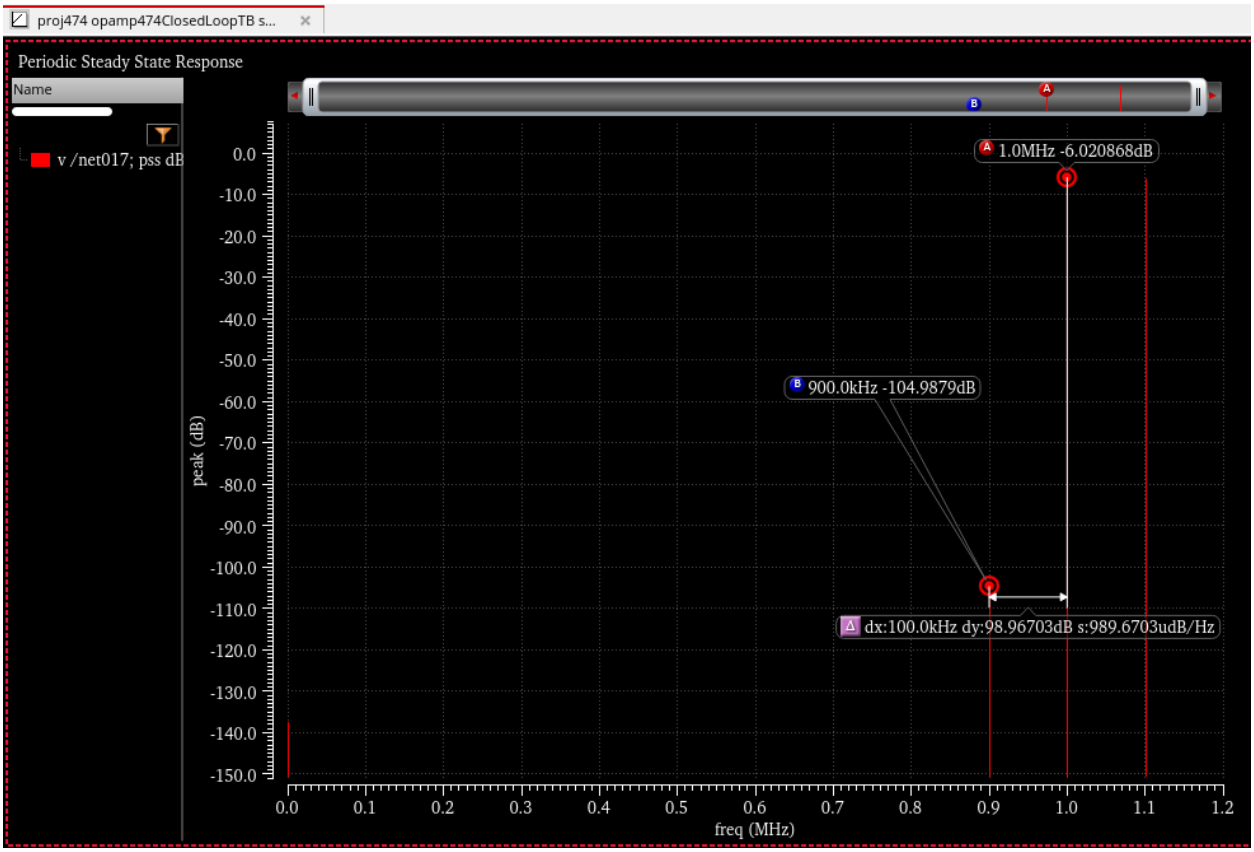

Common Mode Feedback Phase Margin = 62.767˚

Noise:




Noise = -168.5dB

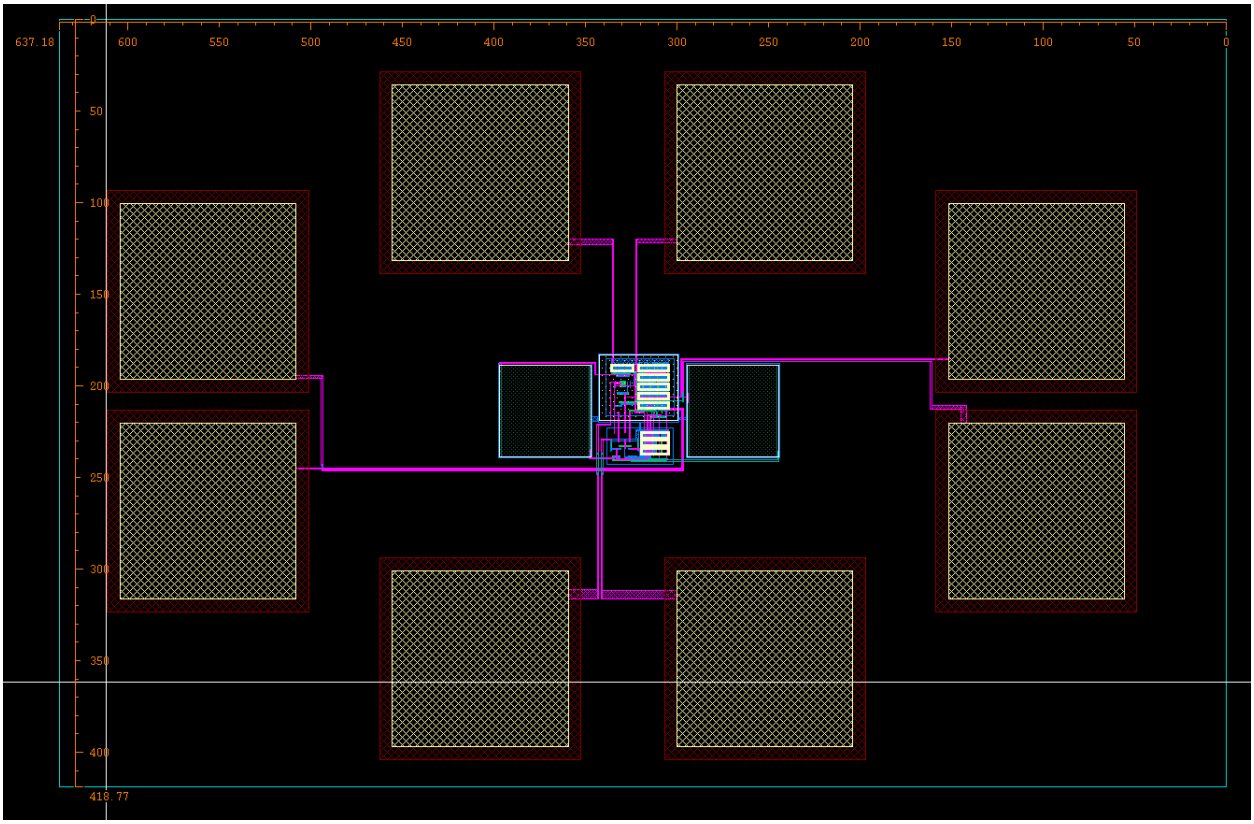
IM3:


proj474 opamp474ClosedLoopTB s...
Periodic Steady State Response
Name
v /net017; pss dB
1.0MHz -6.020868dB
900.0kHz -104.9879dB
dx:100.0kHz dy:98.96703dB s:989.6703udB/Hz
peak (dB)
freq (MHz)
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2

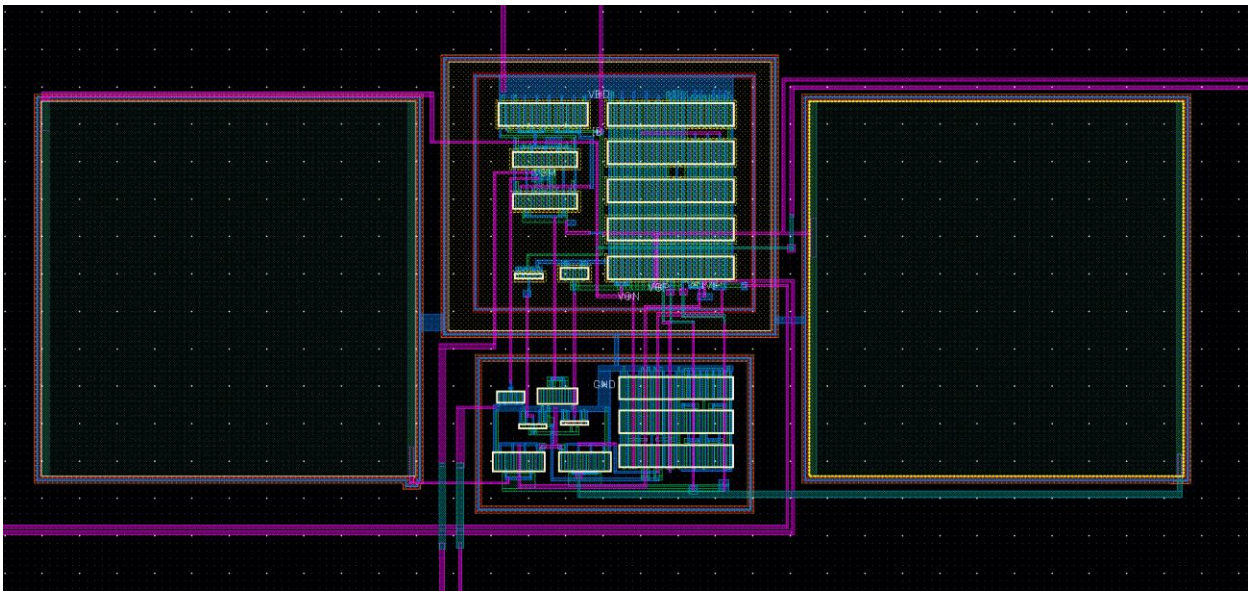
IM3 = 98.967dB

Design Layout

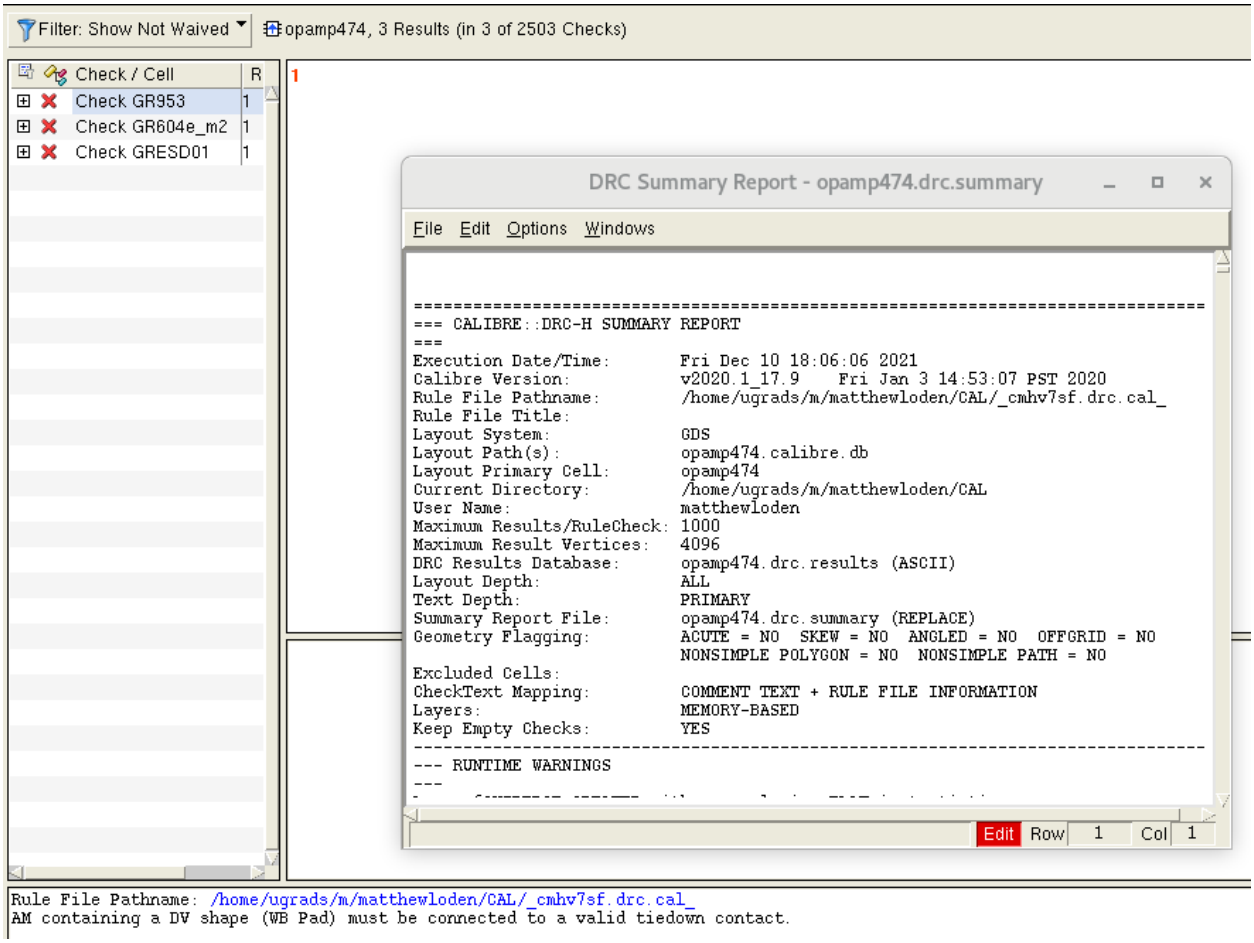
Layout:



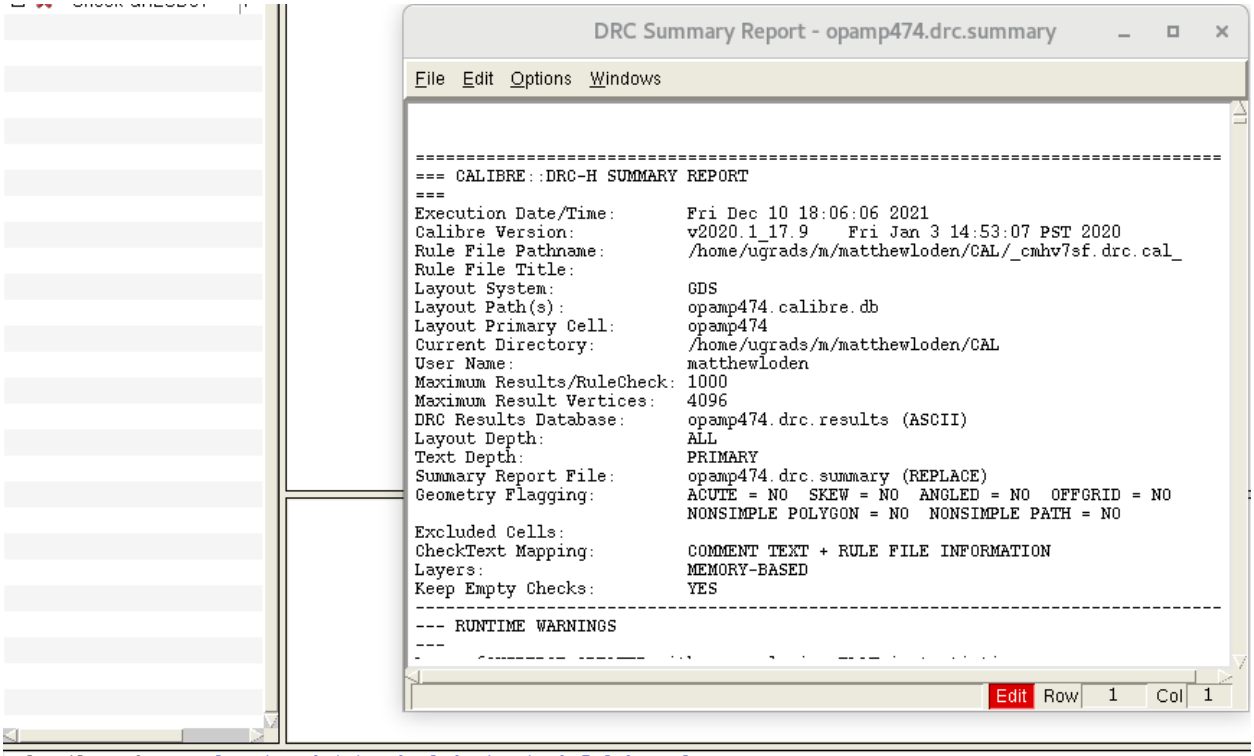

Focused:



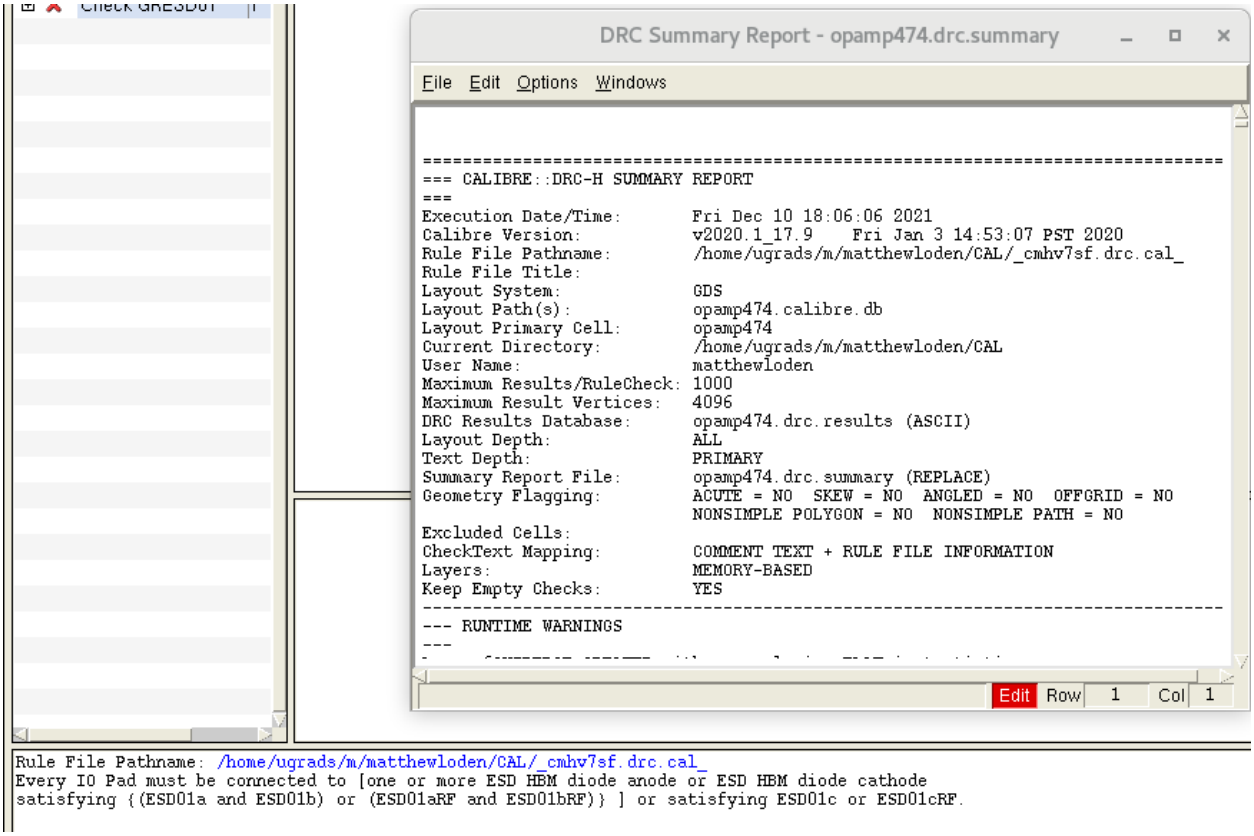
DRC:


Filter: Show Not Waived
opamp474, 3 Results (in 3 of 2503 Checks)
Check / Cell
R
Check GR953
1
Check GR604e_m2
1
Check GRESD01
1
DRC Summary Report - opamp474.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Dec 10 18:06:06 2021
Calibre Version: v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
Rule File Title:
Layout System: GDS
Layout Path(s): opamp474.calibre.db
Layout Primary Cell: opamp474
Current Directory: /home/ugrads/m/matthewloden/CAL
User Name: matthewloden
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: opamp474.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: opamp474.drc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
Edit Row 1 Col 1
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
AM containing a DV shape (WB Pad) must be connected to a valid tiedown contact.

Error 2:

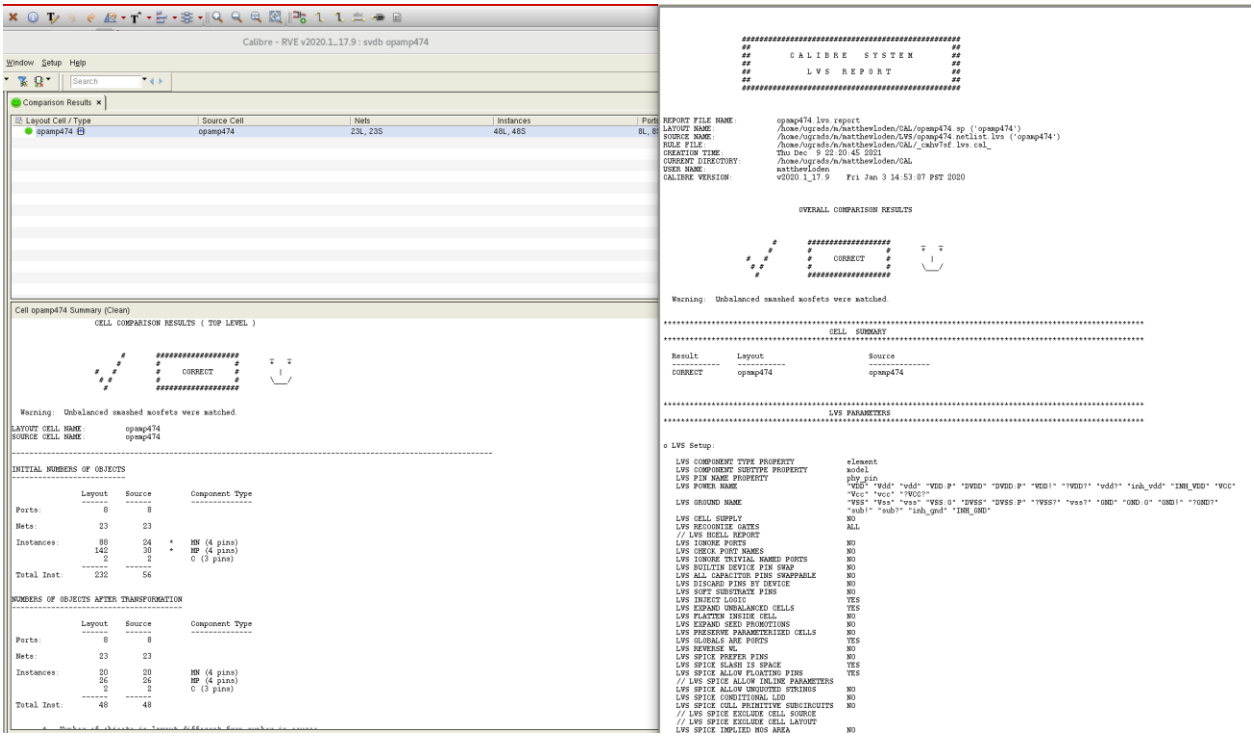

DRC Summary Report - opamp474.drc.summary
File Edit Options Windows
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Fri Dec 10 18:06:06 2021
Calibre Version: v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
Rule File Title:
Layout System: GDS
Layout Path(s): opamp474.calibre.db
Layout Primary Cell: opamp474
Current Directory: /home/ugrads/m/matthewloden/CAL
User Name: matthewloden
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: opamp474.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: opamp474.drc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
Edit Row 1 Col 1
Rule File Pathname: /home/ugrads/m/matthewloden/CAL/_cmhv7sf.drc.cal_
M2 space >= 0.80 um. ([if one M2 shape is greater than 200um2 and is not electrically connected to RX]
and [the other M2 shape (of any area) is electrically connected to RX])

Error 3:



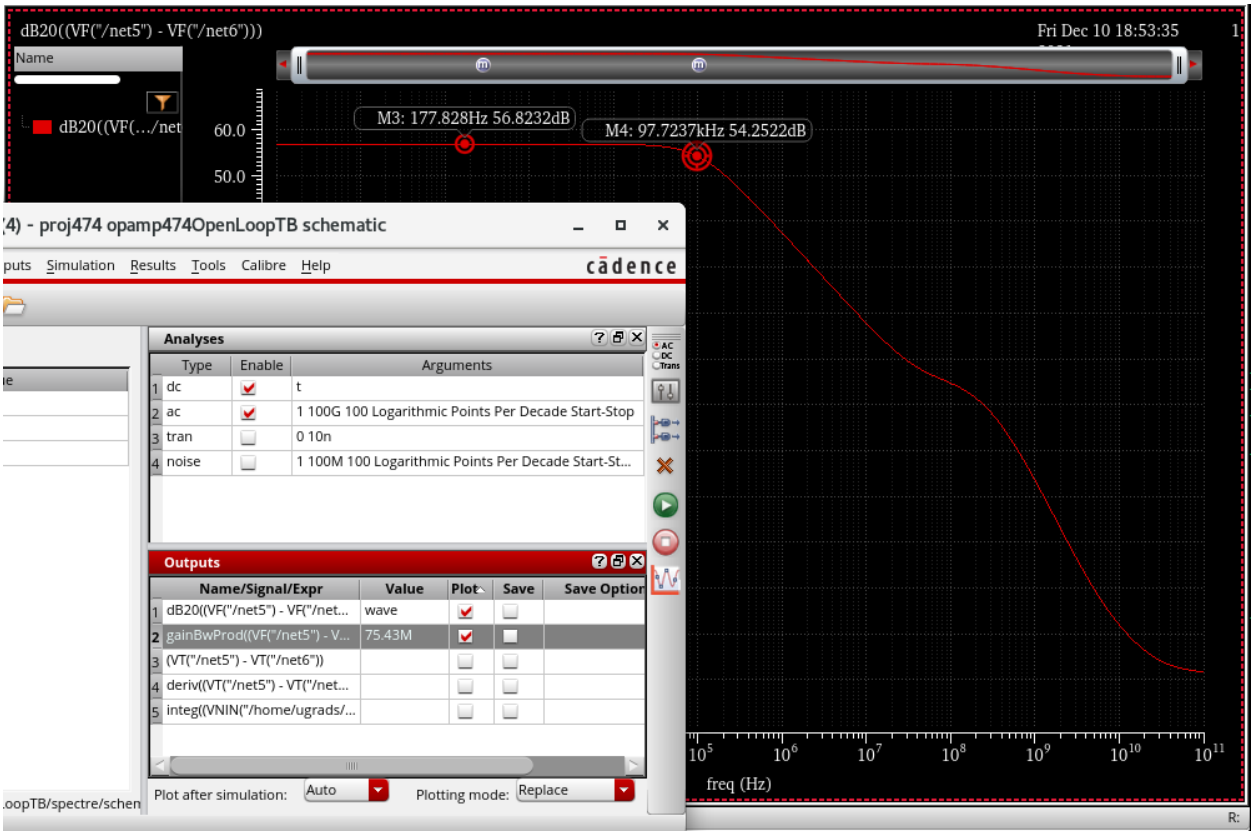

All three errors are expected and ignored for the purposes of this assignment.

LVS:


Calibre - RVE v2020.1_17.9 : svdb opamp474
Window Setup Help
Search
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
opamp474
opamp474
23L, 23S
48L, 48S
Cell opamp474 Summary (Clean)
CELL COMPARISON RESULTS ( TOP LEVEL )
CORRECT
Warning: Unbalanced smashed mosfets were matched.
LAYOUT CELL NAME: opamp474
SOURCE CELL NAME: opamp474
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 8 8
Nets: 23 23
Instances: 88 94 * NN (4 pins)
142 30 * MP (4 pins)
2 2 C (3 pins)
Total Inst: 232 56
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 8 8
Nets: 23 23
Instances: 20 20 NN (4 pins)
26 26 MP (4 pins)
2 2 C (3 pins)
Total Inst: 48 48
CALIBRE SYSTEM
LVS REPORT
REPORT FILE NAME: opamp474.lvs.report
LAYOUT NAME: /home/ugrads/m/matthewloden/CAL/opamp474.sp ('opamp474')
SOURCE NAME: /home/ugrads/m/matthewloden/LVS/opamp474.netlist_lvs ('opamp474')
RULE FILE: /home/ugrads/m/matthewloden/CAL/_calvr7sf.lvs.cal_
CREATION TIME: Thu Dec 9 22:20:45 2021
CURRENT DIRECTORY: /home/ugrads/m/matthewloden/CAL
USER NAME: matthewloden
CALIBRE VERSION: v2020.1_17.9 Fri Jan 3 14:53:07 PST 2020
OVERALL COMPARISON RESULTS
CORRECT
Warning: Unbalanced smashed mosfets were matched.
CELL SUMMARY
Result Layout Source
CORRECT opamp474 opamp474
LVS PARAMETERS
o LVS Setup:
LVS COMPONENT TYPE PROPERTY element
LVS COMPONENT SUBTYPE PROPERTY model
LVS PIN NAME PROPERTY phy_pin
LVS POWER NAME "VDD" "Vdd" "vdd" "VDD:P" "DVDD" "DVDD:P" "VDD!" "?VDD?" "vdd?" "inh_vdd" "INH_VDD" "VCC" "Vcc" "vcc" "?VCC?"
LVS GROUND NAME "VSS" "Vss" "vss" "VSS:G" "DVSS" "DVSS:P" "?VSS?" "vss?" "GND" "GND:G" "GND!" "?GND?" "sub!" "sub?" "inh_gnd" "INH_GND"
LVS CELL SUPPLY NO
LVS RECOGNIZE GATES ALL
// LVS HSELL REPORT
LVS IGNORE PORTS NO
LVS CHECK PORT NAMES NO
LVS IGNORE TRIVIAL NAMED PORTS NO
LVS BUILTIN DEVICE PIN SWAP NO
LVS ALL CAPACITOR PINS SWAPPABLE NO
LVS DISCARD PINS BY DEVICE NO
LVS SOFT SUBSTRATE PINS NO
LVS INJECT LOGIC YES
LVS EXPAND UNBALANCED CELLS YES
LVS FLATTEN INSIDE CELL NO
LVS EXPAND SEED PROMOTIONS NO
LVS PRESERVE PARAMETERIZED CELLS NO
LVS GLOBALS ARE PORTS YES
LVS REVERSE WL NO
LVS SPICE PREFER PINS NO
LVS SPICE SLASH IS SPACE YES
LVS SPICE ALLOW FLOATING PINS YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS NO
LVS SPICE CONDITIONAL LDD NO
LVS SPICE COLL PRIMITIVE SUBCIRCUITS NO
// LVS SPICE EXCLUDE CELL SOURCE
// LVS SPICE EXCLUDE CELL LAYOUT
LVS SPICE IMPLIED MOS AREA NO

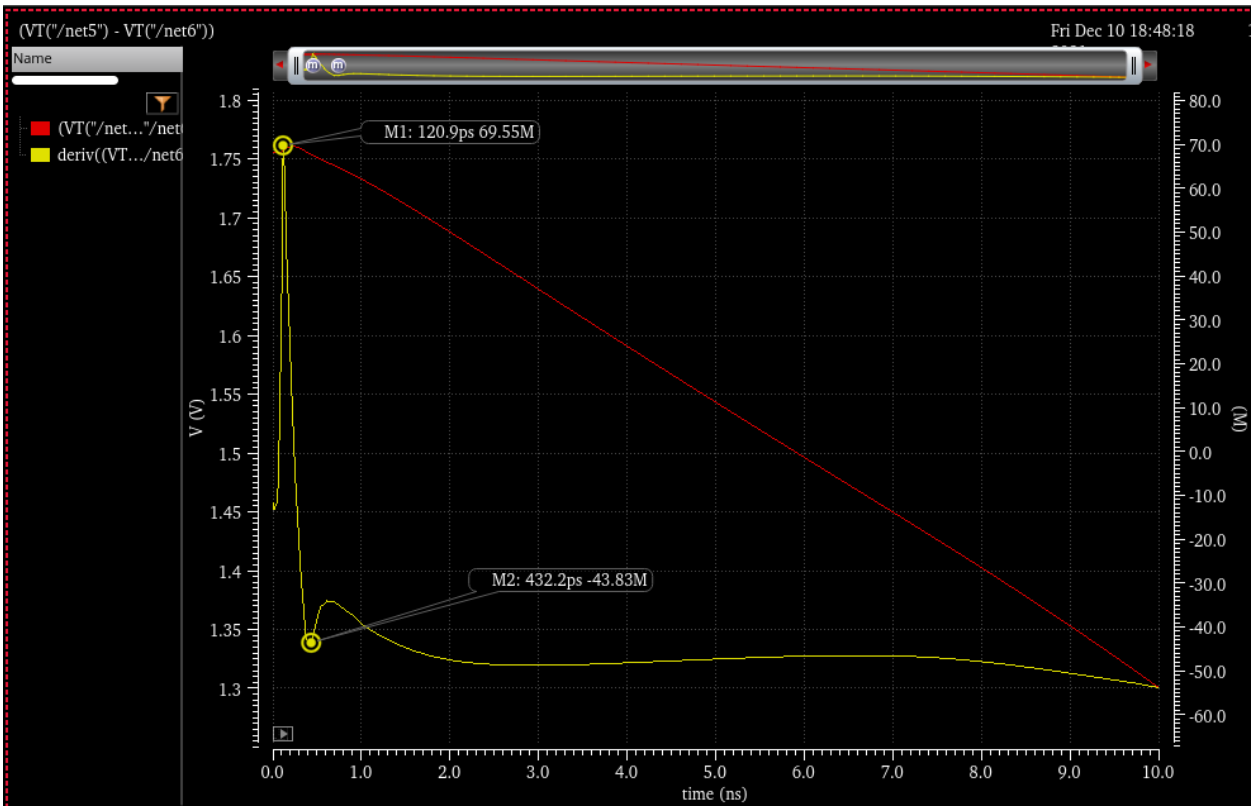
Post Layout Simulation Data

Gain:



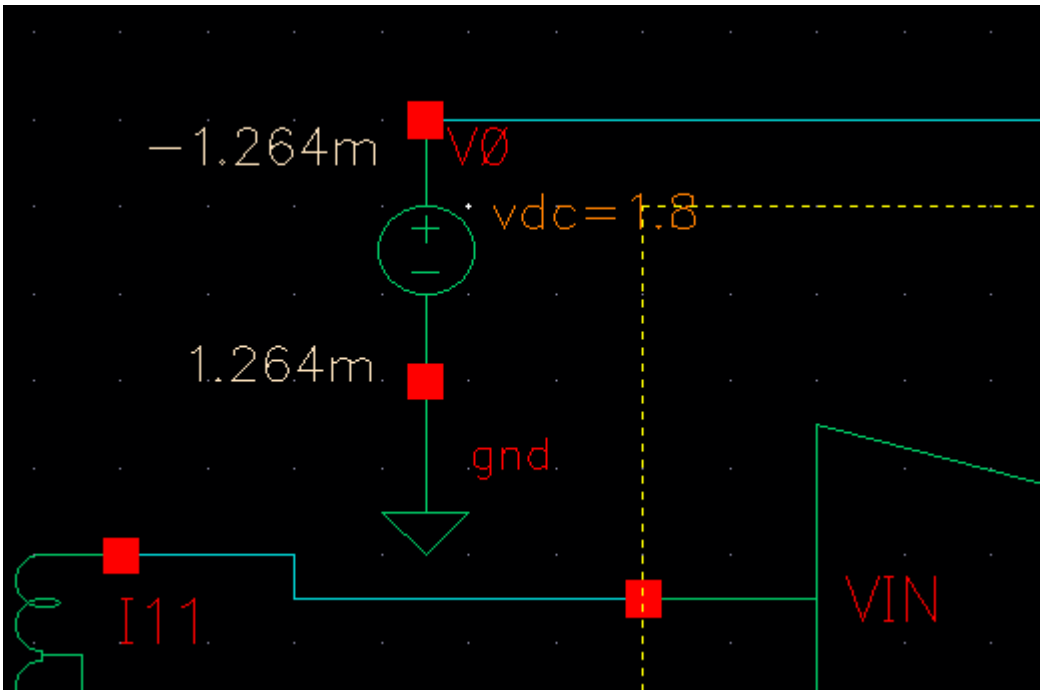

Gain = 56.8232dB  Dominant Pole = 97.734kHz  GBW Product = 75.43MHz

Slew Rate:



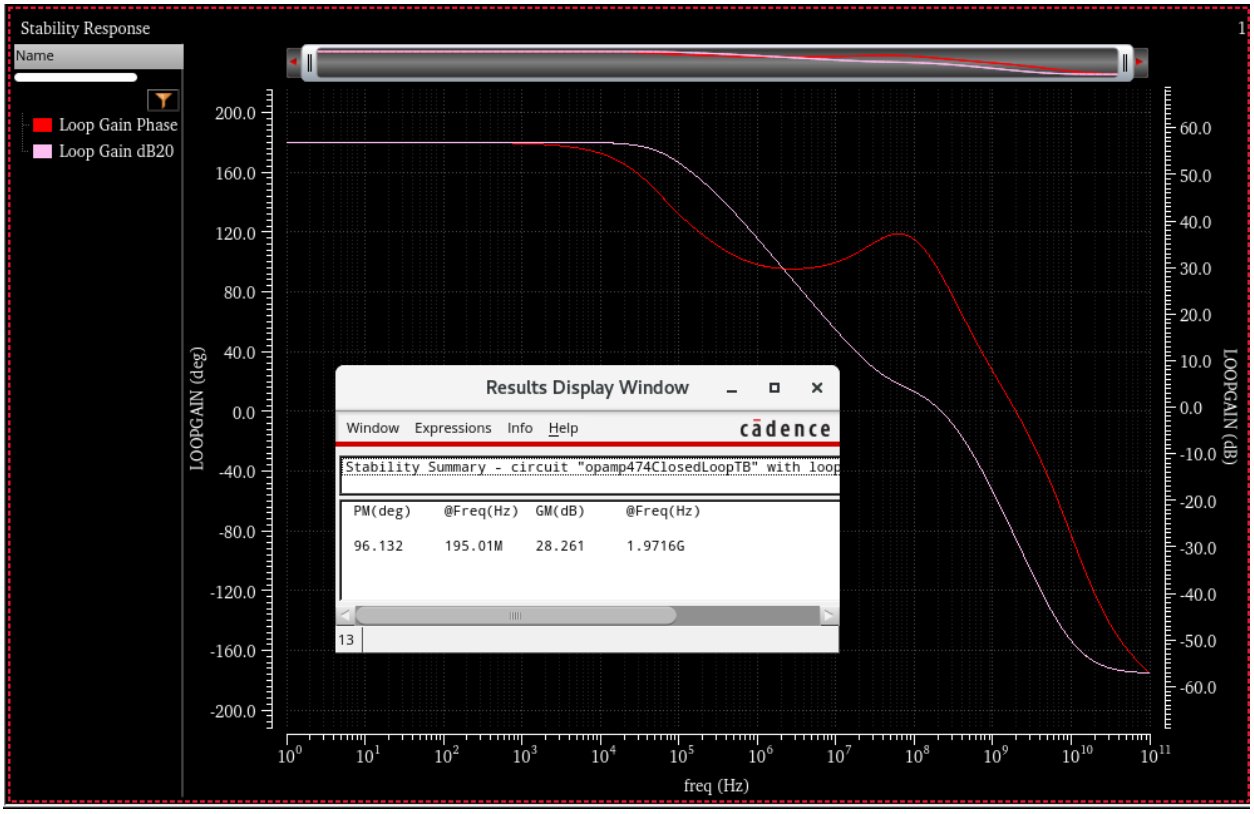

Slew Rate = 43.83M

Power Draw:

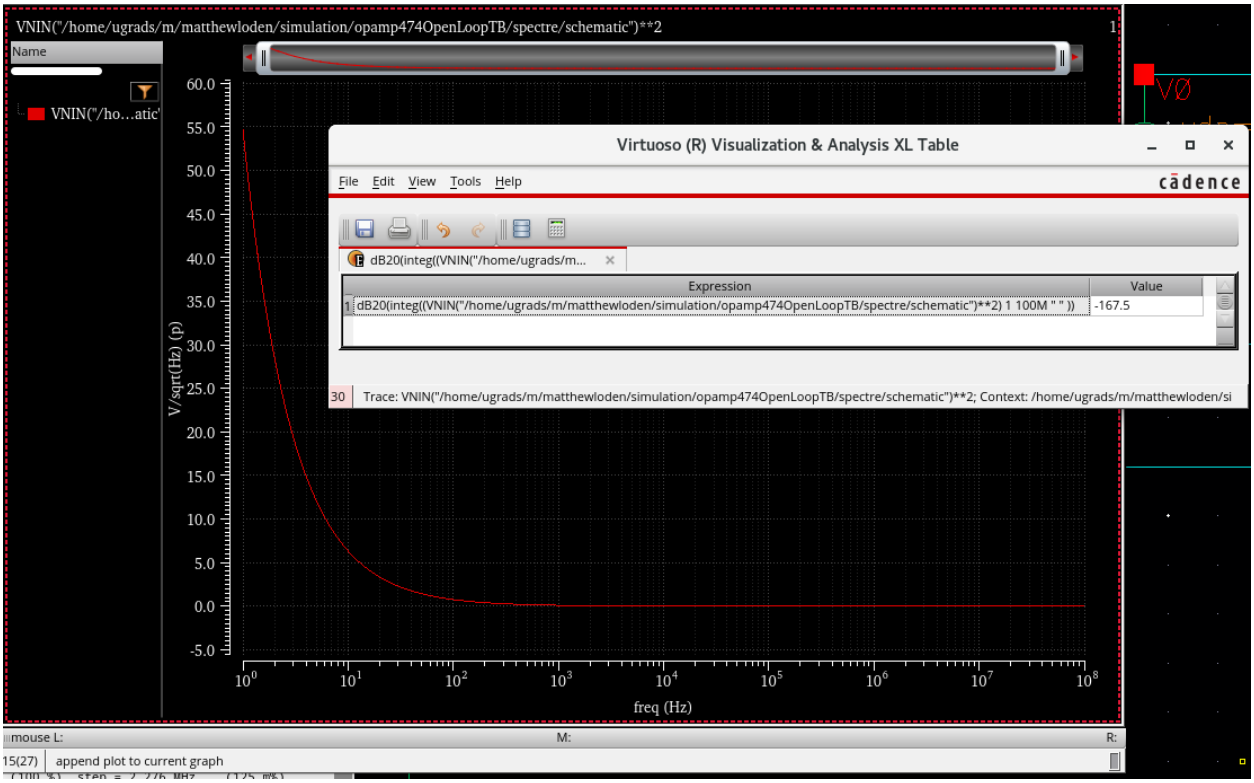


Power = (1.264mA-50uA) * 1.8V = 2.1852mW

Differential Phase Margin:

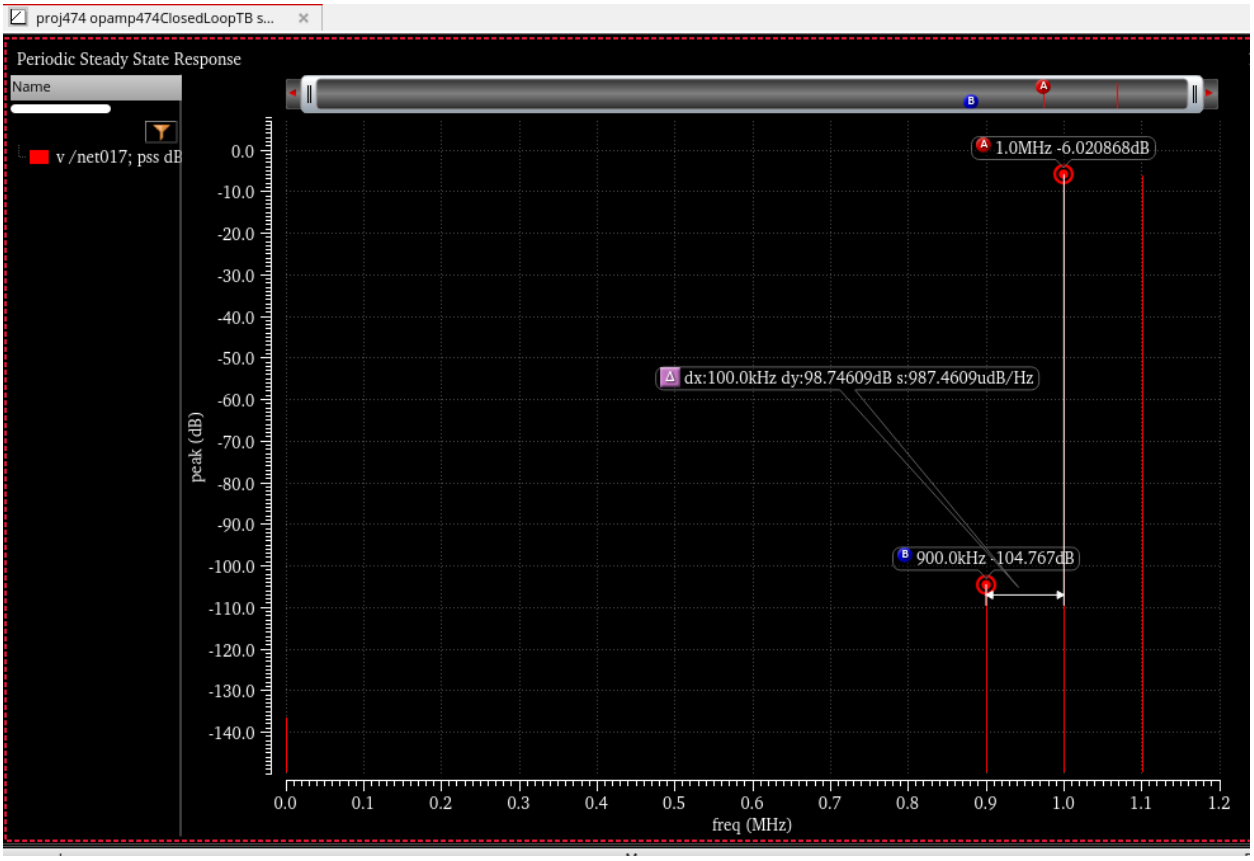



Noise:




Noise = -167.5dB

IM3:


proj474 opamp474ClosedLoopTB s...
Periodic Steady State Response
Name
v /net017; pss dB
1.0MHz -6.020868dB
dx:100.0kHz dy:98.74609dB s:987.4609udB/Hz
900.0kHz -104.767dB
peak (dB)
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
-130.0
-140.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
freq (MHz)

IM3= 98.74dB

Results Discussed

My two requirements to meet were the differential mode phase margin and the common mode feedback being above 60˚. The prelab simulation data resulted in both data being above spec however the common mode margin was much closer to dropping below the margin. When the layout was created and the post layout simulations were conducted, the differential mode phase margin increased. The common mode phase margin was more difficult to calculate as it required breaking the loop somehow in a laid-out setting. It can be assumed that based on the amplifier meeting most other specs and the phase margin increasing for the differential amplifier that the common mode amplifier would similarly have robust phase margin. A basic, however undocumented, test of the common mode phase margin was conducted using a step input on the common mode input port and then a measure of the output waveform was taken. The resultant graph had negligible ripple suggesting an above 45˚ phase margin was well met.

The size constraints of this lab were well within margin as the total area of my device came out to be around 640um by 420um area. The main area of the device was taken up by the pads used as contact points however the main device sizing was much smaller.

The layout technique used was partially a common centroid method. Due to sizing of primarily the current mirror amplifier and the common mode feedback portion, the other half of the device was primarily interdigitated with endcap dummies to ensure upmost safety from parasitics.