EECS 501 Lab 2 Report - Switching Power Supply

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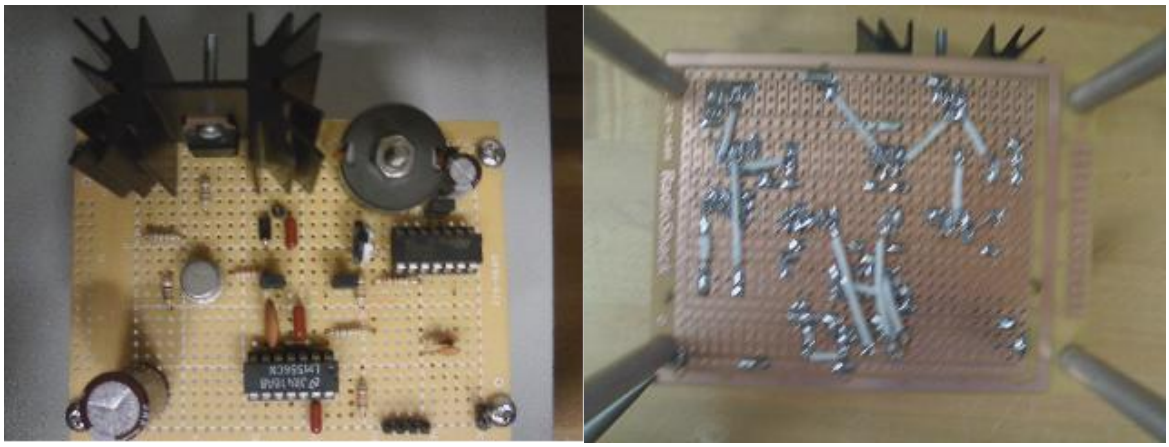

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0. Abstract

The goal of this laboratory was to combine design, fabrication and testing skills to construct a functioning switching power supply. Built to provide an output of 5 V (± 500 mV), the power supply supports various loads over a range of 250 mA to 1 A through the use of a LM723 voltage regulator, a 556 timer, a TIP-42 transistor, and a N3053 transistor. The detail behind the theory, construction and analysis of this linearly regulated power supply is outlined in the following report.

The goal of this project was to design a step-down DC to DC converter, also known as a Buck Converter. This power supply switching at approximately 54 kHz was to output 5 V ± 0.5 V with load currents ranging from 250 mA to 1000 mA. The switching supply was built and found to have 40 mΩ of internal resistance, a load regulation of 0.996%, and maximum ripple of 80 mV.

1. Introduction

The switching regulator designed in this laboratory can be broken up into four distinct stages. The first stage is the error amplifier, which compares the supply's output voltage to the nominal output voltage, and amplifies the difference. The second stage is the Pulse Width Modulator (PWM), which modulates a square-wave according to the control voltage at the input. The third stage is the Control Element, which switches on and off, for a period of time that depends on the duty cycle of the pulse width modulated wave, and thus supply's the output with power. The fourth stage consists of a temporary storage element and an output filter, which provides power to the output and maintains the output voltage, respectively, when the Control Element is switched off.

Power supplies are a crucial part of any electrical system. Many different requirements must be considered when designing a power supply for a specific system to ensure safety for the components it is powering and the users of the device. For instance, if your operating frequency is too high, the BJTs will dissipate too much power, and the efficiency will suffer.

For Project 2, a switching power supply was constructed to take a DC input from the Agilent Power Supply of 13 V and output a DC voltage of 5 V. Unlike the linear power supplies from Project 1, the switching power supply uses a switching regulator as seen in Figure 1.

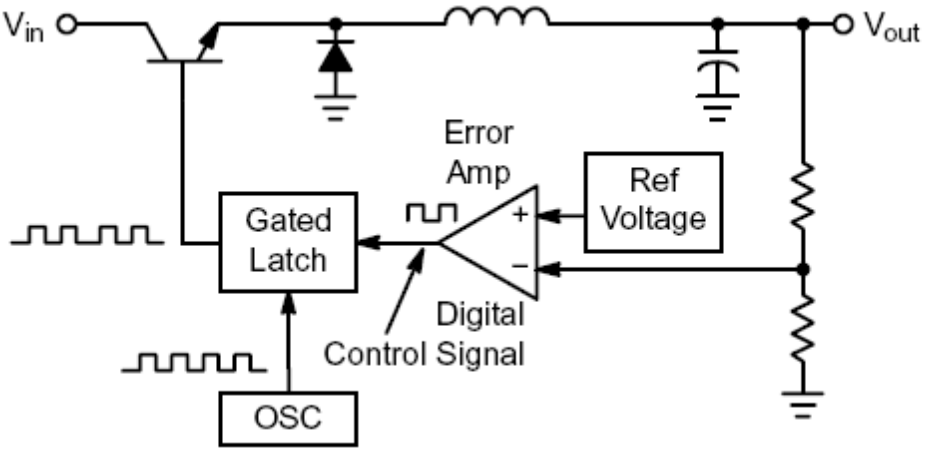

Figure 1: Pictorial Representation of the switching regulator. [2]

This regulator switches the transistor between cutoff and saturation quickly. Cutoff creates a large voltage drop across the transistor and allows no current flow. Saturation allows a large amount of current to pass through but yields a very small voltage drop.

The block diagram for a switching power supply is shown is Figure 2. The control element is powered by a DC input, and is controlled by the pulse width modulator (PWM). The PWM is driven by both the oscillator and the error voltage from the voltage regulator. The error voltage is generated by feeding back the output to the inverting terminal of the voltage regulator. The regulator then compares the output voltage to the reference voltage and outputs the error voltage. When the switch is on the control element

charges the inductor, and when the switch is off the energy stored in the inductor forces a diode in between the switch and inductor to be forward biased to discharge the energy stored in the inductor.

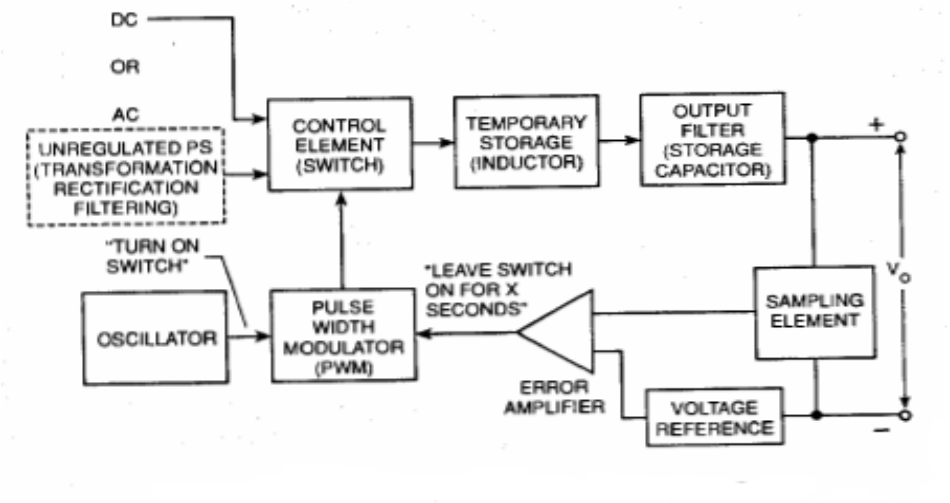

Figure 2: Block Diagram representation of a switching power supply. [2]

2. Methodology

The construction of the switching power supply began with designing the circuit in PSpice, seen in Figure 3. This was done to test the calculated resistance, capacitance, and inductance values and make sure the circuit operated properly. Initially, each element of the design (voltage regulator, square wave generator, PWM, and the switch) was assembled separately on PSpice. Once they were performing the correctly, each part was combined into the master schematic shown in Figure 3.

The LM723 chip was used as a voltage regulator to drive both the PWM and the switch. The reference voltage on the LM723 is 7.1 V, so a voltage divider was used to drop this to 5 V and fed it into the non-inverting terminal. A potentiometer, resistor R5 as seen in Figure 3, was used to fine-tune the voltage divider to ensure that the non-inverting terminal was precisely 5 V. The output voltage is fed into the inverting terminal through the use of feedback. The LM723 compares the non-inverting terminal to the inverting terminal and outputs the difference as an error voltage, which is fed into the PWM as a control voltage. Resistor R14 was sized first by using a potentiometer. A sinusoidal signal was applied to the non-inverting terminal and the output was viewed on the oscilloscope. The potentiometer was adjusted until the output was 180° out of phase from the input. Then the pot resistor was removed, measured, and replace with a 43 kΩ axial resistor.

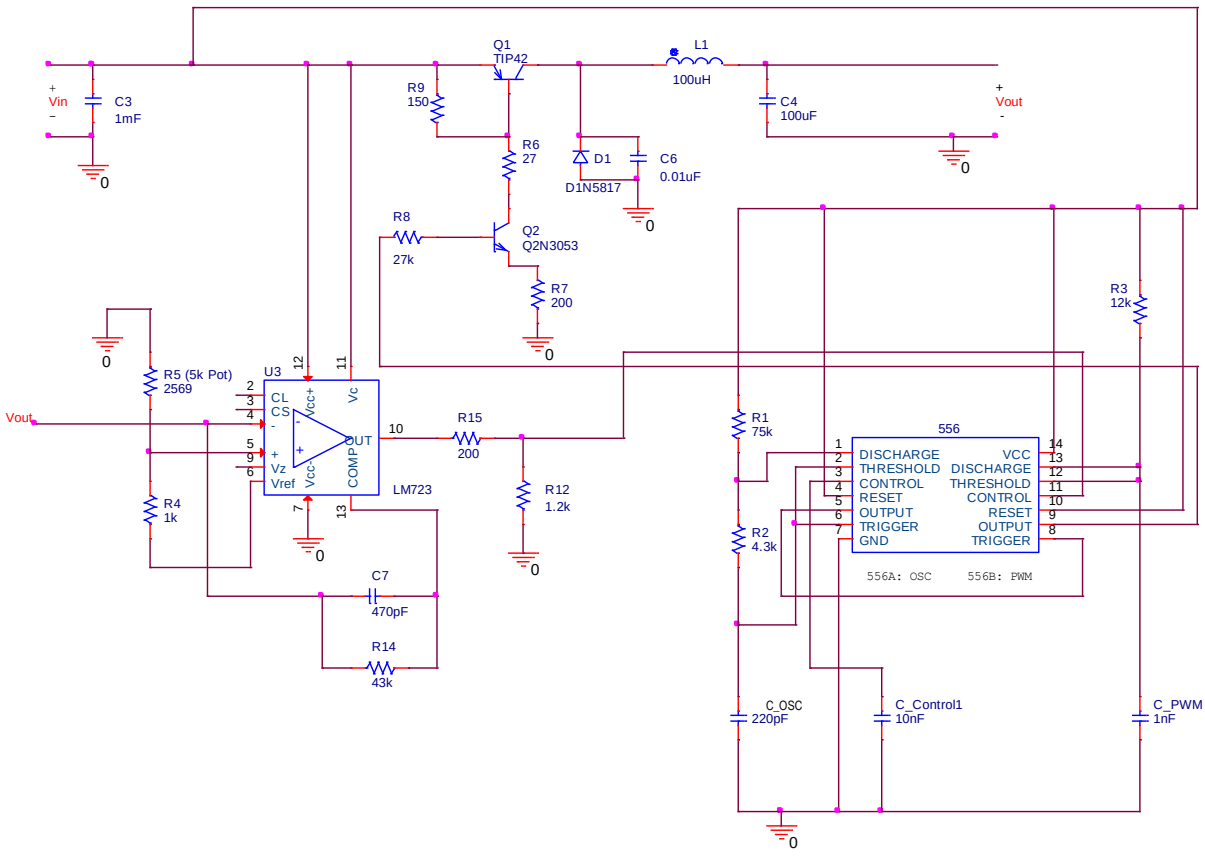

Figure 3: PSpice circuit for switching power supply designed to output 5 V for a range of load current varying from 0.25-1 A.

The square wave generator was made with a 555 timer configured in astable mode. The configuration is called astable because it is never stable at any time. The output waveform is constantly changing between low and high where low and high represent what is connected to ground and V_{cc}. The astable configuration requires two resistors, and a capacitor. The astable configuration is shown in Figure 4.

The 555 in astable configuration operates when output goes high, the capacitor is charged by current through R1 and R2. The trigger and threshold pins sense the capacitor voltage, and when it reaches $\frac{2}{3}V_{cc}$, the output changes to low. The capacitor then discharges through R2 into the discharge pin. When the capacitor voltage drops to $\frac{1}{3}V_{cc}$ the output becomes high which disconnects the discharge pin to ground allowing the capacitor to charge again, and the entire process repeats.

The time that the capacitor takes to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ corresponds to the time that the output is high, and can be calculated by Equation 1.

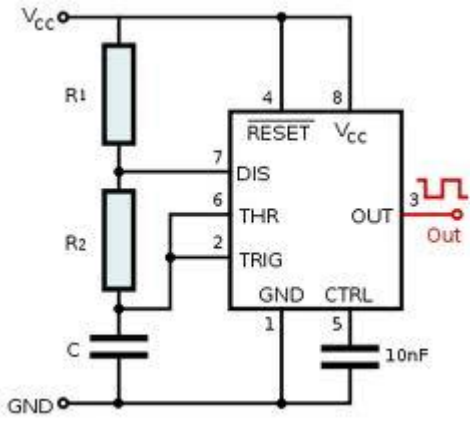

Figure 4 Astable Configuration [8]

$$T_{high} = \ln(2) * (R1 + R2) * C \quad [1]$$

The square wave generator should have a duty cycle greater than 90% because the pulse width modulator (PWM) begins to modulate on the rising edge of the square wave. If the duty cycle of the square wave was low then the PWM could only modulate up until the next rising edge of the square wave. Therefore by making the duty cycle greater than 90%, the PWM has a greater range of potential high output which to modulate over.

The equation representing the time that the output is low is Equation 2.

$$T_{low} = \ln(2) * R2 * C \quad [2]$$

A targeted frequency of 50 kHz was choosen for the square wave oscillator. A capacitor had to be picked such that it would allow this high frequency, and a high capacitance will increase the cycle time, and decrease the frequency. Therefore a capacitor value of 220 pF was choosen because of the low time period that the capacitor takes to charge/discharge. The values of R1 and R2 can now be calculated from two equations with two unknowns.

$$Period = T = \frac{1}{50000} = 20\ \mu s \quad [3]$$

$$T_{high} = 90\% * T = \ln(2) * (R1 + R2) * (220 * 10^{-12})$$

$$T_{low} = 10\% * T = \ln(2) * R2 * (220 * 10^{-12})$$

The values for R1 and R2 that were calculated yielded a square wave with a frequency below 50 kHz. The frequency was lower because of the addition of a smoothing capacitor between V_{cc} and ground. This problem was solved by placing a 100 kΩ potentiometer in place of R1, and tuning it such that the output was closer to 50 kHz. This resistance was then measured, and replaced with the closest axial resistor value. The final values determined for R1 and R2 were 75 kΩ and 4.3 kΩ respectively. This yielded a square wave with a frequency of 54 kHz, and a duty cycle of 93%.

The PWM is constructed by configuring the 555 timer to be in monostable mode rather than astable mode. A key difference between the square wave generator and the PWM is that the control voltage varies which modulates the duty cycle of the output of the PWM. The monostable configuration is shown in figure X.

The operation of the monostable setup is the timing period beings when the trigger input is less than $\frac{1}{3}V_{cc}$ which causes the output to be high. The capacitor then begins to charge through the single resistor, while the threshold input senses the capacitor voltage. When the threshold reaches $\frac{2}{3}V_{cc}$, the output becomes low which causes the discharge pin to have a path to ground. The capacitor discharges through this path, and the entire cycle repeats when the next rising edge at the trigger is detected.

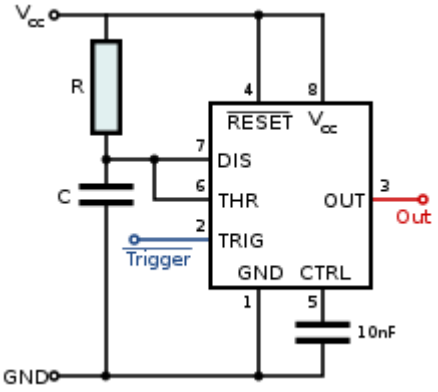

Figure 5 Monostable configuration [8]

The ideal duty cycle of the PWM would be 38% under ideal conditions because the ratio of the load and source voltage is $\frac{5}{13} * 100 = 38\%$.. What this means is the load voltage would have 13V 38% of the time, and 0V

62% of the time. Therefore the average voltage applied to the load over a single period would be the desired 5V output. The time the PWM is high is represented by Equation 4.

$$T_{high} = 38\% * T = \ln(3) * R * C \quad [4]$$

Choosing a capacitor value of 1nF yields a resistance value of 6.9 kΩ. However during experimentation, it was found that representing the resistor with a 25kΩ potentiometer offered a greater degree of control of the output voltage. The optimal value for the resistor was determined through experimentation to be 12 kΩ.

Including resistors the Control Element employs two BJTs, which must be properly biased if the upper TIP-42 BJT (Q1) is to switch effectively. The biasing modes that Q1 operates in are Cutoff and Saturation. The upper BJT will only be in Cutoff if both p-n junctions are reverse biased and the Base current (i_{B1}) is zero. Since this transistor is of P-type, the Base voltage must be greater than the Emitter and Collector voltages. Saturation can be achieved only if both p-n junctions are forward biased and the Base current is greater than zero. The lower BJT (Q2) operates in the Cutoff and Active modes. Cutoff will be achieved every time the pulse width modulated wave is low, since the Base terminal will be at zero potential. Resistor R1 ensures that Q2 enters Cutoff even if the PWM wave's low voltage is slightly greater than 0 V, by maintaining the Emitter at a greater potential than the Base. The Active mode requires that the Collector-Base Junction (CBJ) be reverse biased, the Emitter-Base Junction (EBJ) be forward biased and the Base current greater than zero. When Q1 is in the Active mode, the Collector current is greater than the Base current by a factor of β, a device parameter that has minimum and maximum values of 50 and 250, respectively. Thus, the Base current of Q2 is used to bias the Base current of Q1, since the upper transistor's Base current is equal to the Collector current of Q2 minus the current through R_4. The current through R_4 is minimal, making the Q2 Collector current approximately equal to the Base current of Q1.

An inductor and a capacitor were used to implement the temporary storage element and the output filter, respectively. The charging inductor was wound by hand and placed inside a Ferroxcube core (grade 3C81) which substantially increased the inductance. The minimum value of the inductance was determined using Equation 5.

$$L_{min} = \frac{V_{IN} - V_{sat} - V_{OUT}}{I_{pk(switch)}} t_{on} \quad [5]$$

Since the minimum inductance was calculated to be about 29 μH, it was decided that 35 μH would be used. The number of turns needed to provide 35 μH was calculated using Equation 6

$$N = \sqrt{\frac{L \times 10^9}{A_L}} \quad [6]$$

where: N = number of turns

L = desired inductance in H

A_L = μH /1000 (~400 for the 3C81 core)

which turned out to be about 9.4 turns. An inductor meter was used to verify the inductance which proved the validity of the formula. This inductor would later be increased to 100 µH, to provide smoother switching. The capacitance of the output filter was chosen to be 100 µF, a value based on Equation 7.

$$C_o > \frac{I_{pk(switch)}(t_{on} + t_{off})}{8 \cdot V_{ripple(p-p)}} \quad [7]$$

3. Results

Data was collected using the Agilent 54622A oscilloscope and the Fluke 73III multimeter. Loads were attached to the output to draw currents ranging from 250 mA to 1 A. For a DC input of 13 V, the output voltage ranges from 5.09 V – 4.98 V for the specified load current values. The complete results from the measurements can be seen in Table 1 and Figure 6.

Table 1: Output Voltages vs. Load Currents for 13 V DC input.

Output Voltage [V]	Load Current [mA]
5.09	250
5.06	300
5.06	350
5.05	400
5.05	450
5.04	500
5.03	550
5.03	600
5.02	650
5.01	700
5.00	750
4.99	800
4.99	850
4.98	900
4.98	950
4.98	1000

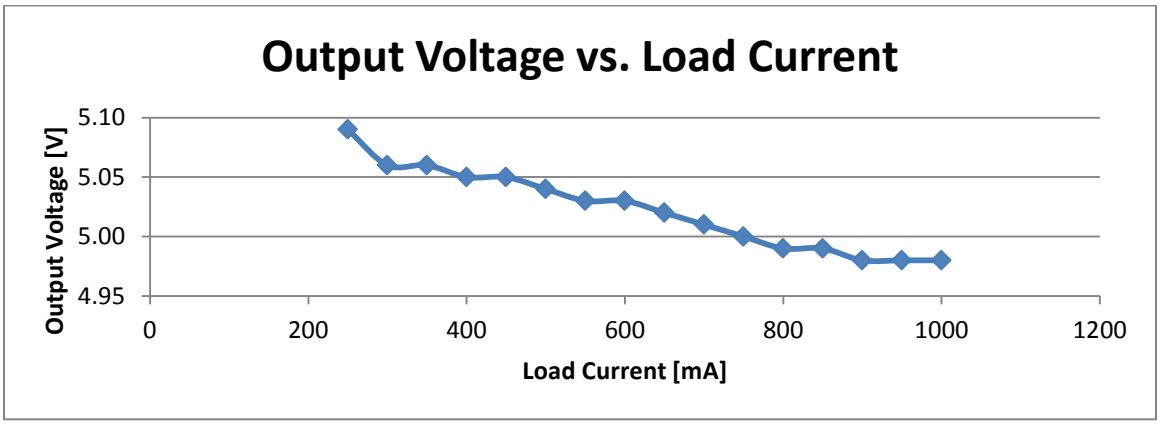

Figure 6: Plot of Output Voltage vs. Load Currents for a DC input of 13 V.

Figure 6 shows that the output voltage has a range of 100 mV, which is well within the design specifications. Equations 8, 9, and 10 were used to calculate the efficiency of the circuit. A plot of efficiency vs. load current can be seen in Figure 7. The efficiency ranges from 69-77%. As the load current increases, the efficiency converges to a value of roughly 76%.

$$\eta = P_{OUT}/P_{IN} \quad [8]$$

$$P_{OUT} = V_{OUT} * I_{LOAD} \quad [9]$$

$$P_{IN} = V_{IN} * I_{IN} \quad [10]$$

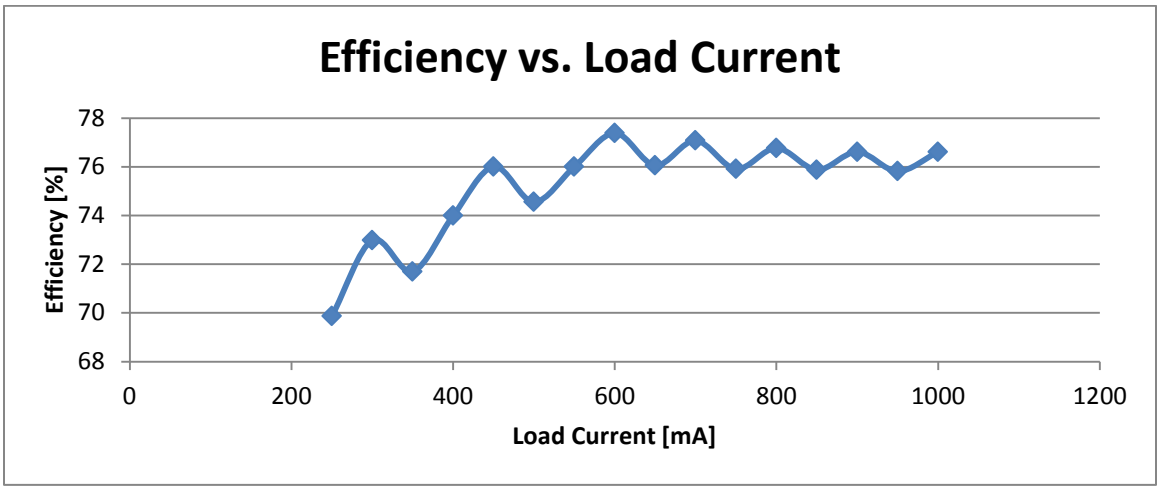

Figure 7: Plot of Efficiency vs. Load Current showing a range from 69 – 77%.

Figure 8 shows the plot of BJT case temperature vs. time. This measurement was taken to see how the BJT would perform over an extended period of time. Since the efficiency was above 75%, the BJT did not over-heat as time progressed.

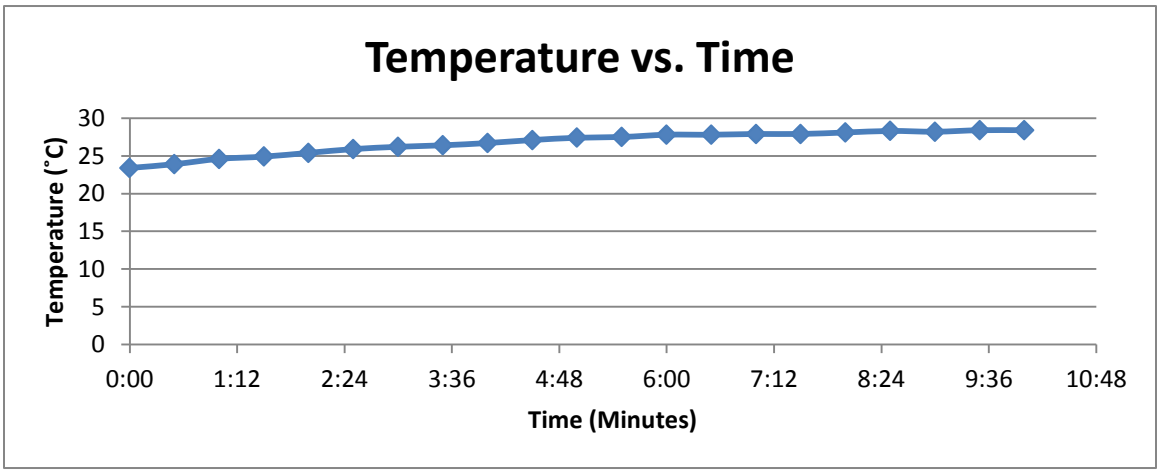

Figure 8: Plot of BJT Case Temperature vs. Time, shows the temperature of the BJT over a ten-minute range.

The maximum sink to ambient thermal resistance, $\theta_{sa,}$ which is capable of dissipating the worst case power loss from the TIP-42 can be approximated by assuming that all the power that is not dissipated at the load is dissipated by the TIP-42. The total power loss at minimum load is 1520 mW. Furthermore the temperature of the junction, T_j, is assumed to be the maximum die temperature of 150 °C. The ambient temperature is 25 °C, the case to sink thermal resistance is assumed to be negligible, and the junction to case thermal resistance, θ_{jc}, is 1.67 $\frac{^{\circ}\mathrm{C}}{\mathrm{W}}$. Using these assumptions, both $\theta_{ja(max)}$ and θ_{sa} can be calculated.

$$\theta_{ja(\max)} = \frac{T_j - T_a}{P_D} = \frac{150-25}{1.520} = 82.24\ \frac{^{\circ}C}{W} \quad [11]$$

$$\theta_{sa} = \theta_{ja(max)} - \theta_{jc} - \theta_{cs} = 82.24 - 1.67 - 0 = 80.57\ \frac{^{\circ}C}{W} \quad [12]$$

These calculations show that the desired heatsink must have a thermal resistance value of less than 80.57 $\frac{^{\circ}C}{W}$. The TO-220 heatsink has a thermal resistance of 5 $\frac{^{\circ}C}{W}$ which is well below the maximum calculated value. According to the TIP-42 datasheet, the θ_{ja} without a heatsink is 57 $\frac{^{\circ}\mathrm{C}}{\mathrm{W}}$. Therefore a heatsink may not be required which would save on manufacturing costs as well as optimize the space required for the circuit. [6][8]

The case and junction thermal temperatures of the TIP-42 can be approximated by assuming that all the power loss is being dissipated through the TIP-42, the Schottky diode, and the Ferroxcube inductor. The equivalent series resistance (ESR) of the output capacitor is ignored as well as the losses from the LM723 and 556 circuits. The power loss due the inductor core is approximated from the datasheet to be 0.46 W. The power loss due to the Schottky diode is more in-depth, and requires approximating the average forward current, $I_{F(av)}$. $I_{F(av)}$ is calculated by taking the difference between the output current and the current supplied by the Agilent power supply. This approximation is made on the basis that while the TIP-42 is conducting there is negligible current passing through the Schottky diode because it is in reverse bias. Therefore the current that did not originate from the Agilent source must have flowed through the Schottky diode when the TIP-42 was in cutoff. Once $I_{F(av)}$ is determined for a specific load, the forward power dissipation figure from the datasheet can be used to approximate the average power dissipation, $P_{F(av)}$, which is the power loss from the Schottky diode. When the power loss due to the inductor and the Schottky diode are found, the power dissipated by the TIP-42 can be calculated. Using the power loss from the TIP-42, the theoretical temperatures of the case and junction can be found, and compared against the maximum operating temperature which is 150 $°C$. The theoretical case and junction temperatures are calculated below under a load of 1 A. Furthermore the temperature at the junction was calculated both with a heatsink, and without a heatsink. [6][8]

$I_{F(av)}$ = 500 mA → $P_{F(av)}$ = 0.29 W (Measured from datasheet graph)

$$P_{TIP42} = P_{Loss\_Tot} - \left(P_{Inductor} + P_{F(av)}\right) = 1.520 - (0.46 + 0.29) = 0.77\ \mathrm{W} \quad [13]$$

$$T_c = T_a + \theta_{sa} * P_{TIP42} = 25 + 5 * 0.77 = 28.85\ °C \quad [14]$$

$$T_{j\_heatsink} = T_{c\_measured} + \theta_{jc\_heatsink} * P_{TIP42} = 28.4 + 1.67 * 0.77 = 29.6859\ °C \quad [15]$$

$$T_{j\_no\_heatsink} = T_{c\_measured} + \theta_{jc\_no\_heatsink} * P_{TIP42} = 28.4 + 57 * 0.77 = 72.29\ °C \quad [16]$$

The theoretical temperature of the case agreed with the measured temperature of the case with a 1.5% error. The junction temperature of the TIP-42 with a heatsink under a load of 1 A is 120.31 $°C$ below the maximum tolerable temperature of the TIP-42. The junction temperature without a heatsink is 77.71 $°C$ below the maximum temperature of 150 $°C$. This suggests that a heatsink is not required for the operation of the switching power supply.

4. Conclusion

Based on the data shown in Table 1 and Figure 4, it is evident that the circuit constructed successfully sustained an output of 5 V ± 0.1 V. Using the data in Table 1 and Equation 17, the internal resistance was found to be 0.1 Ω.

$$R_{internal} = d(V_L)/d(I_L) \quad [17]$$

$$R_{internal} = |V(0.3\ A) - V(0.6\ A)| \,/\, |I_L{=}0.3\ A - I_L{=}0.6\ A|$$

$$R_{internal} = |5.06\ V - 5.03\ V| \,/\, |0.3\ A - 0.6\ A|$$

$$\boxed{R_{internal} = 0.03\ V/\ 0.3\ A = 0.1\ \Omega}$$

Since an ideal power supply would have no internal resistance so that no power would be dissipated and is all delivered to the load. Another characteristic to consider when evaluating any power supply, is load regulation represented by a constant K. This refers to the change in the output voltage as the load varies from its maximum to minimum values. To find this percentage, Equation 18 was used. $V_{RD(max)}$ is the voltage at the maximum allowable load (when the load current is 1 A), and $V_{RL(min)}$ is the voltage at the minimum allowable load (when the load current is 250 mA).

$$K = [(V_{RD(max)} - V_{RL(min)}) / V_{RL(min)}] * 100\% \quad [18]$$

$$K = [(5.06 - 4.98) / 4.98] * 100\%$$

$$K = [0.016] * 100\%$$

$$\boxed{K = 1.6\ \%}$$

This result, along with the plot in Figure 4 show that the output voltage changes very little as the load current is varied, which is a crucial feature of a quality switching power supply.

5. Recommendations

The design configuration used operated well within the specifications for this project. After demonstrating the functionality of the circuit, it was realized that a few improvement could be made. The first being the removal of resistor R6, as seen in Figure 3, which could increase the efficiency of the circuit. Another recommendation would be to use surface mount components because of they provide more precise values. When viewing the output signal on the oscilloscope multiply high frequency

components showed up. In order to filter out some of these unwanted frequencies, a few small capacitances could be added. The last measurement taken was the BJT case temperature, this was measured for ten minutes and the highest temperature reached was roughly 28 °C. Since the temperature did not get very high, the heat sink probably was not necessary and could be removed from the design to save money. Of course, the temperature should be measured for longer than ten minutes to ensure that it will eventually quit rising before removing the heat sink.

6. References

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