Increasing Dynamism in Plasticine

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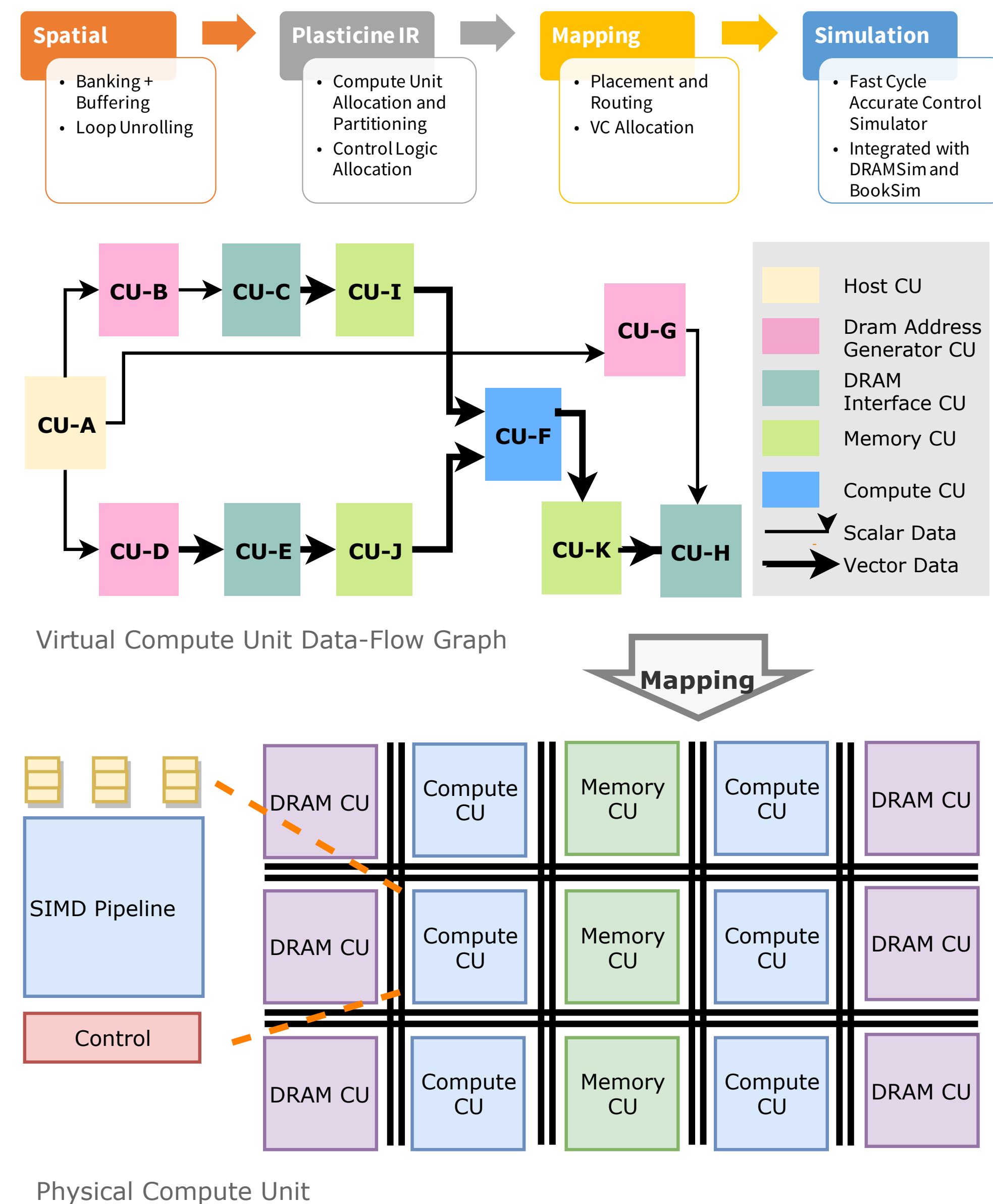mvilim@stanford.edu

Background

Plasticine a vector Coarse-Grained Reconfigurable Array:

- 6-stage, 16-lane 32-bit floating point SIMD pipelines
- Distributed 256-kByte memories
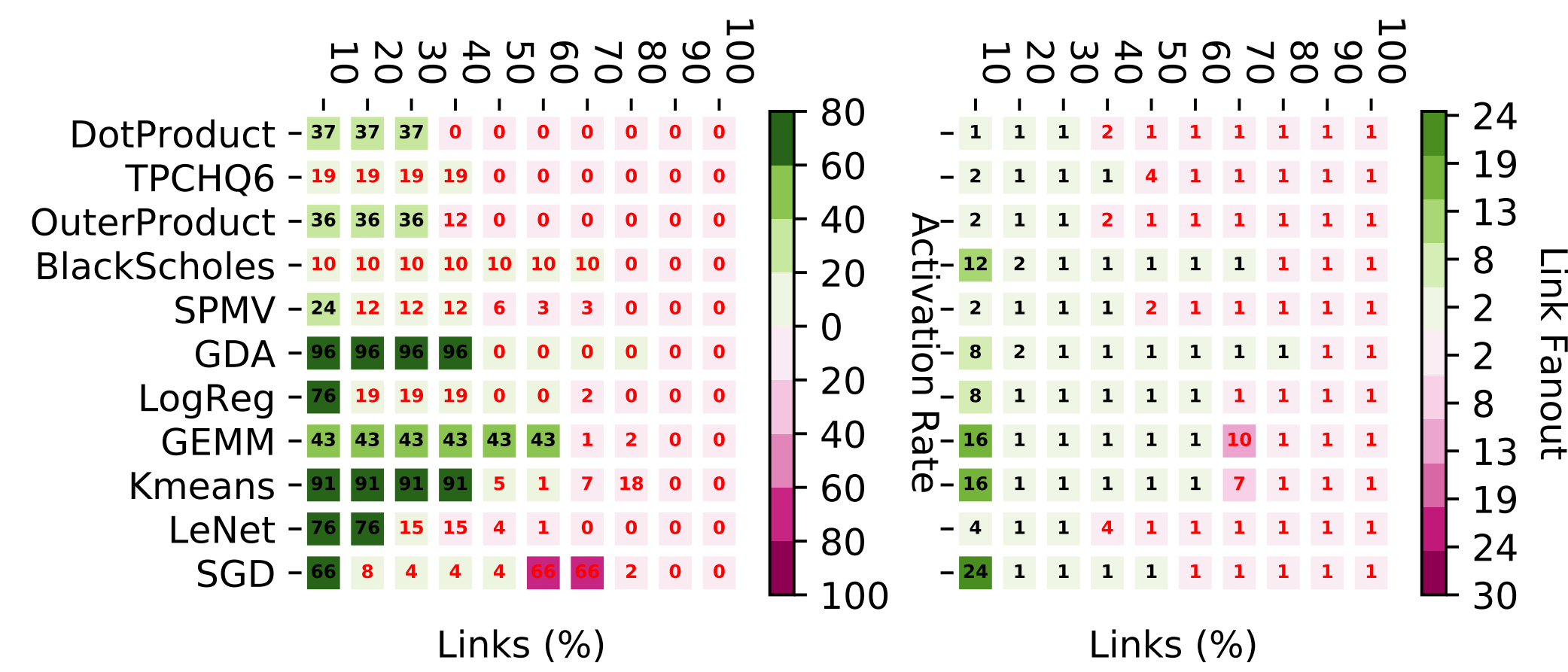- DRAM controllers with tile load and scatter-gather support

Plasticine demonstrated an average speedup of XXX and XXX times performance per watt than an FPGA.

How can we retain Plasticine's performance and efficiency while enabling new applications?

Compiler & Mapping Flow

Virtual Compute Unit Data-Flow Graph
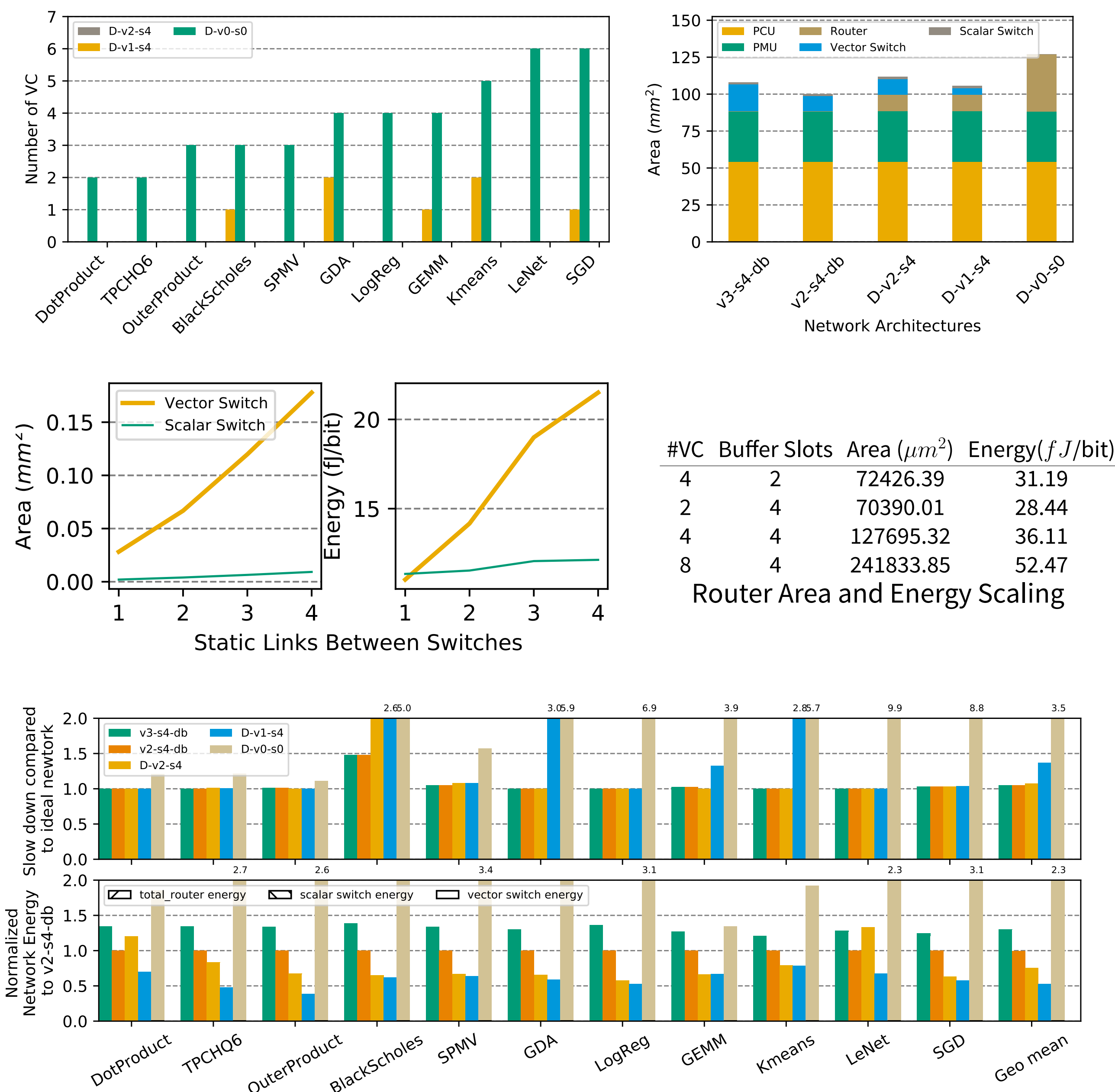

Physical Compute Unit

Hybrid Networks

How to improve link utilization given communication characteristics?

- Use static network for high-bandwidth and broadcast links
- Use dynamic network to encourage link sharing on low-activated links
- Specialize networks at different granularities

#VC	Buffer Slots	Area (μm^2)	Energy(fJ/bit)
4	2	72426.39	31.19
2	4	70390.01	28.44
4	4	127695.32	36.11
8	4	241833.85	52.47

Router Area and Energy Scaling

Future Work