Increasing Dynamism in Plasticine

Alexander Rucker
acrucker@stanford.edu

Yaqi Zhang
yaqiz@stanford.edu

Matthew Vilim
mvilim@stanford.edu

Background

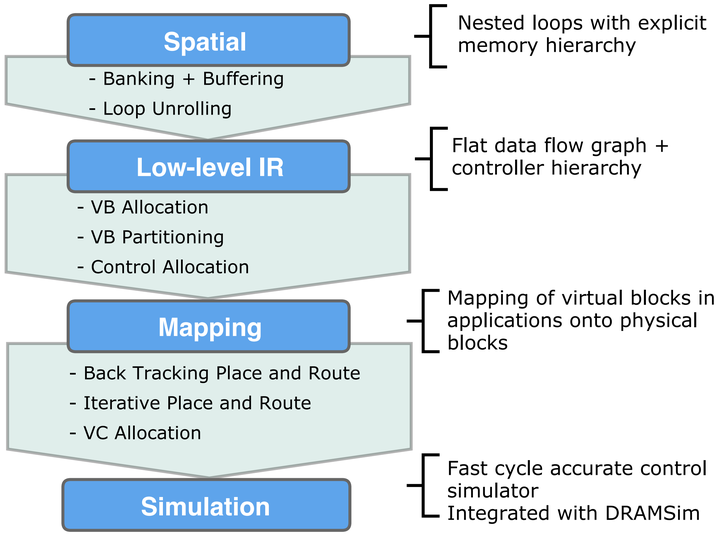
Plasticine is a vectorized Coarse-Grained Reconfigurable Array (CGRA), with the following key features:

- 6-stage, 16-lane 32-bit floating point SIMD pipelines
- Distributed 256-kByte memories
- DRAM controllers with tile load and scatter-gather support

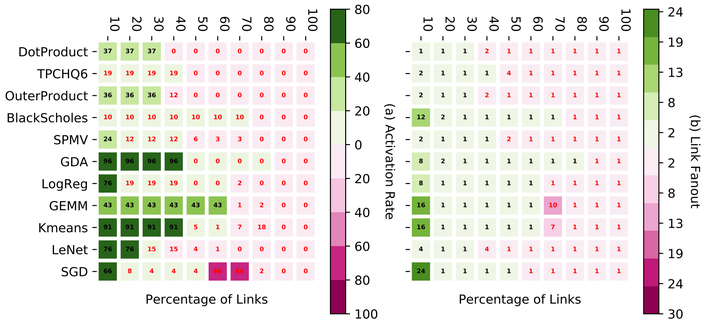
Plasticine demonstrated an average speedup of XXX and XXX times performance per watt than an FPGA.

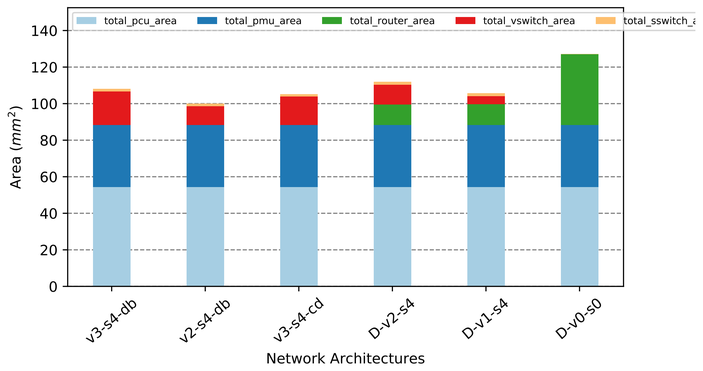
How can we retain Plasticine's performance and efficiency while enabling new classes of applications?

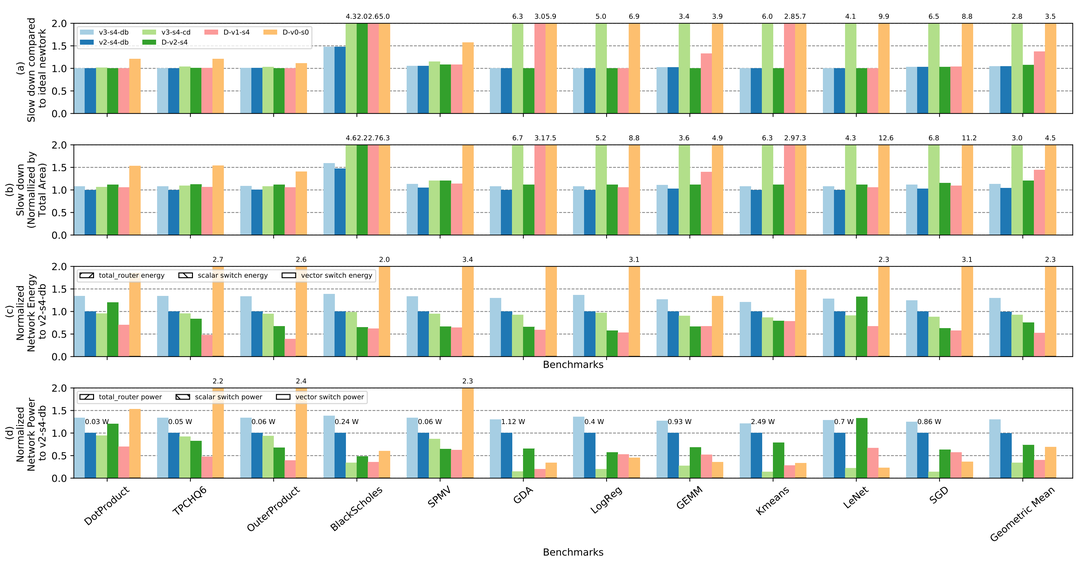
Compiler & Mapping Flow

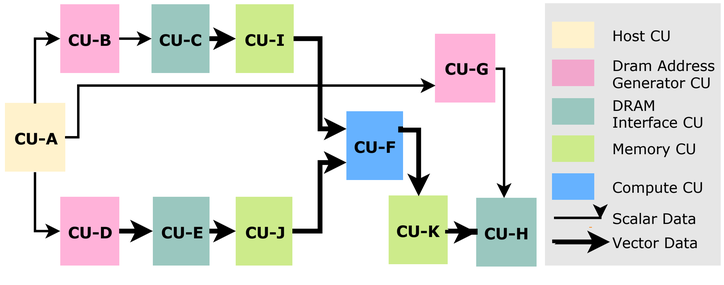


Hybrid Networks

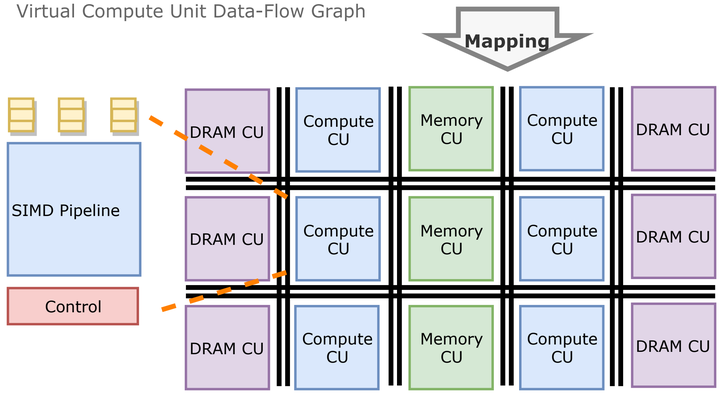








Virtual Compute Unit Data-Flow Graph



Physical Compute Unit