

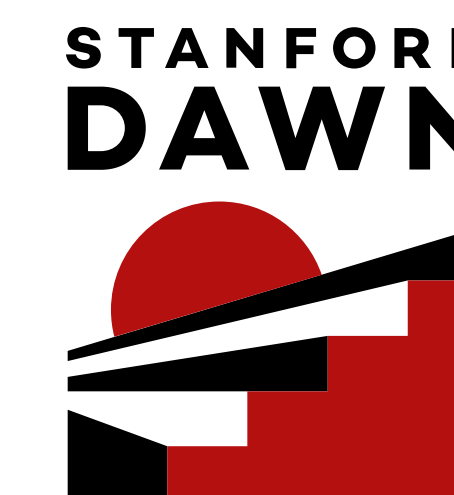


# Increasing Dynamism in Plasticine

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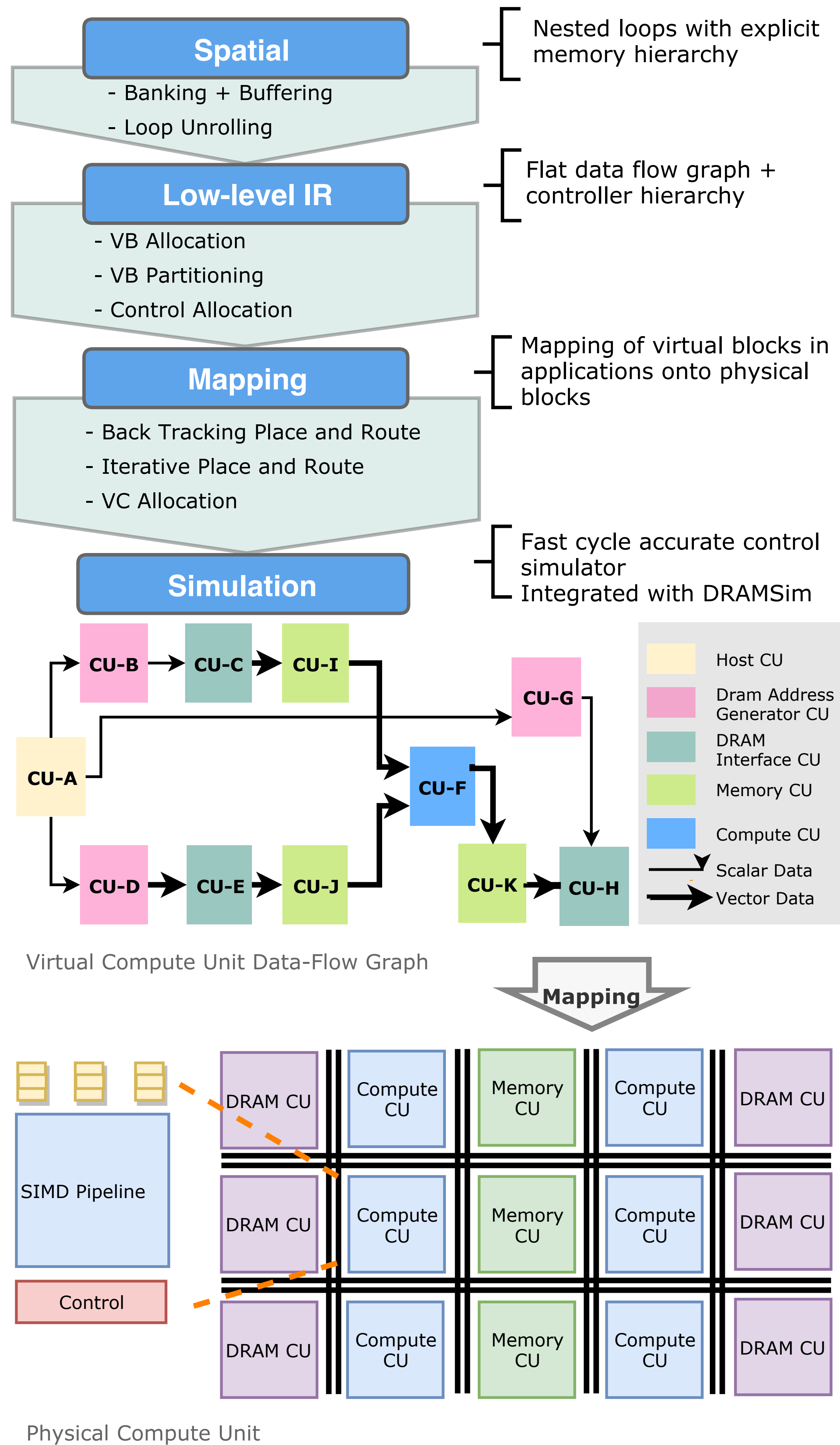


## — Background —

- Plasticine* a vectorized Coarse-Grained Reconfigurable Array with
  - 6-stage, 16-lane 32-bit floating point SIMD pipelines
  - Distributed 256-kByte memories
  - DRAM controllers with tile load and scatter-gather support
- Plasticine* demonstrated an average speedup of XXX and XXX times performance per watt than an FPGA.

*How can we retain Plasticine's performance and efficiency while enabling new classes of applications?*

## — Compiler & Mapping Flow —



## — Hybrid Networks —

