

# TMS416409A, TMS417409A, TMS426409A, TMS427409A 4194304 BY 4-BIT EXTENDED DATA OUT DYNAMIC RANDOM-ACCESS MEMORIES

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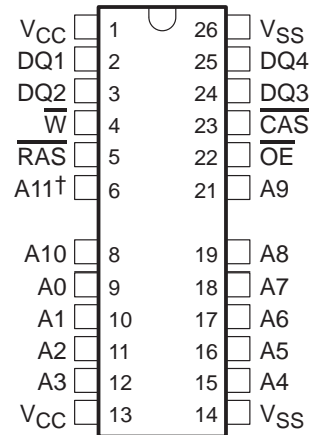
This data sheet is applicable to all TMS41x409As and TMS42x409As symbolized by Revision "B", Revision "E", and subsequent revisions as described in the device symbolization section.

- **Organization . . . 4194304 × 4**
- **Single Power Supply (5 V or 3.3 V)**
- **Performance Ranges:**

	ACCESS TIME	ACCESS TIME	ACCESS TIME	EDO CYCLE
	t <sub>RAC</sub> MAX	t <sub>CAC</sub> MAX	t <sub>AA</sub> MAX	t <sub>HPC</sub> MIN
'41x409A-50	50 ns	13 ns	25 ns	20 ns
'41x409A-60	60 ns	15 ns	30 ns	25 ns
'41x409A-70	70 ns	18 ns	35 ns	30 ns
'42x409A-50	50 ns	13 ns	25 ns	20 ns
'42x409A-60	60 ns	15 ns	30 ns	25 ns
'42x409A-70	70 ns	18 ns	35 ns	30 ns

- **Extended-Data-Out (EDO) Operation**
- **CAS-Before-RAS (CBR) Refresh**
- **Low Power Dissipation**
- **3-State Unlatched Output**
- **High-Reliability Plastic 24/26-Lead  
300-Mil-Wide Surface-Mount Small-Outline  
J-Lead (SOJ) Package (DJ Suffix) and  
24/26-Lead 300-Mil-Wide Surface-Mount  
Thin Small-Outline Package (TSOP)  
(DGA Suffix)**
- **Operating Free-Air Temperature Range  
0°C to 70°C**

## DJ/DGA PACKAGES (TOP VIEW)



## PIN NOMENCLATURE

A0–A11†	Address Inputs
DQ1–DQ4	Data In/Data Out
CAS	Column-Address Strobe
NC	No Internal Connection
OE	Output Enable
RAS	Row-Address Strobe
V <sub>CC</sub>	5-V or 3.3-V Supply†
V <sub>SS</sub>	Ground
W	Write Enable

† A11 is NC for TMS417409A and TMS427409A.

‡ See Available Options Table

## AVAILABLE OPTIONS

DEVICE	POWER SUPPLY	SELF REFRESH, BATTERY BACKUP	REFRESH CYCLES
TMS416409A	5 V	–	4096 in 64 ms
TMS417409A	5 V	–	2048 in 32 ms
TMS426409A	3.3 V	–	4096 in 64 ms
TMS427409A	3.3 V	–	2048 in 32 ms

## description

The TMS41x409A and TMS42x409A series are 16777216-bit dynamic random-access memory (DRAM) devices organized as 4194304 words of four bits each.

These devices feature maximum  $\overline{\text{RAS}}$  access times of 50, 60, and 70 ns. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416409A and TMS417409A are offered in a 24/26-lead plastic surface-mount SOJ package (DJ suffix). The TMS426409A and TMS427409A are offered in a 24/26-lead plastic surface-mount SOJ package (DJ suffix) and a 24-lead plastic surface-mount TSOP (DGA suffix). These packages are designed for operation from 0°C to 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

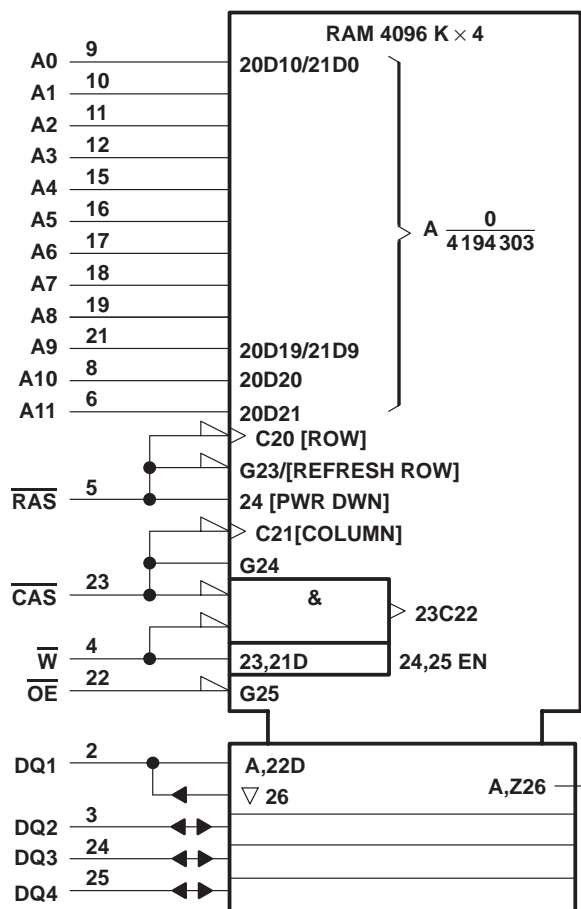
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# TMS416409A, TMS417409A, TMS426409A, TMS427409A 4194304 BY 4-BIT EXTENDED DATA OUT DYNAMIC RANDOM-ACCESS MEMORIES

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## logic symbol (TMS416409A and TMS426409A)†

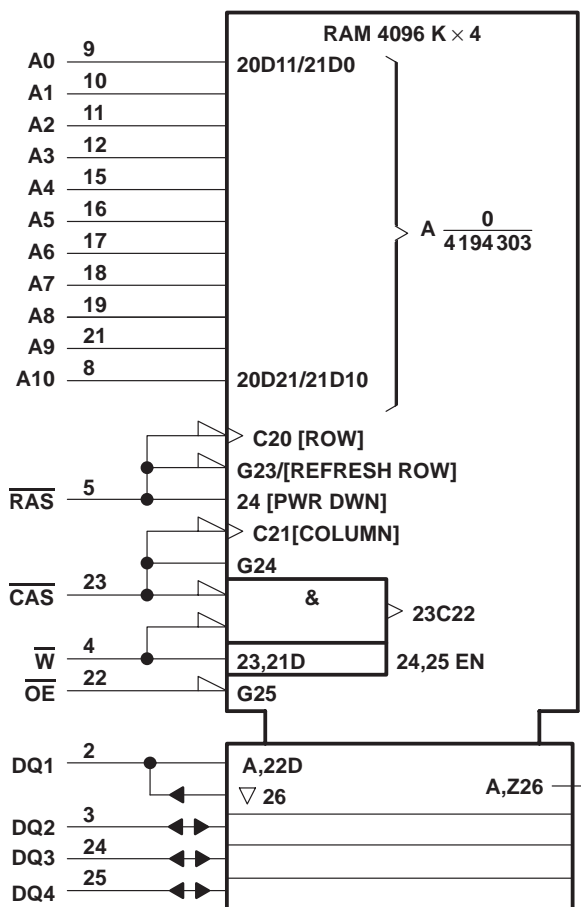


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

TMS416409A, TMS417409A, TMS426409A, TMS427409A  
4194304 BY 4-BIT EXTENDED DATA OUT  
DYNAMIC RANDOM-ACCESS MEMORIES

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logic symbol (TMS417409A and TMS427409A)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

# TMS416409A, TMS417409A, TMS426409A, TMS427409A

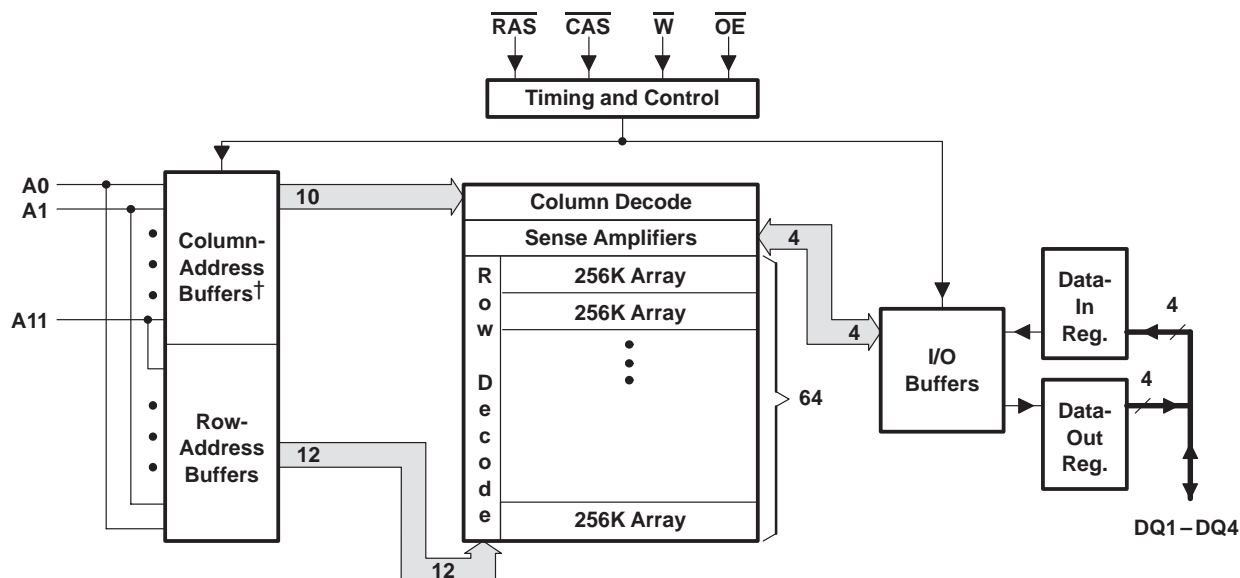
## 4194304 BY 4-BIT EXTENDED DATA OUT

### DYNAMIC RANDOM-ACCESS MEMORIES

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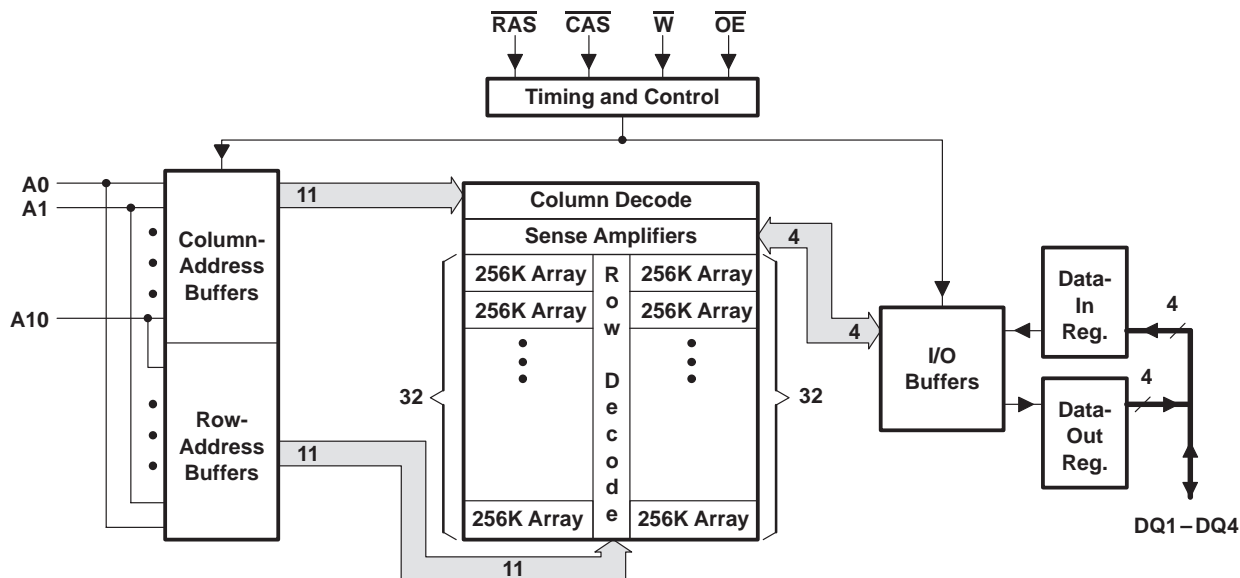
#### functional block diagram

#### TMS416409A, TMS426409A



† Column addresses A10 and A11 are not used.

#### TMS417409A, TMS427409A



## operation

### extended data out

Extended data out (EDO) allows data output rates of up to 50 MHz for 50-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and for address multiplex is eliminated. The maximum number of columns that can be accessed is determined by  $t_{RASP}$ , the maximum RAS low time.

Extended data out does not place the data in/data out pins (DQ pins) into the high-impedance state with the rising edge of  $\overline{CAS}$ . The output remains valid for the system to latch the data. After  $\overline{CAS}$  goes high, the DRAM decodes the next address.  $\overline{OE}$  and  $\overline{W}$  can control the output impedance. Descriptions of  $\overline{OE}$  and  $\overline{W}$  further explain EDO operation benefit.

### address: A0–A11 (TMS416409A and TMS426409A) and A0–A10 (TMS417409A and TMS427409A)

Twenty-two address bits are required to decode each of the 4194304 storage cell locations. For the TMS416409A and TMS426409A, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe ( $\overline{RAS}$ ). Ten column-address bits are set up on A0 through A9. For the TMS417409A and TMS427409A, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by  $\overline{RAS}$ . Eleven column-address bits are set up on A0 through A10. All addresses must be stable on or before the falling edge of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip enable because it activates the sense amplifiers as well as the row decoder.  $\overline{CAS}$  is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

### output enable ( $\overline{OE}$ )

$\overline{OE}$  controls the impedance of the output buffers. While  $\overline{CAS}$  and  $\overline{RAS}$  are low and  $\overline{W}$  is high,  $\overline{OE}$  can be brought low or high and the DQs transition between valid data and high impedance (see Figure 8). There are two methods for placing the DQs into the high-impedance state and maintaining that state during  $\overline{CAS}$  high time. The first method is to transition  $\overline{OE}$  high before  $\overline{CAS}$  transitions high and keep  $\overline{OE}$  high for  $t_{CHO}$  (hold time,  $\overline{OE}$  from  $\overline{CAS}$ ) past the  $\overline{CAS}$  transition. This disables the DQs and they remain disabled, regardless of  $\overline{OE}$ , until  $\overline{CAS}$  falls again. The second method is to have  $\overline{OE}$  low as  $\overline{CAS}$  transitions high. Then  $\overline{OE}$  can pulse high for a minimum of  $t_{OEP}$  (precharge time,  $\overline{OE}$ ) anytime during  $\overline{CAS}$  high time, disabling the DQs regardless of further transitions on  $\overline{OE}$  until  $\overline{CAS}$  falls again (see Figure 8).

### write enable ( $\overline{W}$ )

The read or write mode is selected through  $\overline{W}$ . A logic high on  $\overline{W}$  selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$  (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with  $\overline{OE}$  grounded. If  $\overline{W}$  goes low in an extended-data-out read cycle, the DQs are disabled so long as  $\overline{CAS}$  is high (see Figure 9).

### data in/data out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the later falling edge of  $\overline{CAS}$  or  $\overline{W}$  strobes data into the on-chip data latch with setup and hold times referenced to the later edge. The DQs drive valid data after all access times are met and remain valid except in cases described in the  $\overline{W}$  and  $\overline{OE}$  sections.

# TMS416409A, TMS417409A, TMS426409A, TMS427409A

## 4194304 BY 4-BIT EXTENDED DATA OUT

### DYNAMIC RANDOM-ACCESS MEMORIES

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#### **$\overline{\text{RAS}}$ -only refresh**

##### ***TMS416409A, TMS426409A***

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a  $\overline{\text{RAS}}$ -only refresh.

##### ***TMS417409A, TMS427409A***

A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a  $\overline{\text{RAS}}$ -only refresh.

#### **hidden refresh**

A hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{\text{CAS}}$  at  $V_{IL}$  after a read operation and cycling  $\overline{\text{RAS}}$  after a specified precharge period, similar to a  $\overline{\text{RAS}}$ -only refresh cycle. The external address is ignored, and the refresh address is generated internally.

#### **$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR) refresh**

CBR refresh is performed by bringing  $\overline{\text{CAS}}$  low earlier than  $\overline{\text{RAS}}$  (see parameter  $t_{CSR}$ ) and holding it low after  $\overline{\text{RAS}}$  falls (see parameter  $t_{CHR}$ ). For successive CBR refresh cycles,  $\overline{\text{CAS}}$  can remain low while cycling  $\overline{\text{RAS}}$ . The external address is ignored, and the refresh address is generated internally.

#### **power up**

To achieve proper device operation, an initial pause of 200  $\mu\text{s}$  followed by a minimum of eight initialization cycles is required after power up to the full  $V_{CC}$  level. These eight initialization cycles must include at least one refresh ( $\overline{\text{RAS}}$ -only or CBR) cycle.

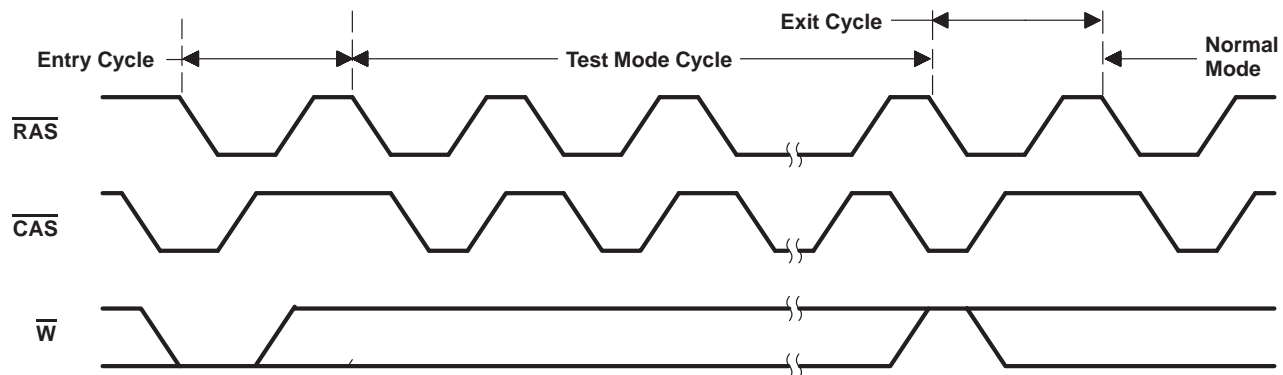
#### **test mode**

The test mode (see Figure 1) is initiated with a CBR-refresh cycle while simultaneously holding the  $\overline{\text{W}}$  input low. The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits test mode if a CBR refresh cycle with  $\overline{\text{W}}$  held high or a  $\overline{\text{RAS}}$ -only refresh cycle is performed.

In the test mode, the device is configured as 1024K bits  $\times$  4 bits for each DQ. Each DQ pin has a separate 4-bit parallel read and write data bus that ignores column addresses A0 and A1. During a read cycle, the four internal bits are compared for each DQ pin. If the four bits agree, DQ goes high; if not, DQ goes low. Test time is reduced by a factor of four for this series.



test mode (continued)



NOTE A: The states of  $\overline{\text{W}}$ , data in, and address are defined by the type of cycle used during test mode.

Figure 1. Test-Mode Cycle

# TMS416409A, TMS417409A, TMS426409A, TMS427409A

## 4194304 BY 4-BIT EXTENDED DATA OUT

### DYNAMIC RANDOM-ACCESS MEMORIES

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ (TMS41x409A)	– 1 V to 7 V
Supply voltage range, $V_{CC}$ (TMS42x409A)	– 0.5 V to 4.6 V
Voltage range on any pin (TMS41x409A) (see Note 1)	– 1 V to 7 V
Voltage range on any pin (TMS42x409A) (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	– 55°C to 125°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

#### recommended operating conditions

	TMS41x409A			TMS42x409A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	3	3.3	3.6	V
$V_{SS}$ Supply voltage		0			0		V
$V_{IH}$ High-level input voltage	2.4		6.5	2		$V_{CC} + 0.3$	V
$V_{IL}$ Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
$T_A$ Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.



**TMS416409A, TMS417409A, TMS426409A, TMS427409A**  
**4194304 BY 4-BIT EXTENDED DATA OUT**  
**DYNAMIC RANDOM-ACCESS MEMORIES**

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

**TMS416409A**

PARAMETER	TEST CONDITIONS†	'416409A-50		'416409A-60		'416409A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$ High-level output voltage	$I_{OH} = -5\text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$ Low-level output voltage	$I_{OL} = 4.2\text{ mA}$		0.4		0.4		0.4	V
$I_I$ Input current (leakage)	$V_{CC} = 5.5\text{ V}$ , $V_I = 0\text{ V to } 6.5\text{ V}$ , All others = $0\text{ V to } V_{CC}$		$\pm 10$		$\pm 10$		$\pm 10$	$\mu\text{A}$
$I_O$ Output current (leakage)	$V_{CC} = 5.5\text{ V}$ , $V_O = 0\text{ V to } V_{CC}$ , CAS high		$\pm 10$		$\pm 10$		$\pm 10$	$\mu\text{A}$
$I_{CC1}^{\ddagger\$}$ Average read- or write-cycle current	$V_{CC} = 5.5\text{ V}$ , Minimum cycle		100		80		70	mA
$I_{CC2}$ Average standby current	$V_{IH} = 2.4\text{ V (TTL)}$ , After one memory cycle, RAS and CAS high		2		2		2	mA
	$V_{IH} = V_{CC} - 0.2\text{ V (CMOS)}$ , After one memory cycle, RAS and CAS high		1		1		1	mA
$I_{CC3}^{\ddagger\$}$ Average refresh current (RAS-only refresh or CBR)	$V_{CC} = 5.5\text{ V}$ , Minimum cycle, RAS cycling, CAS high (RAS only), RAS low after CAS low (CBR)		100		80		70	mA
$I_{CC4}^{\ddagger\parallel}$ Average EDO current	$V_{CC} = 5.5\text{ V}$ , $t_{HPC} = \text{MIN}$ , RAS low, CAS cycling		100		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while  $\overline{\text{RAS}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle,  $t_{HPC}$

**TMS416409A, TMS417409A, TMS426409A, TMS427409A**  
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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**TMS417409A**

PARAMETER	TEST CONDITIONS†	'417409A-50		'417409A-60		'417409A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	2.4		2.4		2.4		V
V <sub>OL</sub>	Low-level output voltage	0.4		0.4		0.4		V
I <sub>I</sub>	Input current (leakage)	± 10		± 10		± 10		μA
I <sub>O</sub>	Output current (leakage)	± 10		± 10		± 10		μA
I <sub>CC1</sub> ‡§	Average read- or write-cycle current	130		110		100		mA
I <sub>CC2</sub>	Average standby current	2		2		2		mA
		1		1		1		mA
I <sub>CC3</sub> ‡§	Average refresh current (RAS-only refresh or CBR)	130		110		100		mA
I <sub>CC4</sub> ‡¶	Average EDO current	110		90		80		mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while  $\overline{\text{RAS}} = V_{\text{IL}}$

¶ Measured with a maximum of one address change during each EDO cycle,  $t_{\text{HPC}}$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

**TMS426409A**

PARAMETER		TEST CONDITIONS†		'426409A-50		'426409A-60		'426409A-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I <sub>OH</sub> = – 100 µA	LVC MOS	V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.2		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2 mA	LVTTL		0.4		0.4		0.4	V
		I <sub>OL</sub> = 100 µA	LVC MOS		0.2		0.2		0.2	
I <sub>I</sub>	Input current (leakage)	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 V to 3.9 V, All others = 0 V to V <sub>CC</sub>			± 10		± 10		± 10	µA
I <sub>O</sub>	Output current (leakage)	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> , CAS high			± 10		± 10		± 10	µA
I <sub>CC1</sub> ‡§	Average read- or write- cycle current	V <sub>CC</sub> = 3.6 V, Minimum cycle			90		70		60	mA
I <sub>CC2</sub>	Average standby current	V <sub>IH</sub> = 2 V (LVTTL) After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			2		2		2	mA
		V <sub>IH</sub> = V <sub>CC</sub> – 0.2 V (LVC MOS), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			1		1		1	mA
I <sub>CC3</sub> ‡§	Average refresh current (RAS-only refresh or CBR)	V <sub>CC</sub> = 3.6 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high (RAS-only refresh), $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)			90		70		60	mA
I <sub>CC4</sub> ‡¶	Average EDO current	V <sub>CC</sub> = 3.6 V, RAS low, t <sub>HPC</sub> = MIN, CAS cycling			100		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while  $\overline{\text{RAS}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t<sub>HPC</sub>

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**TMS427409A**

PARAMETER		TEST CONDITIONS†		'427409A - 50		'427409A - 60		'427409A - 70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 2 mA	LVTTL	2.4		2.4		2.4		V
		I <sub>OH</sub> = - 100 µA	LVC MOS	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2 mA	LVTTL		0.4		0.4		0.4	V
		I <sub>OL</sub> = 100 µA	LVC MOS		0.2		0.2		0.2	
I <sub>I</sub>	Input current (leakage)	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 V to 3.9 V, All others = 0 V to V <sub>CC</sub>			± 10		± 10		± 10	µA
I <sub>O</sub>	Output current (leakage)	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> , $\overline{\text{CAS}}$ high			± 10		± 10		± 10	µA
I <sub>CC1</sub> ‡§	Average read- or write- cycle current	V <sub>CC</sub> = 3.6 V, Minimum cycle			120		100		90	mA
I <sub>CC2</sub>	Average standby current	V <sub>IH</sub> = 2 V (LVTTL) After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			2		2		2	mA
		V <sub>IH</sub> = V <sub>CC</sub> - 0.2 V (LVC MOS), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high			1		1		1	mA
I <sub>CC3</sub> ‡§	Average refresh current (RAS-only refresh or CBR)	V <sub>CC</sub> = 3.6 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high (RAS-only refresh), $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)			120		100		90	mA
I <sub>CC4</sub> ‡¶	Average EDO current	V <sub>CC</sub> = 3.6 V, $\overline{\text{RAS}}$ low, $t_{\text{HPC}}$ = MIN, $\overline{\text{CAS}}$ cycling			110		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while  $\overline{\text{RAS}}$  = V<sub>IL</sub>

¶ Measured with a maximum of one address change during each EDO cycle,  $t_{\text{HPC}}$

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**4194304 BY 4-BIT EXTENDED DATA OUT**  
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**capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1$  MHz (see Note 3)**

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
$C_o$	Output capacitance‡		7	pF

† A11 is NC (no internal connection) for TMS417409A and TMS427409A.

‡  $\overline{CAS}$  and  $\overline{OE} = V_{IH}$  to disable outputs

NOTE 3:  $V_{CC} = \text{NOM supply voltage} \pm 10\%$ , and the bias on pins under test is 0 V.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)**

PARAMETER	'41x409A-50 '42x409A-50		'41x409A-60 '42x409A-60		'41x409A-70 '42x409A-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AA}$	Access time from column address (see Note 5)		25	30	35		ns
$t_{CAC}$	Access time from $\overline{CAS}$ (see Note 5)		13	15	18		ns
$t_{CPA}$	Access time from $\overline{CAS}$ precharge (see Note 5)		28	35	40		ns
$t_{RAC}$	Access time from $\overline{RAS}$ (see Note 5)		50	60	70		ns
$t_{OEA}$	Access time from $\overline{OE}$ (see Note 5)		13	15	18		ns
$t_{CLZ}$	Delay time, $\overline{CAS}$ to output in low impedance		0	0	0		ns
$t_{REZ}$	Output buffer turn off delay from $\overline{RAS}$ (see Note 6)		3	13	3	18	ns
$t_{CEZ}$	Output buffer turn off delay from $\overline{CAS}$ (see Note 6)		3	13	3	18	ns
$t_{OEZ}$	Output buffer turn off delay from $\overline{OE}$ (see Note 6)		3	13	3	18	ns
$t_{WEZ}$	Output buffer turn off delay from $\overline{W}$ (see Note 6)		3	13	3	15	ns

NOTES: 4. With ac parameters, it is assumed that  $t_T = 2$  ns.

5. For TMS42x409A, access times are measured with output reference levels of  $V_{OH} = 2$  V and  $V_{OL} = 0.8$  V.

6. The maximum values of  $t_{REZ}$ ,  $t_{CEZ}$ ,  $t_{OEZ}$ , and  $t_{WEZ}$  are specified when the output is no longer driven. Data in should not be driven until one of the applicable maximum specifications is satisfied.



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**EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)**

	'41x409A-50 '42x409A-50		'41x409A-60 '42x409A-60		'41x409A-70 '42x409A-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>HPC</sub> Cycle time, EDO page mode, read-write	20		25		30		ns
t <sub>PRWC</sub> Cycle time, EDO read-write	57		68		78		ns
t <sub>CSH</sub> Delay time, $\overline{\text{RAS}}$ active to $\overline{\text{CAS}}$ precharge	40		48		58		ns
t <sub>CHO</sub> Hold time, $\overline{\text{OE}}$ from $\overline{\text{CAS}}$	7		10		10		ns
t <sub>DOH</sub> Hold time, output from $\overline{\text{CAS}}$	5		5		5		ns
t <sub>CAS</sub> Pulse duration, $\overline{\text{CAS}}$ active (see Note 7)	8	10 000	10	10 000	12	10 000	ns
t <sub>WPE</sub> Pulse duration, $\overline{\text{W}}$ active (output disable only)	7		7		7		ns
t <sub>OCH</sub> Setup time, $\overline{\text{OE}}$ before $\overline{\text{CAS}}$	8		10		10		ns
t <sub>CP</sub> Pulse duration, $\overline{\text{CAS}}$ precharge	8		10		10		ns
t <sub>OEP</sub> Precharge time, $\overline{\text{OE}}$	5		5		5		ns

NOTES: 4: With ac parameters, it is assumed that  $t_T = 2$  ns.  
7: In a read-write cycle, t<sub>CWD</sub> and t<sub>CWL</sub> must be observed.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)**

		'41x409A-50 '42x409A-50		'41x409A-60 '42x409A-60		'41x409A-70 '42x409A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Cycle time, random read or write	84		104		124		ns
t <sub>RWC</sub>	Cycle time, read-write	111		135		160		ns
t <sub>RASP</sub>	Pulse duration, $\overline{\text{RAS}}$ active, fast page mode (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t <sub>RAS</sub>	Pulse duration, $\overline{\text{RAS}}$ active, non-page mode (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t <sub>RP</sub>	Pulse duration, $\overline{\text{RAS}}$ precharge	30		40		50		ns
t <sub>WP</sub>	Pulse duration, write command	8		10		10		ns
t <sub>ASC</sub>	Setup time, column address	0		0		0		ns
t <sub>ASR</sub>	Setup time, row address	0		0		0		ns
t <sub>DS</sub>	Setup time, data in (see Note 9)	0		0		0		ns
t <sub>RCS</sub>	Setup time, read command	0		0		0		ns
t <sub>CWL</sub>	Setup time, write command before $\overline{\text{CAS}}$ precharge	8		10		12		ns
t <sub>RWL</sub>	Setup time, write command before $\overline{\text{RAS}}$ precharge	8		10		12		ns
t <sub>WCS</sub>	Setup time, write command before $\overline{\text{CAS}}$ active (early-write only)	0		0		0		ns
t <sub>WRP</sub>	Setup time, $\overline{\text{W}}$ high before $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t <sub>WTS</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ low (test mode only)	10		10		10		ns
t <sub>CSR</sub>	Setup time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only)	5		5		5		ns
t <sub>CAH</sub>	Hold time, column address	8		10		12		ns
t <sub>DH</sub>	Hold time, data in (see Note 9)	8		10		12		ns
t <sub>RAH</sub>	Hold time, row address	8		10		10		ns
t <sub>RCH</sub>	Hold time, read command referenced to $\overline{\text{CAS}}$ (see Note 10)	0		0		0		ns
t <sub>RRH</sub>	Hold time, read command referenced to $\overline{\text{RAS}}$ (see Note 10)	0		0		0		ns
t <sub>WCH</sub>	Hold time, write command during $\overline{\text{CAS}}$ active (early-write only)	8		10		12		ns
t <sub>ROH</sub>	Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$	8		10		10		ns
t <sub>WRH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh)	10		10		10		ns
t <sub>WTH</sub>	Hold time, $\overline{\text{W}}$ low after $\overline{\text{RAS}}$ low (test mode only)	10		10		10		ns
t <sub>CHR</sub>	Hold time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only)	10		10		10		ns
t <sub>OEH</sub>	Hold time, $\overline{\text{OE}}$ command	13		15		18		ns
t <sub>RHCP</sub>	Hold time, $\overline{\text{RAS}}$ active from $\overline{\text{CAS}}$ precharge	28		35		40		ns

- NOTES: 4. With ac parameters, it is assumed that  $t_T = 2$  ns.  
8. In a read-write cycle, t<sub>RWD</sub> and t<sub>RWL</sub> must be observed.  
9. Referenced to the later of CAS or W in write operations  
10. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4) (continued)**

		'41x409A-50 '42x409A-50		'41x409A-60 '42x409A-60		'41x409A-70 '42x409A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AWD</sub>	Delay time, column address to write command (read-write only)	42		49		57		ns
t <sub>CPW</sub>	Delay time, $\overline{W}$ low after xCAS precharge (read-write only)	45		54		62		ns
t <sub>CRP</sub>	Delay time, $\overline{CAS}$ precharge to RAS	5		5		5		ns
t <sub>CWD</sub>	Delay time, $\overline{CAS}$ to write command (read-write only)	30		34		40		ns
t <sub>OED</sub>	Delay time, $\overline{OE}$ to data in	13		15		18		ns
t <sub>RAD</sub>	Delay time, $\overline{RAS}$ to column address (see Note 11)	10	25	12	30	12	35	ns
t <sub>RAL</sub>	Delay time, column address to $\overline{RAS}$ precharge	25		30		35		ns
t <sub>CAL</sub>	Delay time, column address to $\overline{CAS}$ precharge	18		20		25		ns
t <sub>RCD</sub>	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 11)	12	37	14	45	14	52	ns
t <sub>RPC</sub>	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$	5		5		5		ns
t <sub>RSR</sub>	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge	8		10		12		ns
t <sub>RWD</sub>	Delay time, $\overline{RAS}$ to write command (read-write only)	67		79		92		ns
t <sub>TAA</sub>	Access time from address (test mode)	30		35		40		ns
t <sub>TCPA</sub>	Access time, from column precharge (test mode)	35		40		45		ns
t <sub>TRAC</sub>	Access time, from $\overline{RAS}$ (test mode)	55		65		75		ns
t <sub>T</sub>	Transition time	2	30	2	30	2	30	ns
t <sub>REF</sub>	Refresh time interval	'4x6409A		64		64		ms
		'4x7409A		32		32		ms

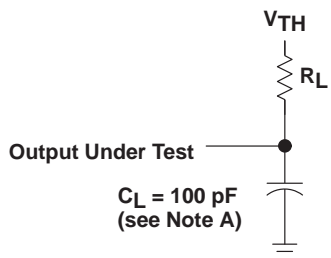
NOTES: 4. With ac parameters, it is assumed that t<sub>T</sub> = 2 ns.

11. The maximum value is specified only to ensure access time.

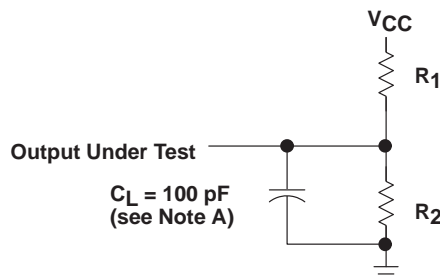




## PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT



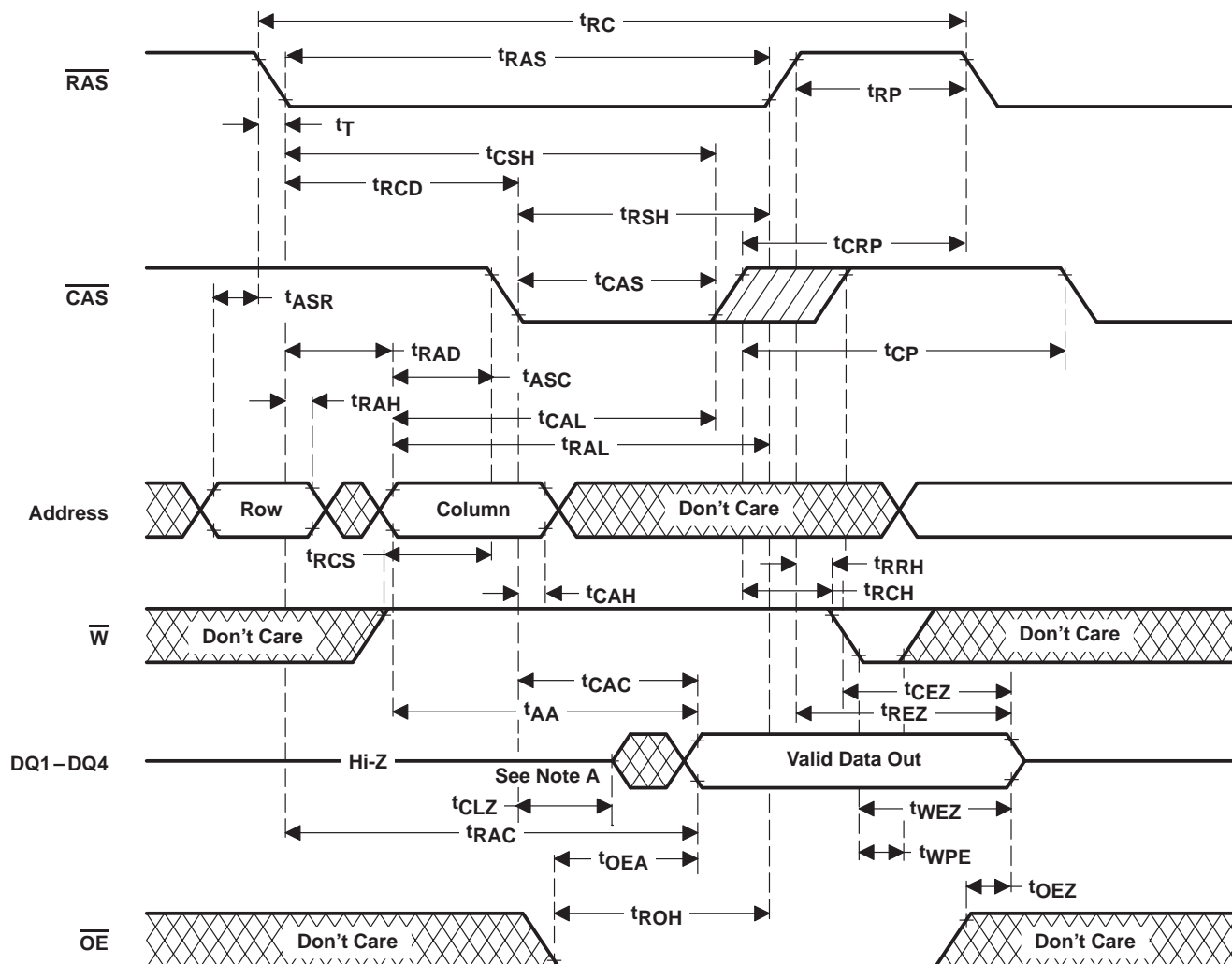
(b) ALTERNATE LOAD CIRCUIT

NOTE A:  $C_L$  includes probe and fixture capacitance.

DEVICE	$V_{CC}$ (V)	$R_1$ ( $\Omega$ )	$R_2$ ( $\Omega$ )	$V_{TH}$ (V)	$R_L$ ( $\Omega$ )
'41x409A	5	828	295	1.31	218
'42x409A	3.3	1178	868	1.4	500

Figure 2. Load Circuits for Timing Parameters

# PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

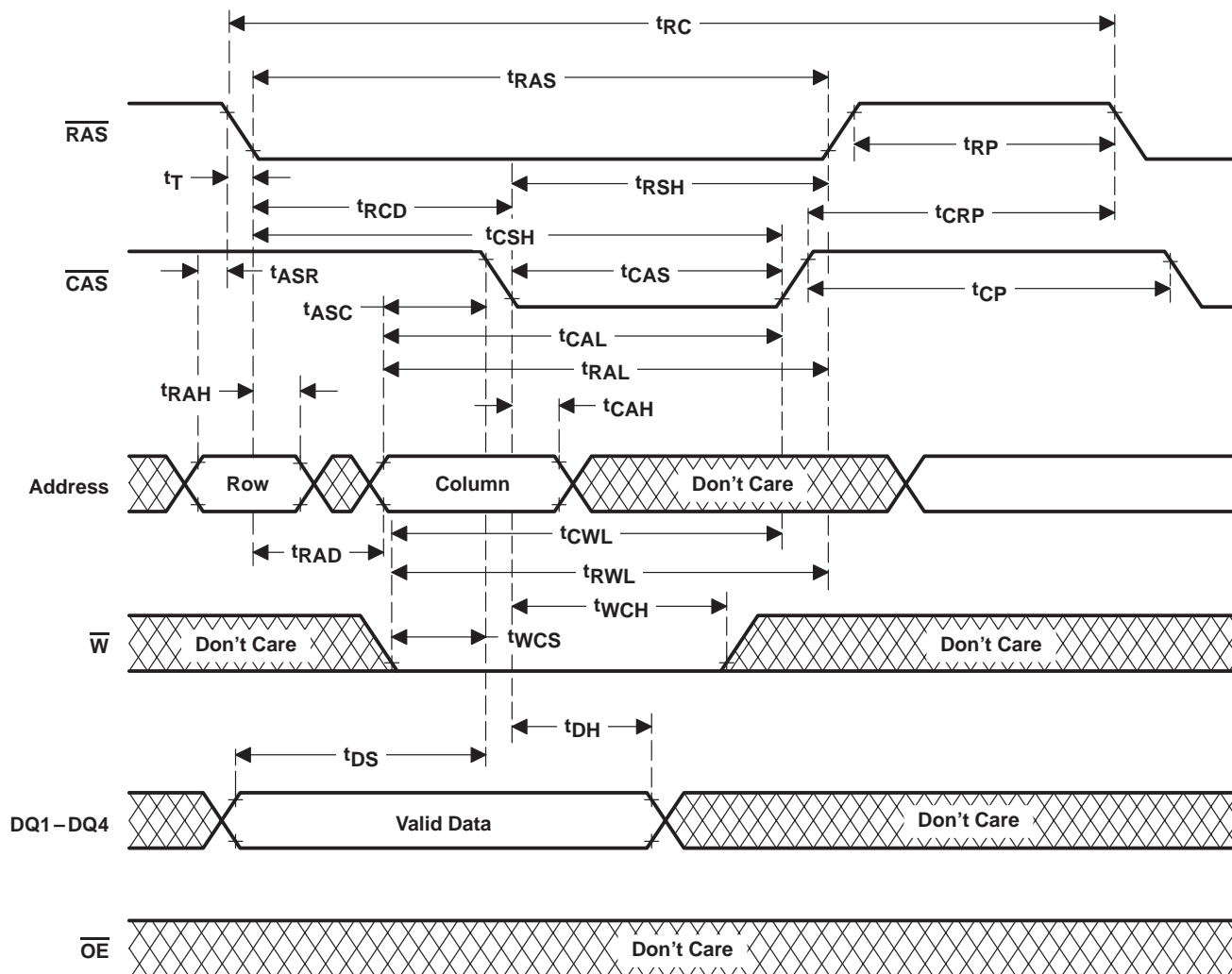


Figure 4. Early-Write-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

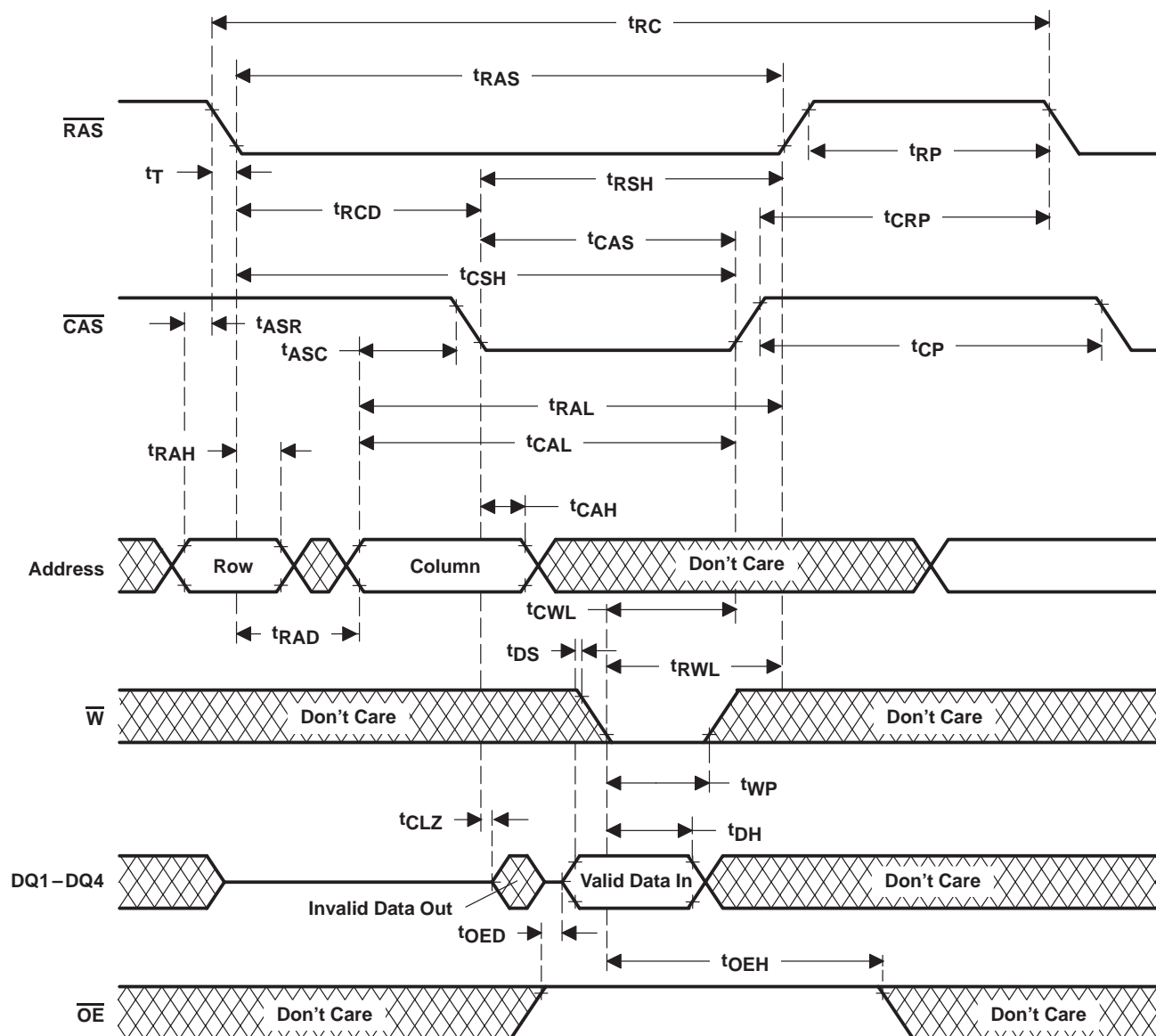
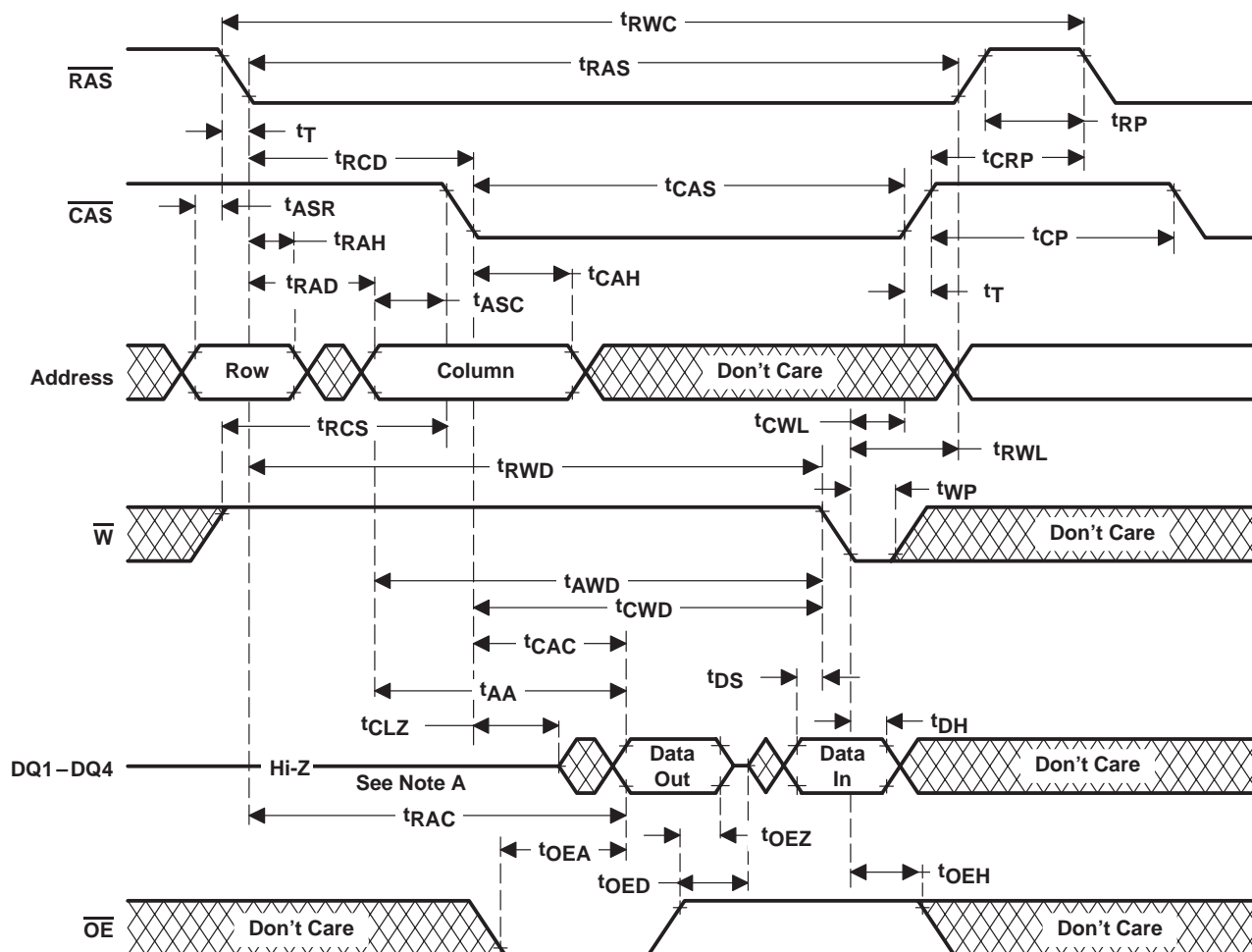


Figure 5. Write-Cycle Timing

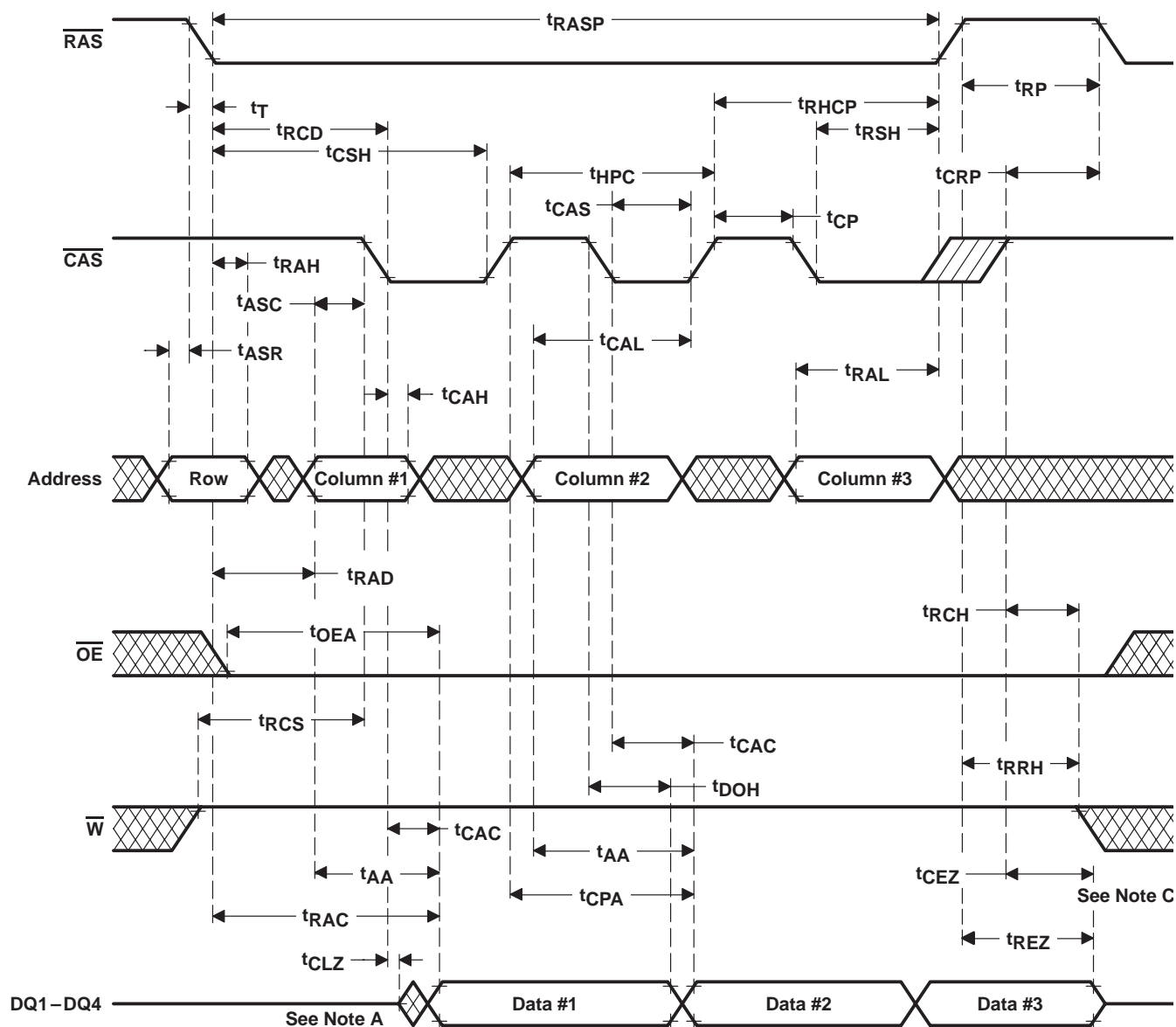
# PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION



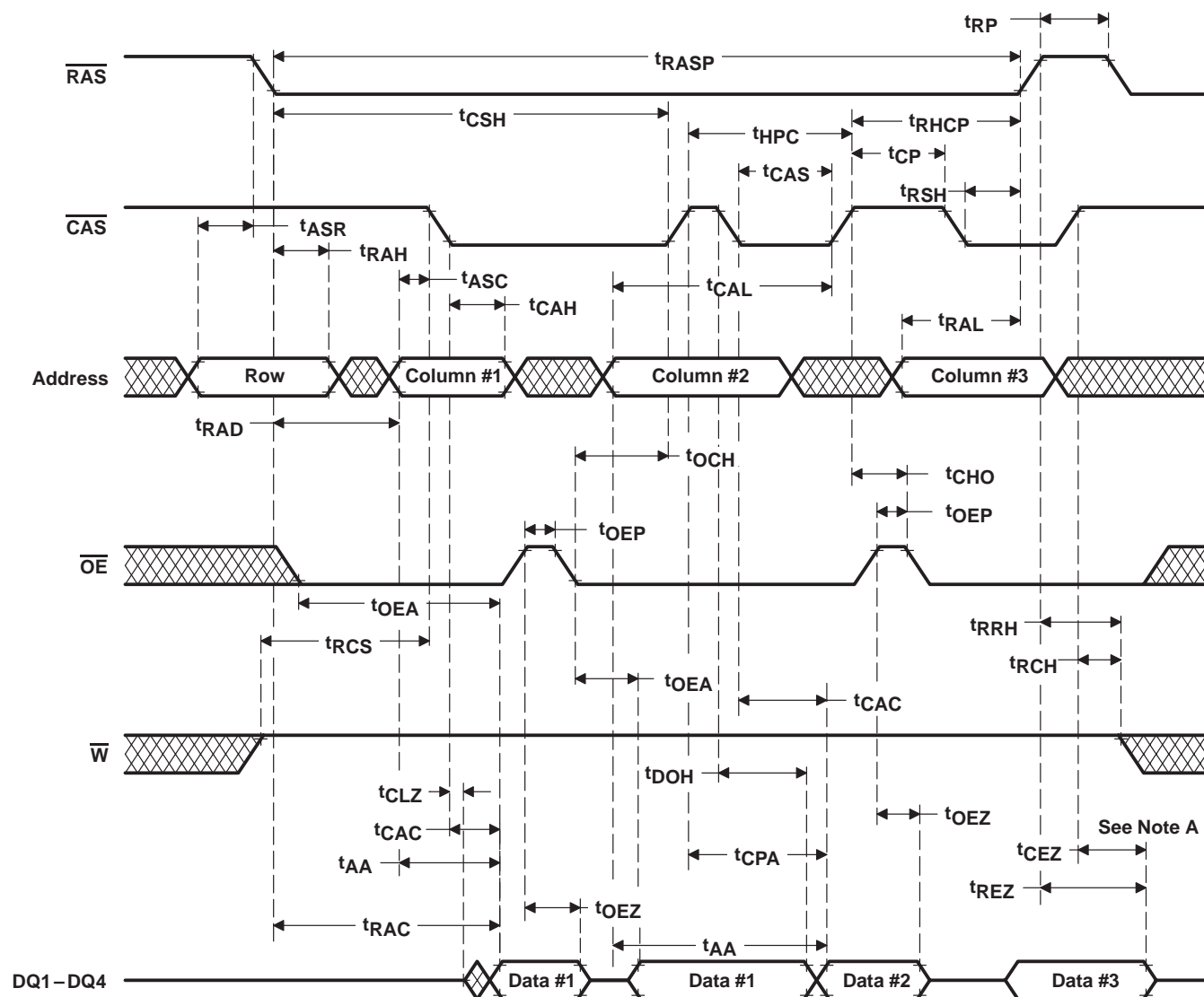
NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

B. Access time is  $t_{CPA}$ ,  $t_{AA}$ , or  $t_{CAC}$ -dependent.

C. Output is turned off by  $t_{CEZ}$  if RAS goes high during CAS low.

Figure 7. EDO Read Cycle

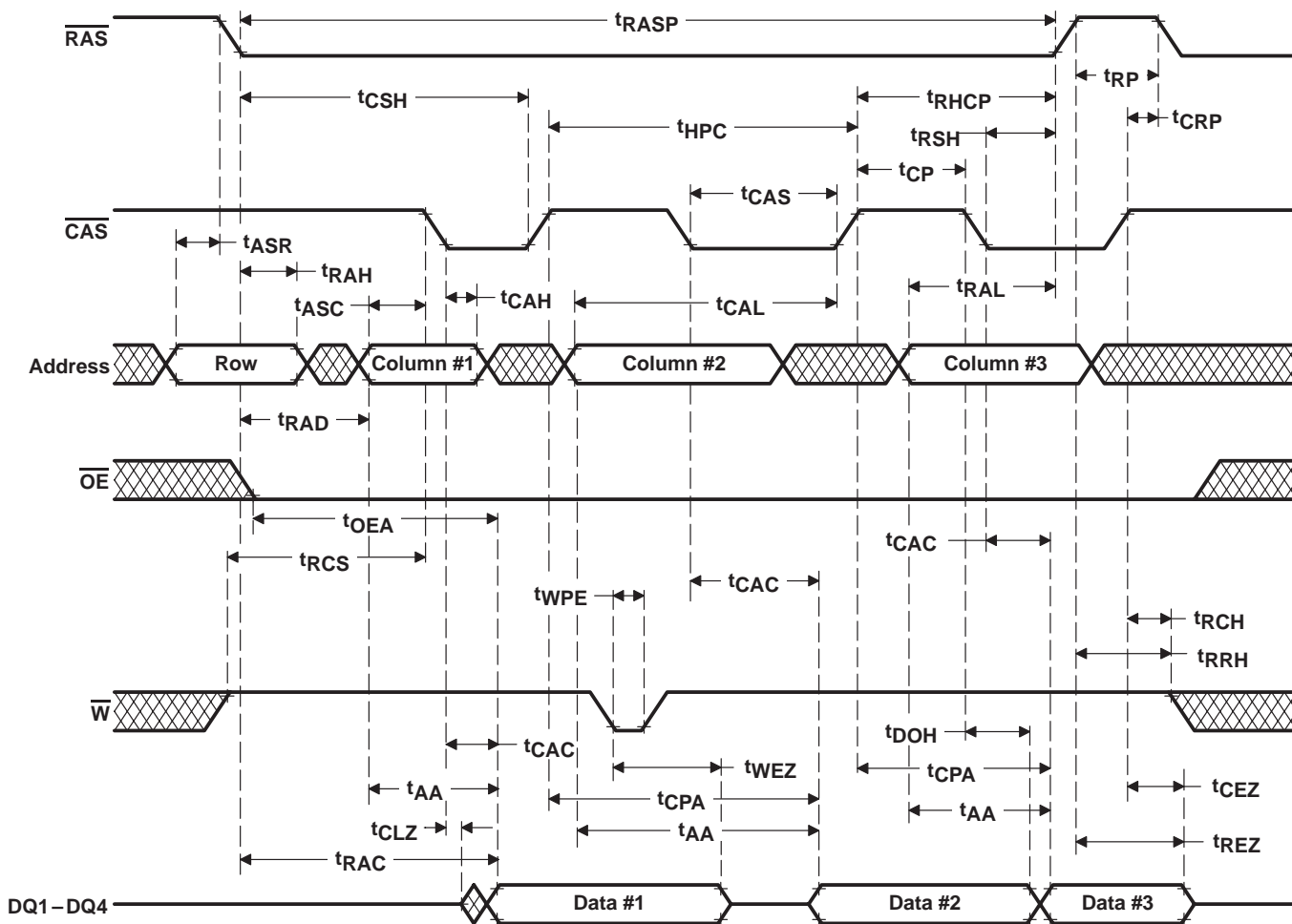
# PARAMETER MEASUREMENT INFORMATION



NOTE A: Output is turned off by  $t_{CEZ}$  if  $\overline{RAS}$  goes high during  $\overline{CAS}$  low.

Figure 8. EDO Read-Cycle With  $\overline{OE}$  Control

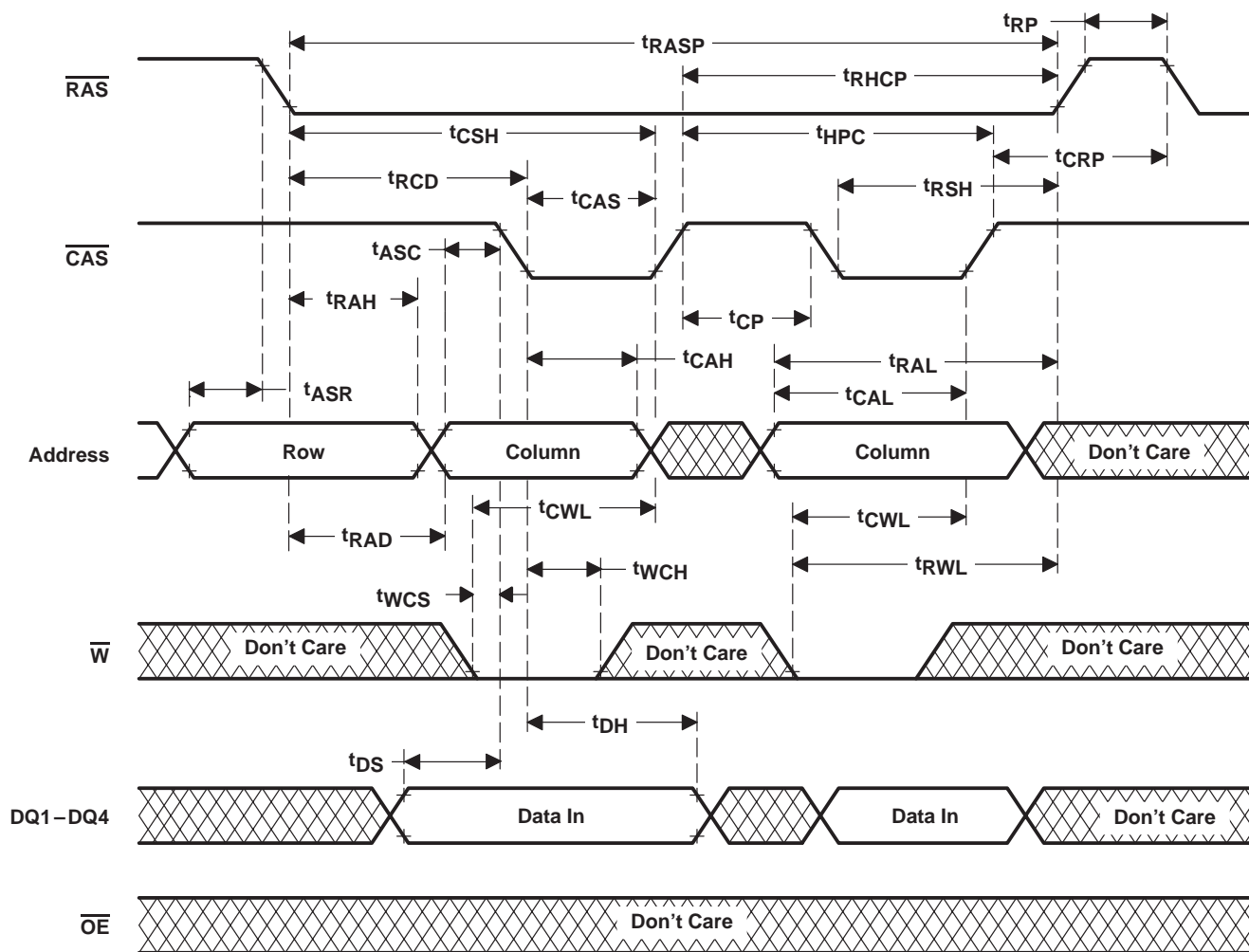
## PARAMETER MEASUREMENT INFORMATION



### Figure 9. EDO Read-Cycle With $\overline{W}$ Control



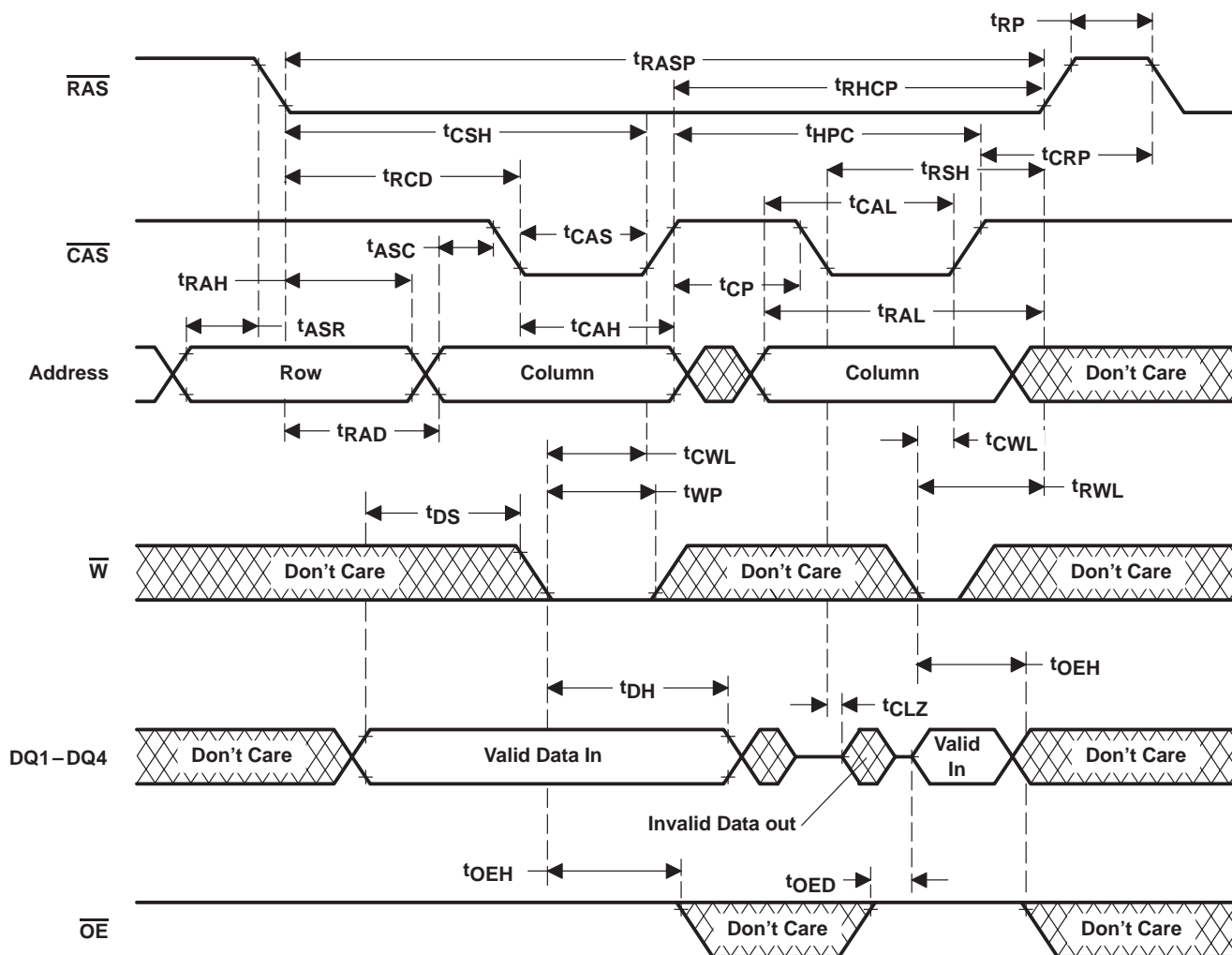
# PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 10. EDO Early-Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 11. EDO Write-Cycle Timing

### Figure 12. EDO Read-Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION

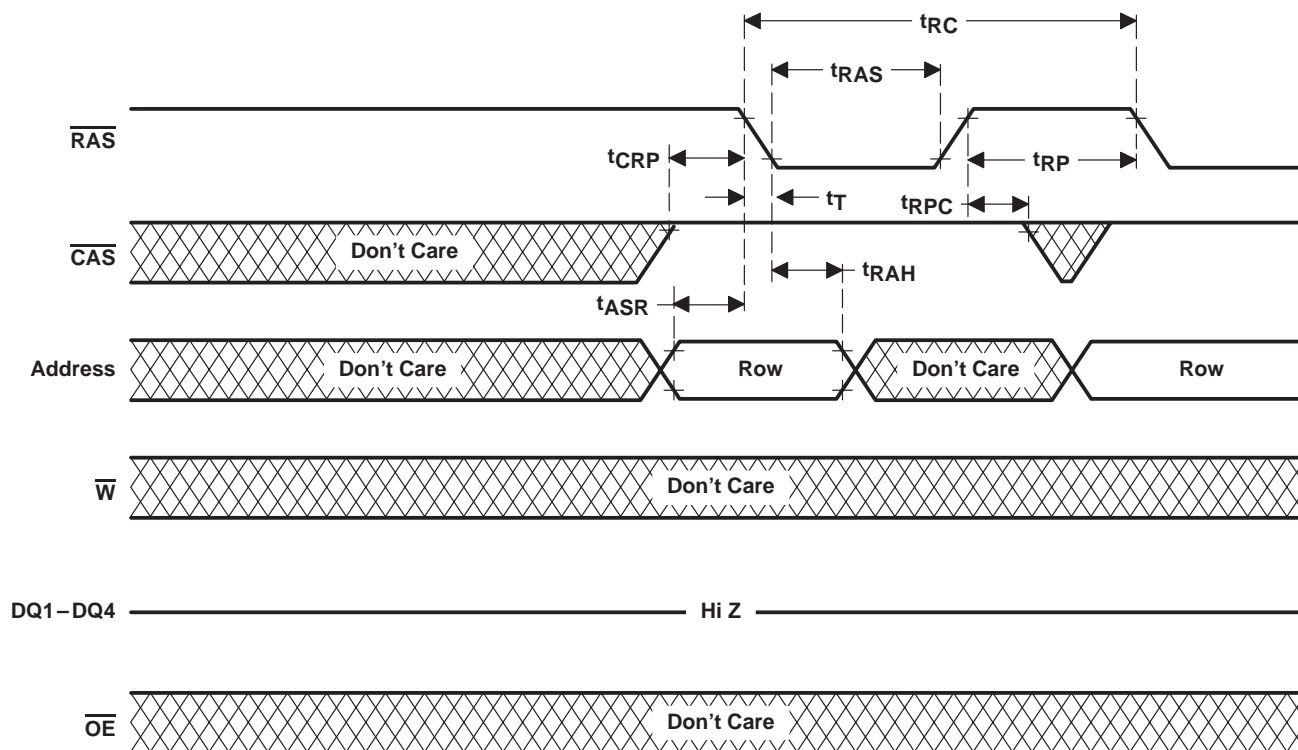


Figure 13.  $\overline{\text{RAS}}$ -Only Refresh-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

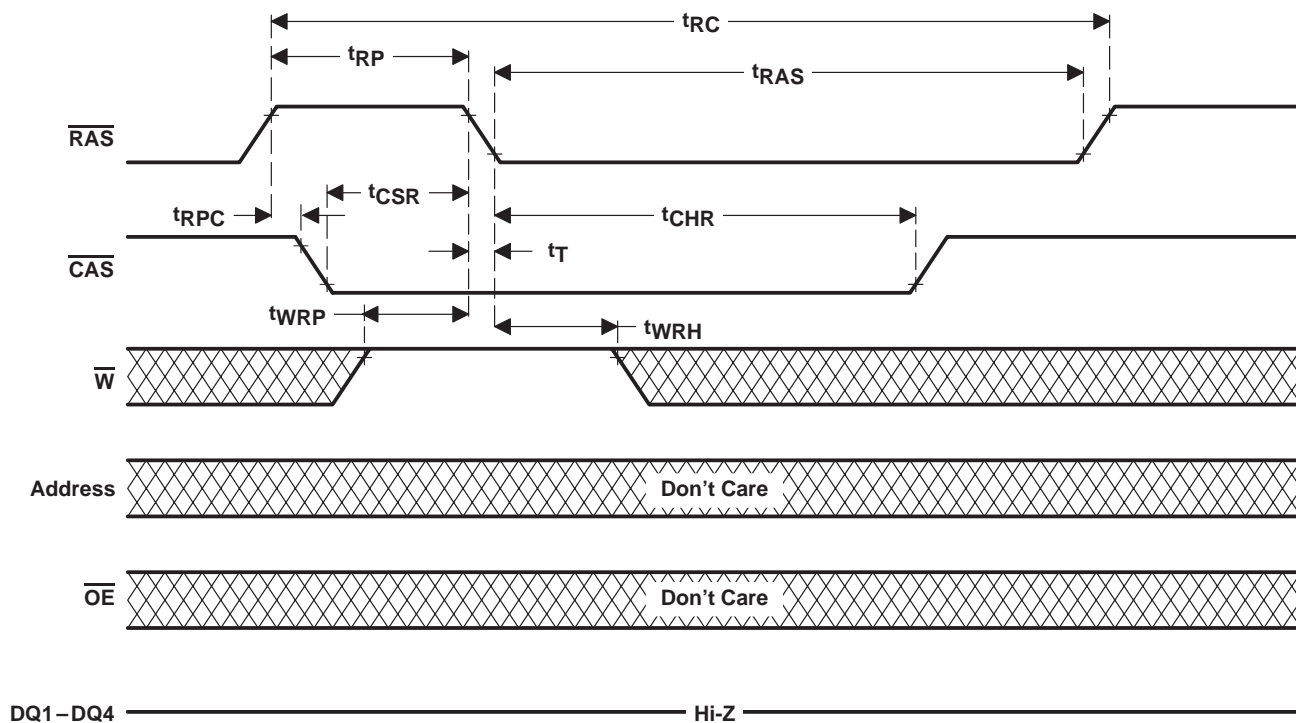


Figure 14. Automatic-CBR-Refresh-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

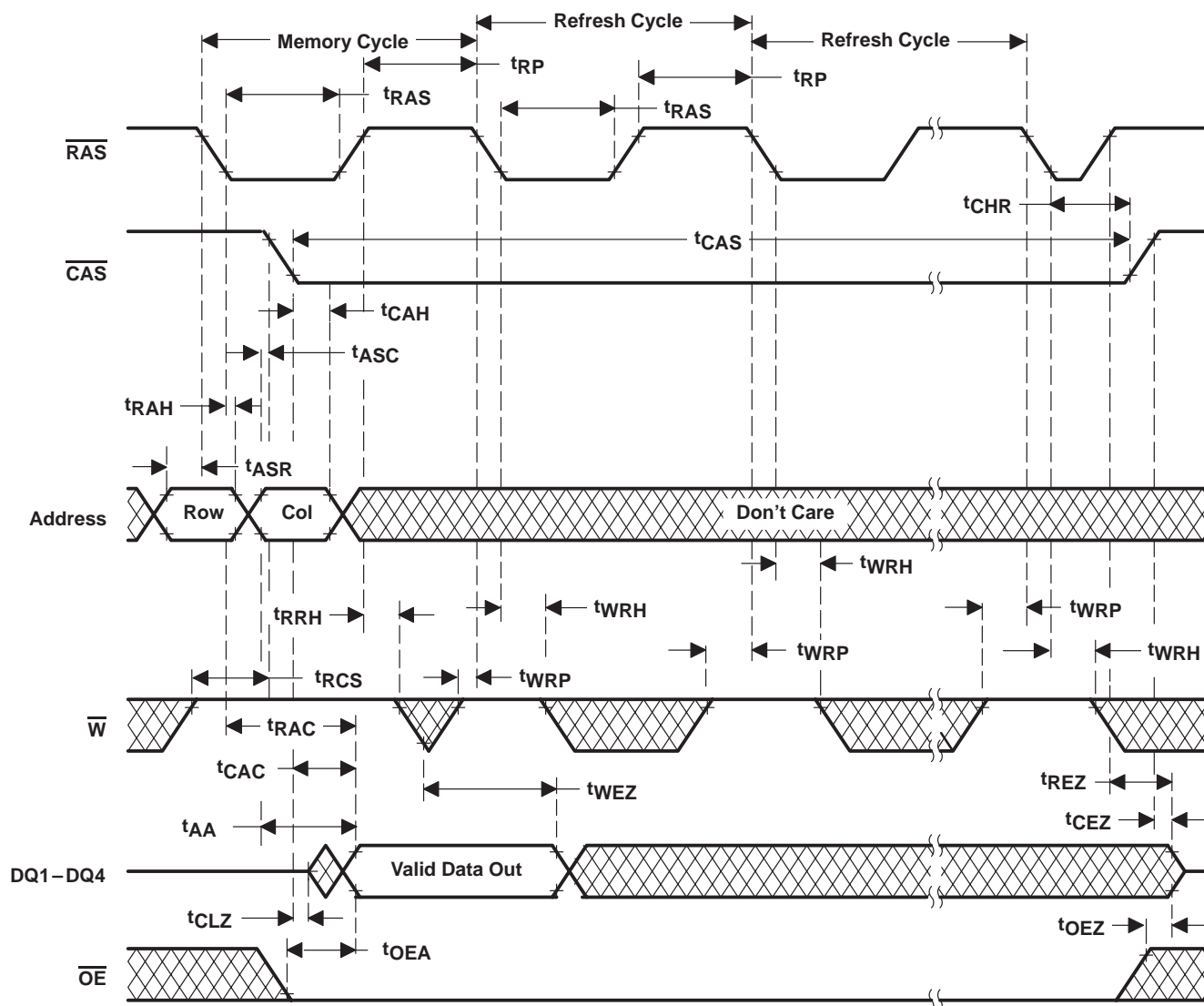


Figure 15. Hidden-Refresh-Cycle (Read) Timing

# PARAMETER MEASUREMENT INFORMATION

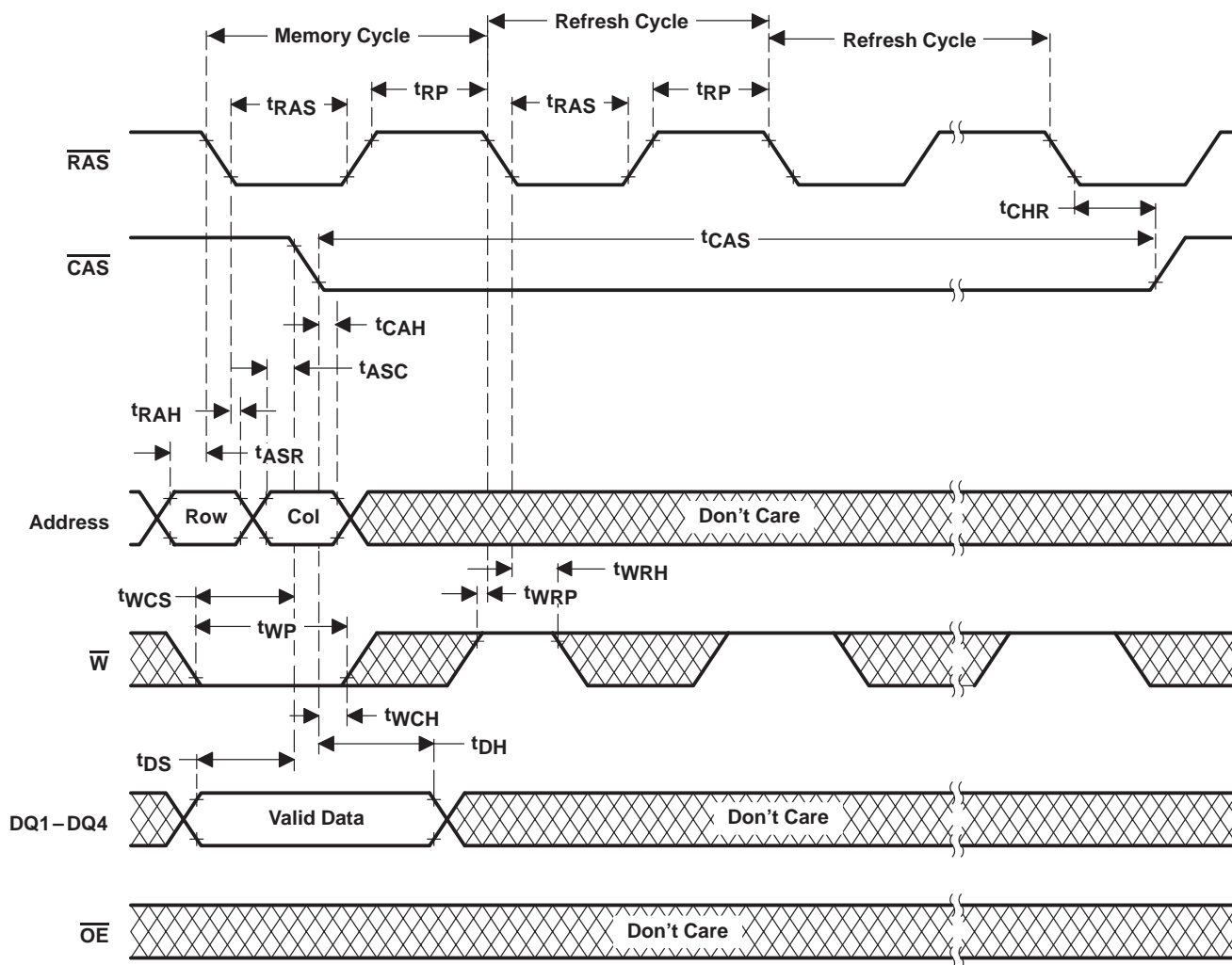


Figure 16. Hidden-Refresh-Cycle (Write) Timing

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PARAMETER MEASUREMENT INFORMATION

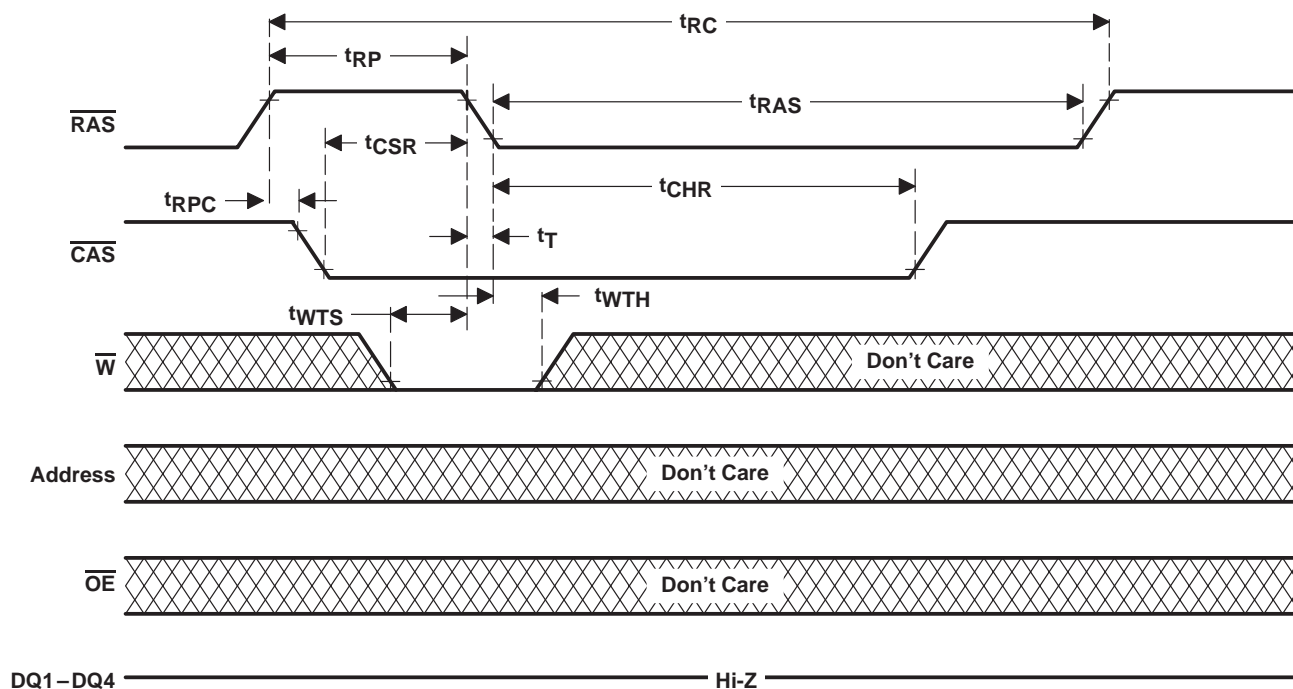


Figure 17. Test-Mode-Entry-Cycle Timing

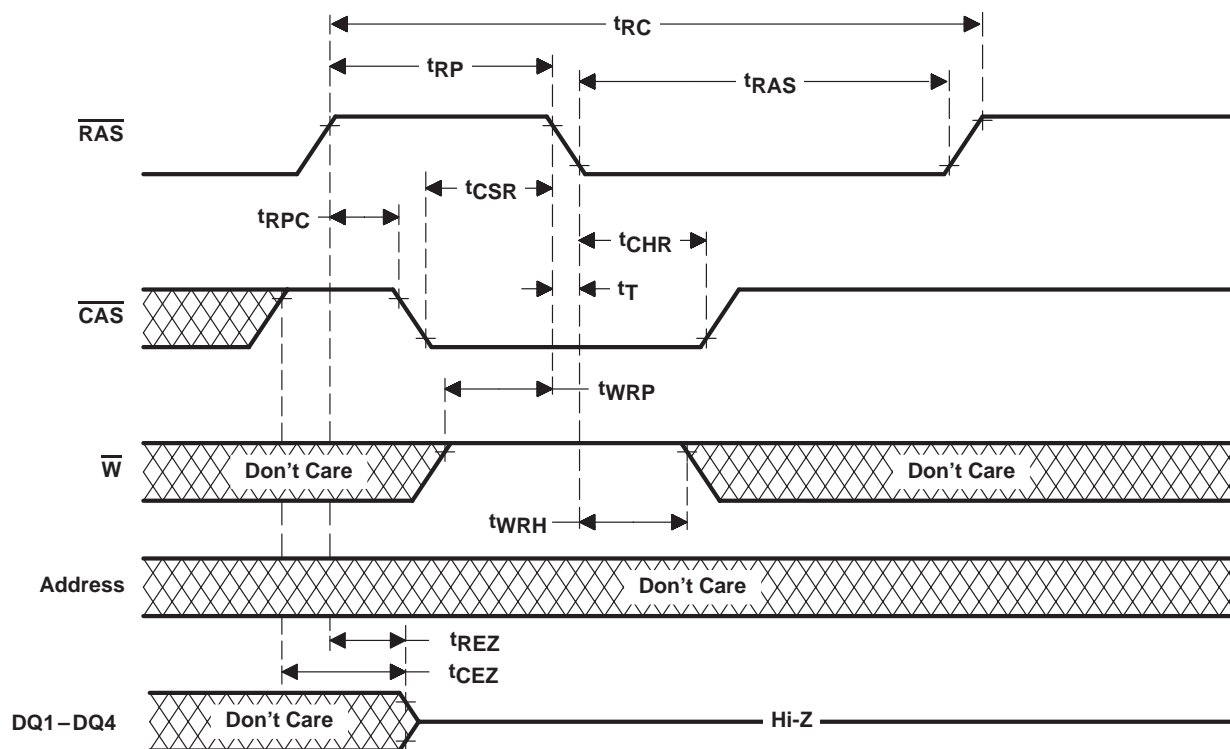


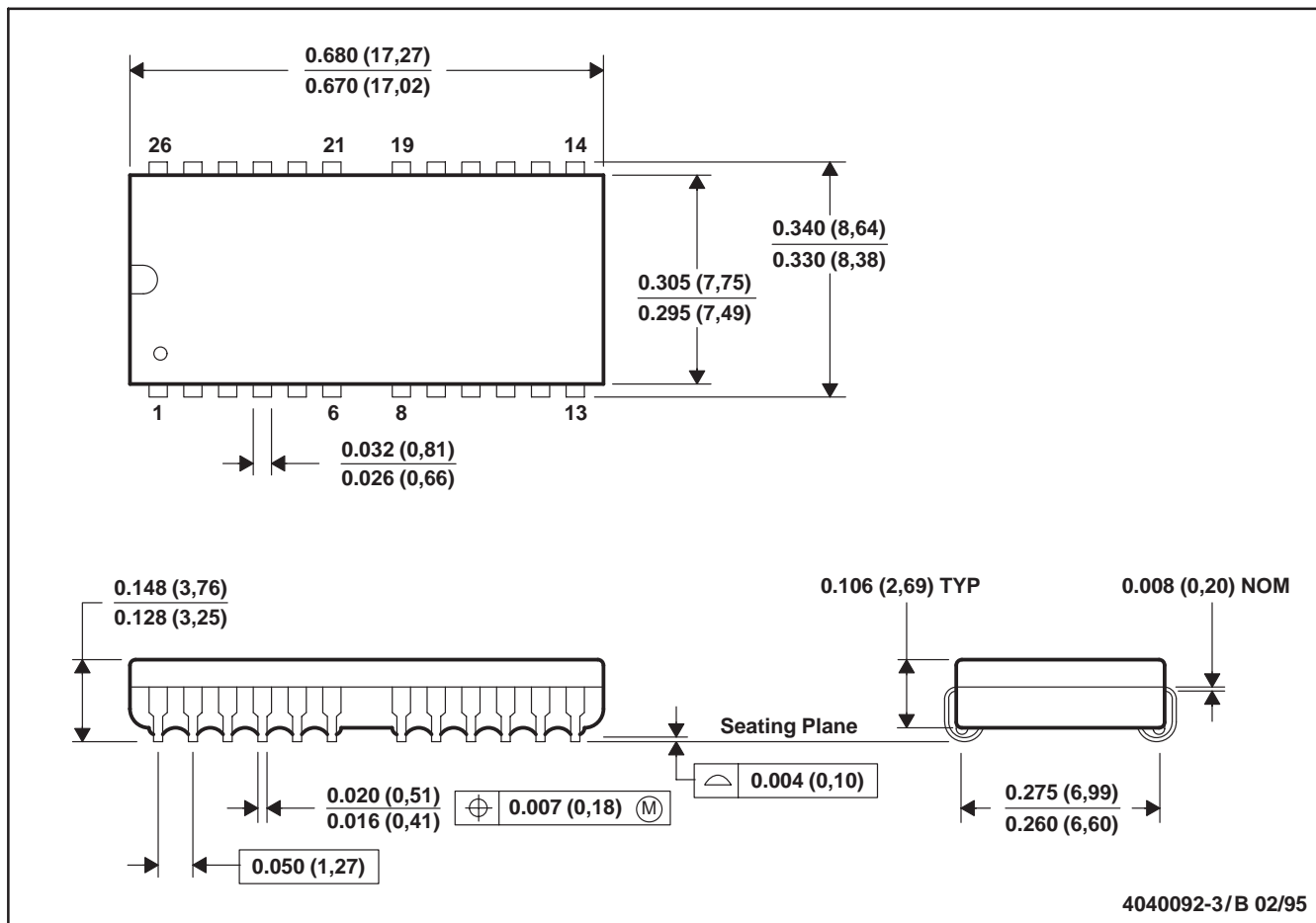
Figure 18. Test-Mode-Exit-Cycle CBR-Refresh-Cycle Timing



## MECHANICAL DATA

DJ (R-PDSO-J24/26)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

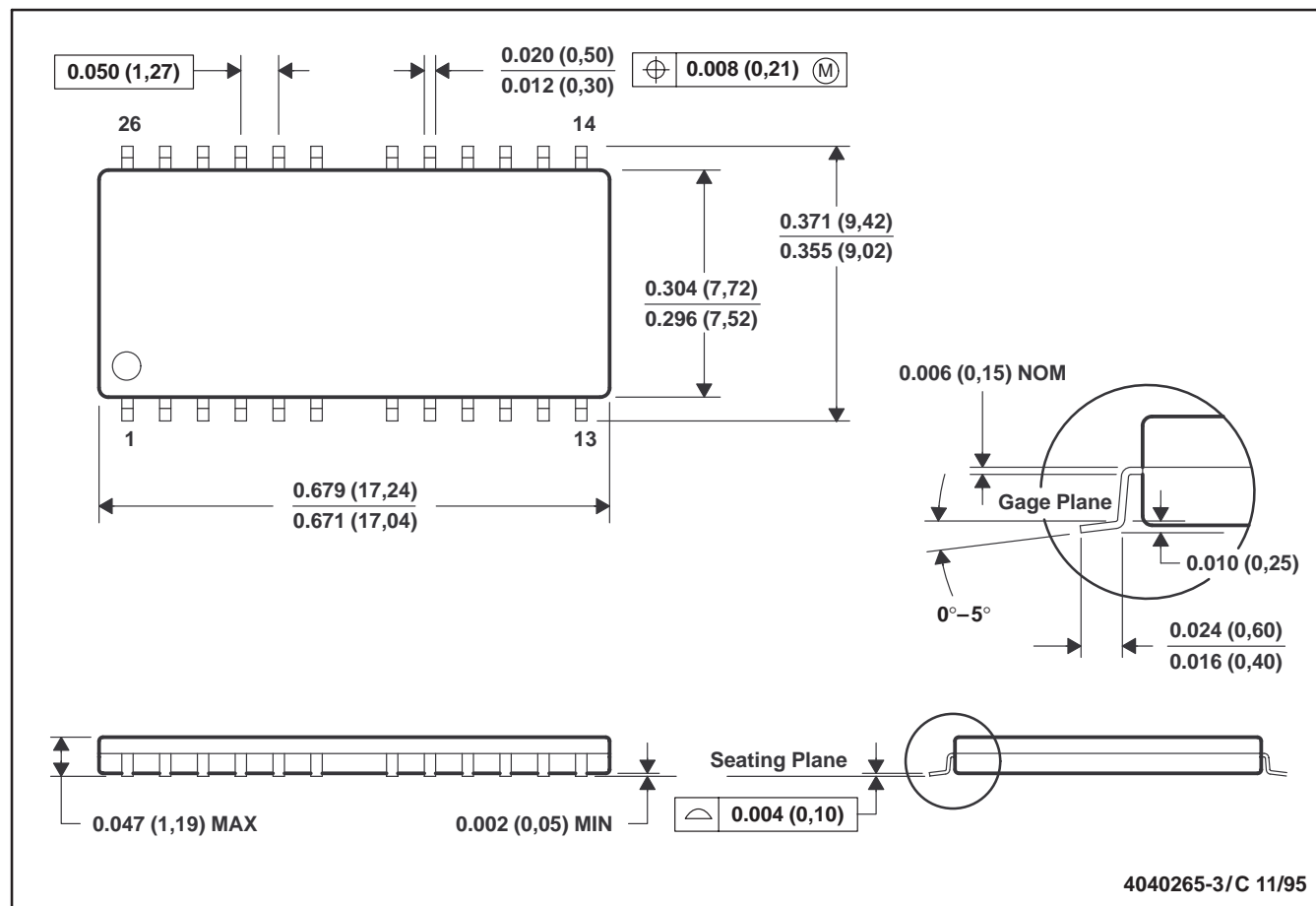
TMS416409A, TMS417409A, TMS426409A, TMS427409A  
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MECHANICAL DATA

DGA (R-PDSO-G24/26)

PLASTIC SMALL-OUTLINE PACKAGE

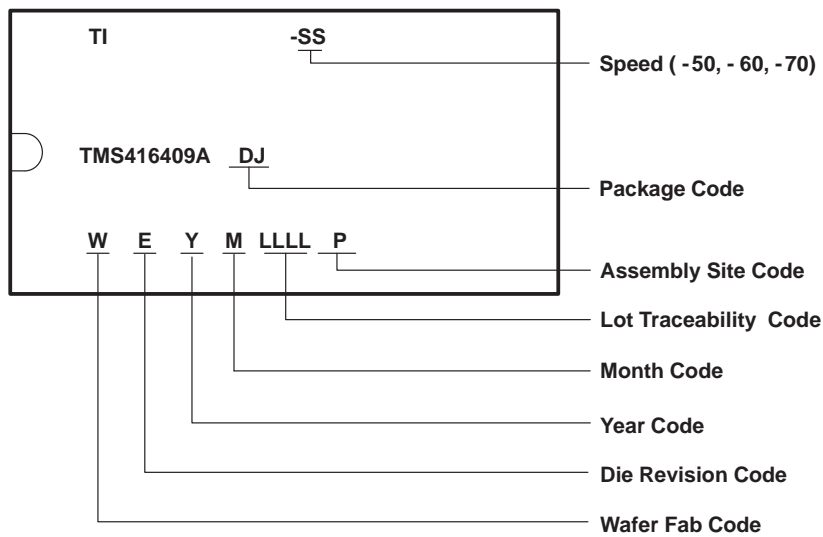


- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion.

TMS416409A, TMS417409A, TMS426409A, TMS427409A  
 4194304 BY 4-BIT EXTENDED DATA OUT  
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device symbolization (TMS416409A illustrated)



**TMS416409A, TMS417409A, TMS426409A, TMS427409A**  
**4194304 BY 4-BIT EXTENDED DATA OUT**  
**DYNAMIC RANDOM-ACCESS MEMORIES**

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