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OPBOX ver 2.2

USB Ultrasonic Testing Box with 2-channel T/R

Control Register Description

(Valid for devices with hardware revision: **Rev. 2.2.80**)

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Document version: 1v4

OPBOX-2.2 Description

Interface:

- USB 2.0 High Speed (480Mbps)
- Vendor ID: 0x0547
- Product ID:0x1003
- Device Version: 2.2 (0x0202)
- Bus powered (<500mA)
- Class: Vendor
- Endpoints:
  - Endpoint 0 (Control Registers): IN/OUT, 64-bytes max packet size
  - Endpoint 2 (TGC curve): OUT, Bulk, 512-bytes max packet size
  - Endpoint 6 (Sample buffer): IN, Bulk, 512-bytes max packet size

Acquisition mode:

- FIFO based Acquisitions mode (internal 256kB memory for Acquisitions) for real-time acquisitions;
- Frame organization – each Acquisition store Header and Sample Data in memory (Frame);
- Header store feature – contain useful Acquisition information such: absolute index, time-stamp, captured I/O, Peak Detectors results, captured Encoders positions etc.;
- Packet-based data read organization – improve data read throughput from device.

Firmware:

- devices with hardware firmware: **rev 2.2.80** or higher (from DEV_REV register)

Direct Orders description table

Vendor Request	Request Type	Value	Index	Length	Name	Description
0xD0	Dir: **IN** [0xC0]	0	0	2	**OPBOX_SN**	Device Serial Number Information Example: SN21.01
				Data[0]	SN_YEAR	0..255
				Data[1]	SN_NO	0..255
0xD1	Dir: **OUT** [0x40]	0	0	0	**RESET**	Global reset all device registers to default settings
0xD2	Dir: **OUT** [0x40]	0	0	0	**FIFO_RESET**	Reset FIFO controller and clear all stored Frames in memory
0xD3	Dir: **OUT** [0x40]	0	0	0	**DIRECT_SW_TRIG**	Direct measurement trigger from software Faster and simpler way to init measurement then via register access to "swTrigger" bit in MEASURE register (Addr: 0x20).
0xD4	Dir: **OUT** [0x40]	0	0	0		Reserved
0xD5	Dir: **IN** [0xC0]	0	0	1	**DIRECT_FRAME_READY**	Direct measurement status
				Data[0]		**0x00** – memory empty or contain less Frames than specified in PACKET_LENGTH register **0x01** – new Packet ready (specified number of Frame are stored in memory and ready to upload)
0xD6	Dir: **OUT** [0x40]	Pulse Ampl	0	1	**PULSE_AMPLITUDE**	Pulse Amplitude settings **0...63** Pulse Amplitude value Correspond to 0...360V pulse amplitude on PE output without load **Note!** Require initialization after reset.
0xD7	Dir: **IN** [0xC0]	0	0	1	**USB_MODE**	USB Speed Mode status
				Data[0]		0x00 – device enumerated in Full-Speed mode (12Mbps) Device need to be reattached to HS USB slot! 0x01 – device enumerated in High-Speed mode (480Mbps)

Control Registers description

Control Registers are accessible via two Vendor Requests to perform register write or read.
Register Write (USB control stage fields settings):

Vendor Request	0xE0
Request Type	0x40 – Dir: OUT
Value	0x00 – this field is not used in register write
Index	register Address (one of listed in tables below)
Length	2 – number of bytes to write

Register Read (USB control stage fields settings):

Vendor Request	0xE1
Request Type	0xC0 – Dir: IN
Value	0x00 – this field is not used in register read
Index	register Address (one of listed in tables below)
Length	2 – number of bytes to read

All Control Registers are 16-bit wide and therefore need to be addressed and accessed (read or write) in 16-bit form. This means Address fields (wIndex field in USB setup stage) must by set to values like: 0x00 0x02, 0x04, 0x06...

Control Register Table Legend:

RO	Read Only Access
WO	Write Only Access
R/W	Read or Write Access

Notation:
decimal – numbers without any prefix or noted as "Dec: ", for example: 1, 20, Dec: 1000
binary – numbers with "b" prefix, for example: b01, b010
hexadecimal – numbers with "0x" prefix, for example: 0x01, 0x2020

Control Registers description tables:

Address	Register Name [range]	Access	Range name	Description	Default value
0x00	**DEV_REV**			**Device Revision Information Register**	**0x2250**
	[7:0]	RO	Firmware Revision	0x50 (dec: 80) FPGA firmware Revision "x.x.80"	"2.2.80"
	[11:8]	RO	Hardware SubVer	0x2 (dec: 2) Hardware sub version "x.2.xx	
	[15:12]	RO	Hardware Version	0x2 (dec: 2) Hardware base version "2.x.xx"	
0x02	**POWER_CTRL**			**Power Supply Control Register**	**0x0000**
	[0]	R/W	Power Enable	Power supply for Analog and DC-DC control bit: 0 – off 1 - on	0
	[3:1]			Reserved	0
	[4]	RO	Power OK	Global power status bit 0 – NOK – power are switched off or fail 1 – OK – power is successfully switched on and stable	0
	[5]	RO	ANALOG PWR Status	Power supply status for Analog section 0 – NOK – input voltage from USB less then 4.4V 1 – OK.	0
	[6]	RO	DC12V Status	Power supply status for internal 12V DC-DC converter 0 – NOK – voltage lass than 11V 1 – OK	0
	[7]	RO	VREG Status	Pulse Amplitude voltage regulator status 0 – NOK – voltage >15% below setting 1 – OK	0
	[9:8]	RO		Reserved	0
	[15:10]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x04	**PACKET_LEN**			**Packet Length Register**	**0x0001**
	[12:0]	R/W	PacketLength	Number of Frames in Packet [1..4854] number of Frames in one Packet Note! Maximum number depends on DEPTH setting and “StoreDisable” option.	1
	[15:13]			Not used	0
0x06	**FRAME_IDX**			**Frame Index Register**	**0x0000**
	[15:0]	RO	FrameIdx	0...65535 – hardware-generated read-only Frame index Frame Index is incremented after each Acquisition and flip to 0x000 after reach 65535 value. Note! Frame Index is cleared after powering up the device and can be reset only with global RESET command (0xD1).	0
0x08	**FRAME_CNT**			**Frame Counter Register**	**0x0000**
	[12:0]	RO	FrameCnt	0..4854 – current number of Frames stored in memory	0
	[15:13]			Not used	0
0x0A	**CAPT_REG**			**Captured GPI and Trigger Overrun Source Register**	**0x0000**
	[0]	RO	TrgOvrSrc_A	Flag indicate lost trigger(s) which appear when Acquisition was in progress	0
	[1]	RO	TrgOvrSrc_H	Flag indicate lost trigger(s) due to Hold-Off time (100us) – trigger frequency higher then 10kHz	0
	[2]	RO	TrgOvrSrc_F	Flag indicate lost trigger(s) due to Acquisition memory Full condition	0
	[3]	RO	TrgOvrSrc_P	Flag indicate lost trigger(s) due to power fail (low input voltage, overload on pulser output, short circuits etc)	0
	[7:4]			Reserved	0
	[12:8]	RO	GPIcaptured	General Purpose Inputs (GPI[5:0]) captured on trigger	0
	[15:13]			Reserved	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x0C	**GP_INPUTS**			**General Purpose Inputs Register**	
	[5:0]	RO	GPI Status	INPUT STATUS (DB15 CONNECTOR) GPI0 – PIN11 GPI1 – PIN4 GPI2 – PIN12 GPI3 – PIN5 GPI4 – PIN15 GPI5 - PIN8	Input states
	[15:6]			Not used	0
0x0E	**GP_OUTPUTS**			**General Purpose Outputs Register**	**0x0100**
	[5:0]	R/W	GPO Settings Write access → Read access →	 Sets outputs pins to desire values (if enabled on [13:8] bits) Return outputs states Bit to DB15 connector cross-connections: bit[0] - GP00 (pin 1) – used as SYNC_OUT signal as default bit[1] - GP01 (pin 9) bit[2] - GP02 (pin 2) bit[3] - GP03 (pin 10) bit[4] - GP04 (pin 13) bit[5] - GP05 (pin 6)	0
	[7:6]			Not used	0
	[13:8]	R/W	GPO enable	Method of controlling of GPO line [5:0] respectively Bit = 0 – output is controlled via [5:0] bits in this register Bit = 1 – internal hardware control **Note**! GPO0 is internally used as SYNC_OUT signal for synchroniza-tion of external devices as default setting (bit[8]=1). Setting bit [8] to '0' will disable SYNC_OUT feature.	1
	[15:14]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x10	**TRIGGER**			**TRIGGER Control Register**	**0x0700**
	[3:0]	R/W	Trigger Source	Trigger source bits: b000 (0) trigger from software (via bit [6] - "Trigger Sw") b001 (1) trigger from external X pin (DB15 pin 11) b010 (2) trigger from external Y pin (DB15 pin 4) b011 (3) trigger from internal TIMER b100 (4) trigger from Encoder 1 (ENC1) b101 (5) trigger from Encoder 2 (ENC2) (6...15) not used	000
	[4]	R/W	Trigger Enable	Global Trigger enable bit 0 – trigger disabled (from any source) 1 – trigger enabled	0
	[5]	WO	Trigger Reset	Reset of measurement sequence and "New Data Ready" flag 0 – writing '0' has no effect 1 – reset current acquisition and/or discard stored data	0
	[6]	WO	Trigger Sw	Trigger initiated by software 0 – writing '0' has no effect 1 – start measurement (in "Trigger Sw" source mode)	0
	[7]			Not used	0
	[8]	R/W	XY Divider Enable	XY Divider counting enable bit 0 – divider disabled 1 – divider enabled (ready to counting)	1
	[9]	R/W	XY Divider Reset	XY Divider reset bit 0 – divider reset and disabled 1 – divider enabled	1
	[10]	R/W	Timer Enable	Internal Timer enable bit 0 – disabled 1 – enabled (source „b011" TIMER)	1
	[11]			Not used	0

	[12]	RO	Trigger Status	Trigger status bit 0 – waiting for trigger (idle) 1 – triggered (measurement in progress)	0
	[13]			Not used	0
	[14]	RO	Trigger Overrun Status	Trigger Overrun status bit 0 – no lost trigger from last Acquisition 1 – lost trigger(s) from last Acquisition (number of missing trigger in TRG_OVERRUN register)	0
	[15]			Not used	0
0x12	**TRG_OVERRUN**			**Trigger Overrun Counter Register**	**0x0000**
	[15:0]	RO	Trigger Overrun Counter	Counter of lost triggers between Acquisitions 0 – OK, no missed triggers 1..65535 – number of lost trigger(s) from last Acquisition	0
0x14	**XY_DIVIDER**			**Divider Register for trigger X and Y**	**0x0000**
	[15:0]	R/W	DividerXY TopValue Write access → Read access →	Settings for external trigger divider for X and Y trigger source 0..65535 – divide factor value for source X or Y 0..TopValue – read current divider counter value (if Trigger disabled or not active divider returns TopValue)	0
0x16	**TIMER**			**Internal Timer Register**	**0x2710**
	[15:0]	R/W	Timer Period	PRF (pulse repetition frequency) setting 100..65535 [us] – period setting for internal Timer (max 10kHz)	10000[us] (100Hz)
0x18	**TIMER_CAPT**			**Internal Timer Capture Register**	**0x0000**
	[15:0]	RO	Timer Capture	Content of TIMER register captured on trigger (can be used as Acquisition time-stamp)	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x1A	**ANALOG_CTRL**			**Analog Control Register**	**0x0000**
	[3:0]	R/W	Analog Filter	Analog filter settings: b0000 (0) 0.5 - 6 MHz b0001 (1) 1 - 6 MHz b0010 (2) 2 - 6 MHz b0011 (3) 4 - 6 MHz b0100 (4) 0.5 - 10 MHz b0101 (5) 1 - 10 MHz b0110 (6) 2 - 10 MHz b0111 (7) 4 - 10 MHz b1000 (8) 0.5 - 15 MHz b1001 (9) 1 - 15 MHz b1010 (10) 2 - 15 MHz b1011 (11) 4 - 15 MHz b1100 (12) 0.5 - 25 MHz b1101 (13) 1 - 25 MHz b1110 (14) 2 - 25 MHz b1111 (15) 4 - 25 MHz	0 0.5-6MHz
	[4]	R/W	Input Attenuator	Input Attenuator control bit: 0 – off (0dB) 1 – on (-20dB)	0
	[5]	R/W	Post Amplifier	Post Amplifier control bit: 0 – off (0dB) 1 – on (+24dB)	0
	[6]	R/W	Analog Input	Analog Source selection bit 0 – PE1 (Pulser/Receiver channel 1 – white BNC input) 1 – PE2 (Pulser/Receiver channel 2 – black BNC input)	0
	[15:7]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x1C	**PULSER_TIME**			**Pulser Control Register**	**0x001F**
	[5:0]	R/W	Pulse Time	Transducer charging time settings: 0...63 [x100ns] charging time value	0x1F (3.1us)
	[6]	R/W	Pulser Select	Active Pulser selection settings: 0 – pulser PE1 active (white BNC) 1 – pulser PE2 active (black BNC)	0
	[7]	R/W	Driver Enable	Pulser driver enable bit 0 – driver enabled 1 – driver disabled	0
	[15:8]			Not used	0
0x1E	**BURST**			**Burst Module Control Register**	**0x0004**
	[6:0]	R/W	Burst Period	Burst Outputs period setting 4..126 [x10 ns] – period time (increment of 2 – 4,6,8,10,12..)	4
	[7]			Not used	0
	[10:8]	R/W	Burst Length	Burst Length setting 0..7 [impulses] – number off burst impulses on outputs	0
	[15:11]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x20	**MEASURE**			**Measurement Control Register**	**0x0000**
	[3:0]	R/W	Sampling Freq	Sampling frequency settings: b0000 (0) 100MHz b0001 (1) 100MHz b0010 (2) 50.0MHz b0011 (3) 33.3MHz b0100 (4) 25.0MHz b0101 (5) 20.0MHz b0110 (6) 16.7MHz b0111 (7) 14.3MHz b1000 (8) 12.5MHz b1001 (9) 11.1MHz b1010 (10) 10.0MHz b1011 (11) 9.1MHz b1100 (12) 8.3MHz b1101 (13) 7.7MHz b1110 (14) 7.1MHz b1111 (15) 6.7MHz	0000
	[5:4]	R/W	Gain Mode	Gain mode settings: b00 – constant gain (register CONST_GAIN) b01 – TGC curve (gain from array / memory) b10 – not used b11 – not used	00
	[6]			Not used	0
	[7]	R/W	Data Processing Mode	Data processing mode settings: 0 – Raw data 1 – Absolute data	0
	[8]			Not used	0
	[9]	R/W	Store Disable	Store Disable mode settings:	0

				0 – normal mode (Header and sample data stored in memory) 1 - store disabled (sample data are **not** stored in memory, only Header)	
	[15:10]			Not used	0
0x22	**DELAY**			**Delay (post trigger) Control Register**	**0x0000**
	[15:0]	R/W	Delay	Post trigger time value 0...65535 [Ts] – number of sampling time periods	0
0x24	**DEPTH_L**			**Depth of Measurement Sample Buffer Register (Low Word)**	**0x003E8**
0x26	**DEPTH_H**			**Depth of Measurement Sample Buffer Register (High Word)**	
	[17:0]	R/W	Buffer Depth	1...262090 [samples] sample buffer depth **Note!** DEPTH_H[1:0] and DEPTH_L[15:0] registers are combined to one DEPTH [17:0] register for Sample Buffer Depth setting	0x03E8 Dec:1000
	[31:18]			Not used	0
0x28	**CONST_GAIN**			**Constants Gain Register (Require initialization after reset)**	**---**
	[7:0]	R/W	Constant Gain	Settings for constant gain during measurement 8...200 Gain DAC value with correspond to [-28...+68dB] gain DAC value formula: DAC = 2*(GAIN[dB] + 32)	
	[15:8]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x2A	**PEAKDET_CTRL**			**Peak Detectors Control Register**	**0x0000**
	[1:0]	R/W	PDA mode	PDA Level Comparator mode settings: b00 (0) – LEVEL mode (first sample above level is an event) b01 (1) – RISING edge mode (1 sample below and next sample above level is an event) b10 (2) – FALLING edge mode (1 sample above and next sample below level is an event) b11 (3) – TRANSITION mode (rising or falling sample crossing the level is an event)	0
	[2]	R/W	PDA enable	Peak Detector A enable bit 0 – PDA disabled 1 – PDA enabled	0
	[3]	RO	PDA result	Peak Detector A Comparator result bit 0 – comparator event not found in gate during last Acquisition 1 – comparator event found in gate during last Acquisition	0
	[4:5]	R/W	PDB mode	PDB Level Comparator mode settings: b00 (0) – LEVEL mode (first sample above level is an event) b01 (1) – RISING edge mode (1 sample below and next sample above level is an event) b10 (2) – FALLING edge mode (1 sample above and next sample below level is an event) b11 (3) – TRANSITION mode (rising or falling sample crossing the level is an event)	0
	[6]	R/W	PDB enable	Peak Detector B enable bit 0 – PDB disabled 1 – PDB enabled	0
	[7]	RO	PDB result	Peak Detector B Comparator result bit	0

				0 – comparator event not found in gate during last Acquisition 1 – comparator event found in gate during last Acquisition	
	[9:8]	R/W	PDC mode	PDC Level Comparator mode settings: b00 (0) – LEVEL mode (first sample above level is an event) b01 (1) – RISING edge mode (1 sample below and next sample above level is an event) b10 (2) – FALLING edge mode (1 sample above and next sample below level is an event) b11 (3) – TRANSITION mode (rising or falling sample crossing the level is an event)	0
	[10]	R/W	PDC enable	Peak Detector C enable bit 0 – PDC disabled 1 – PDC enabled	0
	[11]	RO	PDC result	Peak Detector C Comparator result bit 0 – comparator event not found in gate during last Acquisition 1 – comparator event found in gate during last Acquisition	0
	[15:12]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x2C	**PDA_START_L**			**Peak Detector A Start Register (Low Word)**	**0x0000**
0x2E	**PDA_START_H**			**Peak Detector A Start Register (High Word)**	**0x0000**
	[17:0]	R/W	PDA Start	Peak Detector A gate start value (combined registers) 0.. 262090 sample number which start the PDA gate time	0
	[31:18]			Not used	0
0x30	**PDA_STOP_L**			**Peak Detector A Stop Register (Low Word)**	**0x0000**
0x32	**PDA_STOP_H**			**Peak Detector A Stop Register (High Word)**	**0x0000**
	[17:0]	R/W	PDA Stop	Peak Detector A gate stop value (combined registers) 0.. 262090 sample number which end the PDA gate time	0
	[31:18]			Not used	0
0x34	**PDA_REF_VAL**			**Peak Detector A Reference Control Register**	**0x0000**
	[7:0]	R/W	PDA Reference Val	0..255 comparator reference level value	0
	[15:8]			Not used	0
0x36	**PDA_REF_POS_L**			**Peak Detector A Reference Position Register (Low Word)**	**0x0000**
0x38	**PDA_REF_POS_H**			**Peak Detector A Reference Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDA Reference Position	Peak Detector A Reference Position Register (combined) 0.. 262090 sample number where sampled signal crossed the PDA_REF_VAL value **Note!** Valid only when PDA result bit is '1'	0
	[31:18]			Not used	0
0x3A	**PDA_MAX_VAL**			**Peak Detector A Max Value Register**	**0x0000**
	[7:0]	RO	PDA Max Value	0..255 maximum value of sampled signal in PDA gate	
	[15:8]			Not used	
0x3C	**PDA_MAX_POS_L**			**Peak Detector A Max Position Register (Low Word)**	**0x0000**
0x3E	**PDA_MAX_POS_H**			**Peak Detector A Max Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDA Max Value Position	Peak Detector A Max Value Position Register (combined) 0..262090 sample number where sampled signal reached maximum value (PDA_MAX_VAL) in PDA gate	0
	[31:18]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x40	**PDB_START_L**			**Peak Detector B Start Register (Low Word)**	**0x0000**
0x42	**PDB_START_H**			**Peak Detector B Start Register (High Word)**	**0x0000**
	[17:0]	R/W	PDB Start	Peak Detector B gate start value (combined registers) 0..262090 sample number which start the PDB gate time	0
	[31:18]			Not used	0
0x44	**PDB_STOP_L**			**Peak Detector B Stop Register (Low Word)**	**0x0000**
0x46	**PDB_STOP_H**			**Peak Detector B Stop Register (High Word)**	**0x0000**
	[17:0]	R/W	PDB Stop	Peak Detector B gate stop value (combined registers) 0..262090 sample number which end the PDB gate time	0
	[31:18]			Not used	0
0x48	**PDB_REF_VAL**			**Peak Detector B Reference Control Register**	**0x0000**
	[7:0]	R/W	PDB Reference Val	0..255 comparator reference level value	0
	[15:8]			Not used	0
0x4A	**PDB_REF_POS_L**			**Peak Detector B Reference Position Register (Low Word)**	**0x0000**
0x4C	**PDB_REF_POS_H**			**Peak Detector B Reference Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDB Reference Position	Peak Detector B Reference Position Register (combined) 0..262090 sample number where sampled signal crossed the PDB_REF_VAL value **Note!** Valid only when PDB result bit is '1'	0
	[31:0]			Not used	0
0x4E	**PDB_MAX_VAL**			**Peak Detector B Max Value Register**	**0x0000**
	[7:0]	RO	PDB Max Value	0..255 maximum value of sampled signal in PDB gate	
	[15:8]			Not used	
0x50	**PDB_MAX_POS_L**			**Peak Detector B Max Position Register (Low Word)**	**0x0000**
0x52	**PDB_MAX_POS_H**			**Peak Detector B Max Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDB Max Value Position	Peak Detector B Max Value Position Register (combined) 0..262090 sample number where sampled signal reached maximum value (PDA_MAX_VAL) in PDB gate	0
	[31:18]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x54	**PDC_START_L**			**Peak Detector C Start Register (Low Word)**	**0x0000**
0x56	**PDC_START_H**			**Peak Detector C Start Register (High Word)**	**0x0000**
	[17:0]	R/W	PDC Start	Peak Detector C gate start value (combined registers) 0..262090 sample number which start the PDC gate time	0
	[31:18]			Not used	0
0x58	**PDC_STOP_L**			**Peak Detector C Stop Register (Low Word)**	**0x0000**
0x5A	**PDC_STOP_H**			**Peak Detector C Stop Register (High Word)**	**0x0000**
	[17:0]	R/W	PDC Stop	Peak Detector C gate stop value (combined registers) 0..262090 sample number which end the PDC gate time	0
	[31:18]			Not used	0
0x5C	**PDC_REF_VAL**			**Peak Detector C Reference Control Register**	**0x0000**
	[7:0]	R/W	PDC Reference Val	0..255 comparator reference level value	0
	[15:8]			Not used	0
0x5E	**PDC_REF_POS_L**			**Peak Detector C Reference Position Register (Low Word)**	**0x0000**
0x60	**PDC_REF_POS_H**			**Peak Detector C Reference Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDC Reference Position	Peak Detector C Reference Position Register (combined) 0..262090 sample number where sampled signal crossed the PDC_REF_VAL value **Note!** Valid only when PDC result bit is '1'	0
	[31:18]			Not used	0
0x62	**PDC_MAX_VAL**			**Peak Detector C Max Value Register**	**0x0000**
	[7:0]	RO	PDC Max Value	0..255 maximum value of sampled signal in PDC gate	
	[15:8]			Not used	
0x64	**PDC_MAX_POS_L**			**Peak Detector C Max Position Register (Low Word)**	**0x0000**
0x66	**PDC_MAX_POS_H**			**Peak Detector C Max Position Register (High Word)**	**0x0000**
	[17:0]	RO	PDC Max Value Position	Peak Detector C Max Value Position Register (combined) 0..262090 sample number where sampled signal reached maximum value (PDC_MAX_VAL) in PDC gate	0
	[31:18]			Not used	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x68	**ENC1_CTRL**			**Encoder 1 Control Register**	**0x0000**
	[0]	R/W	Encoder 1 Enable	Encoder Enable bit 0 – encoder disabled 1 – encoder enabled	0
	[1]	WO	Encoder 1 Reset	Encoder Reset bit 0 – writing '0' has no effect 1 – encoder in reset	0
	[2]	R/W	Encoder 1 Input Invert	Encoder Input Mode bit 0 – normal (if CHA lead CHB position is incremented) 1 – inverted (if CHA lead CHB position is decremented)	0
	[3]	R/W	Encoder 1 Index Input Enable	Encoder Index Input Enable bit 0 – IDX input is ignored 1 – high level on IDX input resets Position Counter	0
	[5:4]	R/W	Encoder 1 Decode Mode	Encoder Decode Mode settings: b00 (0)– 1X mode – decode only rising edges on CHA b01 (1) – 2X mode – decode rising and falling edges on CHA b10 (2) – 4X mode – decode both edges on CHA and CHB b11 (3) – not used	00
	[6]	R/W	Input Filter Enable	Digital Filter for Encoder Inputs (CHA, CHB, IDX) Enable bit 0 – digital filter disabled 1 – digital filter enabled for inputs CHA, CHB and IDX Digital filter length setting in Encoder Filter Length Register	0
	[7]	R/W	Encoder 1 Compare Enable	Encoder Position Comparator (position trigger generator) bit 0 comparator disabled 1 comparator enabled	0
	[15:8]	R/W	Encoder 1 Compare Step	Encoder Compare Step (position divider) settings 0..255 Number of steps in positive direction to generate position trigger Position Comparator generate triggers after each "Encoder	0x00

				Compare Step” number of steps. First trigger is always generated at current position. Next position trigger is automatically computed as: (Enc Position Counter + Enc Compare Step) **Example**: Writing value Dec: 10 to this register will cause generating position triggers at positions: 0, 10, 20, 30, 40...	
0x6A	**ENC1_POS_L**			**Encoder 1 Position Register (Low Word)**	**0x0000**
0x6C	**ENC1_POS_H**			**Encoder 1 Position Register (High Word)**	**0x0000**
	[31:0]	RO	Encoder 1 Position	Encoder 1 Position Register (combined) 0..4294967295 – current Encoder 1 position in 32-bit unsigned notation	0
0x6E	**ENC1_CAPT_L**			**Encoder 1 Capture Register (Low Word)**	**0x0000**
0x70	**ENC1_CAPT_H**			**Encoder 1 Capture Register (High Word)**	**0x0000**
	[31:0]	RO	Encoder 1 Capture	Encoder 1 Capture Register (combined) 0..4294967295 – Encoder 1 position captured at last measurement trigger (measurement position stamp)	0
0x72	**ENC1_FILTER**			**Digital Filter Length Register for Encoder 1 CHA, CHB and IDX inputs**	**0x0000**
	[15:0]	R/W	Encoder 1 Filter Length	0..65535 [x100ns] – numbers of 100ns filtering periods If input change it's state and state doesn't change during filtering time, input is assumed as stable and set to output. Any changes of input state during filtering time are discarded and it doesn't change output state of filtered input **Caution**! Filtering time must be properly considered, relative to the highest frequency of the encoder input signals.	0

Address	Register Name [range]	Access	Range name	Description	Default value
0x74	**ENC2_CTRL**			**Encoder 2 Control Register**	**0x0000**
	[0]	R/W	Encoder 2 Enable	Encoder 2 Enable bit 0 – encoder disabled 1 – encoder enabled	0
	[1]	WO	Encoder 2 Reset	Encoder 2 Reset bit 0 – writing '0' has no effect 1 – encoder in reset	0
	[2]	R/W	Encoder 2 Input Invert	Encoder 2 Input Mode bit 0 – normal (if CHA lead CHB position is incremented) 1 – inverted (if CHA lead CHB position is decremented)	0
	[3]	R/W	Encoder 2 Index Input Enable	Encoder 2 Index Input Enable bit 0 – IDX input is ignored 1 – high level on IDX input resets Position Counter	0
	[5:4]	R/W	Encoder 2 Decode Mode	Encoder 2 Decode Mode settings: b00 (0)– 1X mode – decode only rising edges on CHA b01 (1) – 2X mode – decode rising and falling edges on CHA b10 (2) – 4X mode – decode both edges on CHA and CHB b11 (3) – not used	00
	[6]	R/W	Input Filter Enable	Digital Filter for Encoder 2 Inputs (CHA, CHB, IDX) Enable bit 0 – digital filter disabled 1 – digital filter enabled for inputs CHA, CHB and IDX Digital filter length setting in Encoder Filter Length Register	0
	[7]	R/W	Encoder 2 Compare Enable	Encoder 2 Position Comparator (position trigger generator) bit 0 comparator disabled 1 comparator enabled	0
	[15:8]	R/W	Encoder 2 Compare Step	Encoder Compare Step (position divider) settings 0..255 Number of steps in positive direction to generate position trigger Position Comparator generate triggers after each "Encoder	0x00

				Compare Step" number of steps. First trigger is always generated at current position. Next position trigger is automatically computed as: (Enc Position Counter + Enc Compare Step) **Example**: Writing value Dec: 10 to this register will cause generating position triggers at positions: 0, 10, 20, 30, 40...	
0x76	**ENC2_POS_L**			**Encoder 2 Position Register (Low Word)**	**0x0000**
0x78	**ENC2_POS_H**			**Encoder 2 Position Register (High Word)**	**0x0000**
	[31:0]	RO	Encoder 2 Position	Encoder 2 Position Register (combined) 0..4294967295 – current Encoder 1 position in 32-bit unsigned notation	0
0x7A	**ENC2_CAPT_L**			**Encoder 2 Capture Register (Low Word)**	**0x0000**
0x7C	**ENC2_CAPT_H**			**Encoder 2 Capture Register (High Word)**	**0x0000**
	[31:0]	RO	Encoder 2 Capture	Encoder 2 Capture Register (combined) 0..4294967295 – Encoder 2 position captured at last measurement trigger (measurement position stamp)	0
0x7E	**ENC2_FILTER**			**Digital Filter Length Register for Encoder 2 CHA, CHB and IDX inputs**	**0x0000**
	[15:0]	R/W	Encoder 2 Filter Length	0..65535 [x100ns] – numbers of 100ns filtering periods If input change it's state and state doesn't change during filtering time, input is assumed as stable and set to output. Any changes of input state during filtering time are discarded and it doesn't change output state of filtered input **Caution**! Filtering time must be properly considered, relative to the highest frequency of the encoder input signals.	0