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# Chapter 1

## Attribution & Intent

This design is adapted from [a blog post by Henrik Forstén](#). A large portion of the design and schematics as well as parts of the description are his and should be thus credited. I've made a number of modifications to the schematic and attempted to thoroughly document the radar's operation in an effort to understand it. I hope that the description below will be useful to others who want to understand how a radar can be built from scratch but who, like me, are relatively new to electronics design.

# Chapter 2

## Physics

### 2.1 Range Calculation

The principle of operation of an FMCW radar is shown in Fig. 2.1. A sinusoidal signal that ramps in frequency is transmitted through air via an antenna. The reflected signal is picked up by another antenna and mixed with the original signal.

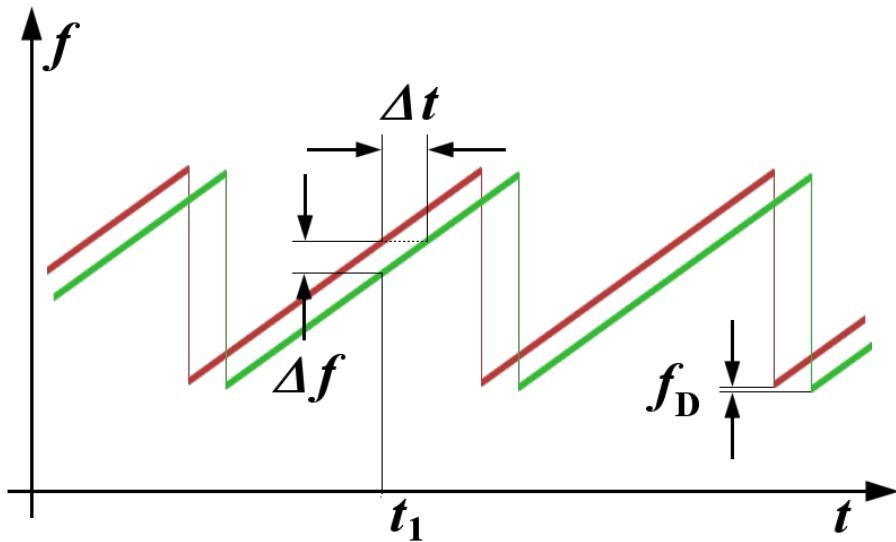


Figure 2.1: FMCW radar operation: a delayed signal is modulated with the original signal and the distance to the remote object can be backed out from the phase difference between the two signals.

Because the signal travels at the speed of light, the distance to the object can be computed using Eq. 2.1.

$$d = \frac{ct_d}{2} \quad (2.1)$$

$c$  is the speed of light,  $t_d$  is the time delay and the 2 is necessary because we are computing the round-trip time. By using the programmed frequency ramp rate we can express this equation in terms of the

frequency difference instead of the time delay<sup>1</sup>. This is shown in Eq. 2.2.

$$d = \frac{ct_{\text{ramp}}\Delta f}{2f_{\text{ramp}}} \quad (2.2)$$

Now we just need to figure out the frequency difference between the transmitted and received signals. The transmitted signal during one ramp is:

$$s_t(t) = T \sin(\omega_t(t)t) \quad T \text{ is the transmitted signal's amplitude.} \quad (2.3)$$

$$= T \sin(2\pi f(t)t) \quad (2.4)$$

$$= T \sin\left(2\pi t \left(f_0 + t \frac{f_{\text{ramp}}}{t_{\text{ramp}}}\right)\right) \quad (2.5)$$

The corresponding received signal is:

$$s_r(t - t_d) = R \sin(\omega_r(t - t_d)(t - t_d)) \quad (2.6)$$

$$= R \sin(2\pi(f(t - t_d) + f_D)(t - t_d)) \quad f_D \text{ is the Doppler shift.} \quad (2.7)$$

The mixer computes the product of these two signals:

$$m = s_t(t)s_r(t - t_d) \quad (2.8)$$

$$\approx TR \cos(\omega_t t - \omega_r t + \omega_r t_d) \quad ^2 \quad (2.9)$$

$$\approx TR \cos((\omega_t - \omega_r)t + \phi) \quad (2.10)$$

$\omega_r t_d = \phi$  is a phase term since it is not a function of  $t$  and therefore doesn't affect the frequency. So, we see that the mixer output is a signal whose frequency is equal to the difference frequency between the transmitted and received signals. We can use the Fourier transform to determine this frequency while ignoring the irrelevant coefficient terms and phase shift. The Fourier transform also makes it easy to separate different objects which will each show up as a separate frequency difference. The one complicating factor is that the received frequency encodes the Doppler shift in addition to the distance. So, what we actually measure is  $2\pi(\Delta f - f_D)$  instead of  $2\pi\Delta f$ . To correct for the Doppler shift we can take multiple measurements of the object to compute its speed<sup>3</sup> and then use the non-relativistic equation for the Doppler shift given by Eq. 2.11.

$$f_D = \frac{v_r}{c} f_0 \quad (2.11)$$

$v_r$  is the object's computed speed and  $f_0$  is the instantaneous ramp frequency. This must be added back in to the original result to get the true distance. However, because the speeds we're dealing with are sufficiently low, the Doppler contribution can be effectively ignored. For instance, the Doppler shift contribution to the distance measurement caused by a car on the highway travelling at 70mi/h is only 14cm. This consideration only really becomes important when using radar for military applications such as for high-speed aircraft or missile defense.

---

<sup>1</sup>It's acceptable to confine ourselves to a single ramp period for each object since the max distance we can detect with a 1ms ramp period is about 150km, well beyond the radar's other physical limits. We'll ignore the edge case where the transmitted and received signals bridge a ramp boundary.

<sup>2</sup>We've used the identity  $\sin \theta \sin \phi = [\cos(\theta - \phi) - \cos(\theta + \phi)]/2$  and the fact that the sum term is well outside the mixer output IF range (as well as the subsequent IF amplifier pass-band) and will therefore be filtered out.

<sup>3</sup>The fact that the individual distance calculations are inaccurate by the Doppler shift doesn't matter here since the speed will be constant on the order of the ADC sampling period and will therefore only produce a constant translation that is cancelled out when computing successive displacements.

## 2.2 Radar Equation

**Fixme Fatal:** There's a really good description of the radar equation derivation at [this link](#). It should be incorporated here to provide an intuitive understanding of this equation.

The maximum range detectable by a radar is given by the radar equation, Eq. 2.12.

$$R_{\max} = \sqrt[4]{\frac{P_t G^2 \lambda^2 \sigma}{P_{\min} (4\pi)^3}} \quad (2.12)$$

Variable	Description	Value
$P_t$	Transmitted power.	19.5dBm <sup>4</sup>
$G$	Antenna gain.	14dBi
$\lambda$	Wavelength.	5.4cm <sup>5</sup>
$\sigma$	Target cross section.	1m <sup>2</sup>
$P_{\min}$	Minimum detectable signal power.	-118dBm <sup>6</sup>

Plugging these values in, we find a maximum range of 357m. Using § 2.1 above, this corresponds to a maximum difference frequency of 1.4MHz.

In order to find the minimum range that avoids distortion, it's helpful to work backward from the maximum ADC differential input voltage of 2V. The IF amplifier that feeds this input has a gain of 23dB and employs an input filter with a gain of -10dBV through most of the passband. Collectively, this permits a mixer differential output voltage of up to 0.4V. As described on Henrik's blog, we can use the equation  $V = \sqrt{Z_{\text{load}} P}$  to translate this into a output power level. Since the mixer's differential output impedance is  $200\Omega$ , the maximum acceptable output power is -0.5dBm. It's power conversion gain at 5.5GHz is -3dB and the collective gain of the LNA and RF amplifier is 24dB, which sets the maximum input power at -21.5dBm. This corresponds to a distance of 1.4m and difference frequency of 5.5kHz. This input power is also below the IP1dB of the LNA and RF amplifier system of -16.5dBm.

### 2.2.1 Minimum Detectable Power

In order to determine the minimum detectable power, we must find the noise power and then the SNR that yields a readily detectable signal. Henrik's blog, as well as [this site](#) recommend using 20dB as the minimum SNR. To find the noise power, we find the thermal noise and then multiply it by the bandwidth for one FFT bin (Eq. 2.13). We then add the receiver noise figure.

$$P = k_B T B \quad (2.13)$$

$k_B$  is the Boltzmann constant,  $T$  is the temperature (we use 300K which is often used for room temperature) and  $B$  is the bandwidth of a single FFT bin in Hz. A single FFT bin bandwidth is given by Eq. 2.14.

$$B = \frac{f_s}{N} \quad N \text{ is the number of FFT samples.} \quad (2.14)$$

$$= \frac{f_s}{f_s t_{\text{ramp}}} \quad t_{\text{ramp}} \text{ is the ramp duration, or 1ms.} \quad (2.15)$$

$$= 1\text{kHz} \quad (2.16)$$

<sup>4</sup>26dBm adjusted for the 75% antenna efficiency.

<sup>5</sup>Using the center frequency, 5.6GHz.

<sup>6</sup>See § 2.2.1.

The last step is to determine the receiver noise figure. When two components are connected together, the equivalent noise factor is given by Eq. 2.17.

$$F_{NET} = F_1 + \frac{F_2 - 1}{G_1} \quad (2.17)$$

$F_1$  and  $F_2$  are the noise factors of each component and  $G_1$  is the gain of component 1. Noise figure is the decibel equivalent of noise factor (Eq. 2.18).

$$NF = 10 \log(F) \quad (2.18)$$

Eq. 2.17 shows why it's important to have an LNA with high gain: it reduces the noise contributions of later components. The only component whose noise figure is not listed on its datasheet is the **IF amplifier**. Henrik uses a guess of 10 – 20dB, which we will use here as well. TI has a [paper](#) on this which can be used if a more precise value is needed. The datasheet also presents information on calculating noise. We use the same 6dB value that Henrik uses. **Fixme Fatal: This really shouldn't just be estimated.**

Fixme Fatal!

Putting all these values together gives a minimum detectable power of  $-118\text{dBm}$ .

## 2.3 Angle Calculation

Fixme Fatal!

**Fixme Fatal:** Complete section.

# **Chapter 3**

## **Schematic**

## 3.1 Power

*schematic*

Fixme Fatal!

**Fixme Fatal:** I think this section needs information about PSRRs, especially for regulators that feed RF circuits.

Fixme Fatal!

**Fixme Fatal:** Another thing that needs clarification is where should the LDO's be placed? Should they be located near the loads they serve or the switching converters? My guess would be near the converters since that decreases the part of the board that is exposed to the switching noise.

### 3.1.1 Overview

A barrel jack is used to feed a 12V input to the board which is then administered to a 10V output linear regulator and two buck converters that output 5.6V and 3.6V. The buck converters in turn pass their voltages on to several LDO voltage regulators for input to the various digital ICs on the board. The benefit of chaining switching converters to linear regulators is greater energy efficiency and better noise suppression than can be achieved by using either alone. An LED indicates when power is administered to the board.

### 3.1.2 Barrel Jack / Power Input

A ferrite bead pi filter is placed at the output of the barrel jack connection. The ferrite bead is rated for 5.1A, which is more than double the absolute max current draw of the radar. The barrel connector is a switched jack, but we do not use a battery on this PCB so the 3rd pin is grounded.

### 3.1.3 TPS5420D Buck Converter

#### Description

The TPS5420D is an internally-compensated buck converter with a fixed switching frequency of 500kHz, whose block diagram is shown in Figure 3.1. The converter first compares the divided voltage output with a 1.221V reference and uses an error amplifier to amplify the difference. It then feeds that difference into a PWM comparator along with a sawtooth ramp waveform. If the PWM comparator outputs a high voltage the switch is turned off, effectively decreasing the duty cycle. Conversely, a low voltage saturates the transistor and increases the duty cycle. This has the effect of converging the output voltage to its set point. The TPS5420 has a ramp time of between 6.6 and 10ms.

#### Pinout

Fixme Fatal!

**Fixme Fatal:** I think pinout sections would be better placed in an appendix, with dual links from the component documentation to the pinout and from the pinout back to the documentation.

Fixme Fatal!

**Fixme Fatal:** What is the point of BOOT?

Table 3.1: TPS5420D pinout.

#	Pin	Description
1	BOOT	
2, 3	NC	No connect.
4	VSENSE	Feedback voltage for the regulator. This compares the divided output with a 1.221V reference.
5	ENA	Enable pin. This can be left floating to enable the device.

6	GND	Ground.
7	VIN	Input supply voltage.
8	PH	Output voltage.

---

## Component Selection

An inductor is chosen such that it satisfies the following 3 requirements:

1. The minimum inductance is given by Equation 3.1.
2. The current rating is at least 2x the maximum load current.
3. The self-resonant frequency is at least 10x the switching frequency.

$$L_{\min} = \frac{T}{2} \frac{V_{\text{out}}}{I_{\text{out}(\min)}} \left( 1 - \frac{V_{\text{out}}}{V_{\text{in}}} \right) \quad (3.1)$$

The requirements are given in Table 3.1.3. All of these requirements are satisfied by the [SRR1210A-330M](#) 33 $\mu$ H Bourns ferrite bead.

**Table 3.2: TPS5420D inductor requirements. I've assumed an input ripple of 300mV.**

Buck Vout	Lmin	Current Rating	SRF min
5.6V	6.5 $\mu$ H	2.21A	5MHz
3.6V	15.1 $\mu$ H	2.50A	5MHz

The input, output and boot capacitors were chosen by the [WEBENCH tool](#). The flyback diode was chosen to support 2A of current.

## Downstream Current Draw

It is important to know both the maximum and minimum current draw of components whose voltage inputs are fed by the output of a buck converter. The minimum current sets a lower bound on the inductance that can be used (see Equation 3.1) since the converter must remain in CCM for proper operation. It is also important to ensure that the buck converter and inductor are rated for the maximum current draw of downstream devices. Saturating the ferrite-core inductor can cause a loss in inductance.

**Table 3.3: The current draw of components downstream from the 5.6V buck converter. When minimum current draw is omitted from the datasheet I've assumed 0A.**

MFN	I <sub>Q</sub>	I <sub>max</sub>	Voltage Inputs
<a href="#">ADL5802</a>	170mA	300mA	5V
<a href="#">ADF4158</a>	312.5 $\mu$ A	5mA	5V (VP)
<a href="#">SE5004L</a>	300mA	800mA	5V (VCC1, VCC2, VCC3)
Total	470mA	1.105A	-

**Table 3.4: Components downstream from the 3.6V buck converter.**

MFN	I <sub>Q</sub>	I <sub>max</sub>	Voltage Inputs
<a href="#">KT2520K</a>	-	2mA	1.8V
<a href="#">NC7S04</a>	1 $\mu$ A	12.5mA	3.3V
<a href="#">NB3N551</a>	-	40mA	3.3V
<a href="#">XC7A15T-FTG256</a>	97mA	277mA	1V (VCCINT, VCCBRAM)
XC7A15T-FTG256	22mA	87mA	1.8V (VCCADC, VCCAUX)

<b>XC7A15T-FTG256</b>	1mA	201mA	3.3V (VCC0)
<b>W25Q32JV</b>	10 $\mu$ A	25mA	3.3V
<b>FT2232H</b>	510 $\mu$ A	280mA	3.3V (VPHY, VPLL, VCORE, VCCIO)
<b>93LC46B</b>	-	2mA	3.3V
<b>LTC2292</b>	5mA	95mA	3.3V (OVDD), 3V (VDD)
<b>ADA4940-2</b>	4.2mA	5.52mA	3.3V
<b>ADF4158</b>	-	32mA	3.3V (AVDD, DVDD)
<b>HMC431LP4</b>	19mA	27mA	3V
<b>TRF37A73</b>	250 $\mu$ A	130mA	3V
<b>SKY65404</b>	20mA	36mA	3V (VENABLE, VCC)
Total	169mA	1.252A	-

## PCB Layout

The datasheet provides a suggested PCB layout, shown in Figure 3.2.

### 3.1.4 TPS560200 Buck Converter

#### Description

The TPS560200 is an internally-compensated buck converter with a switching frequency of 600kHz and a fixed ramp time of 2ms. It is needed, rather than a linear regulator chained to a TPS5420D, because the FPGA requires its 1V power supply first.

#### Pinout

**Table 3.5: TPS50600 pinout.**

#	Pin	Description
1	EN	Enable pin. Can be floated to unconditionally enable device.
2	GND	Ground.
3	PH	Output voltage.
4	VIN	Input voltage.
5	VSENSE	Feedback, compared to a 0.8V reference.

#### Component Selection

The voltage divider resistors, filter capacitors and input capacitors are specified by the datasheet. The output voltage ripple must be sufficiently small that it falls within the required voltage range of the FPGA's V<sub>CCINT</sub> input. Specifically, it must be less than 100mV. Texas Instruments provides<sup>1</sup> an equation for the voltage ripple of a buck converter, given a small capacitor resistance. I'm further assuming an ESR of 0 since I'm using ceramic capacitors at the output and the current draw is fairly low. The equation is provided in Equation 3.2. The ripple current for a buck converter is given in Equation 3.3. Finally, the remaining inductor requirements are specified in Table 3.1.4. All of these requirements are satisfied by a 10 $\mu$ H inductor, which is used in the datasheet.

$$V_{P2P} = \frac{I_{P2P}}{8CF_{SW}} \quad (3.2)$$

<sup>1</sup>[www.ti.com/lit/an/slva630a/slva630a.pdf](http://www.ti.com/lit/an/slva630a/slva630a.pdf)

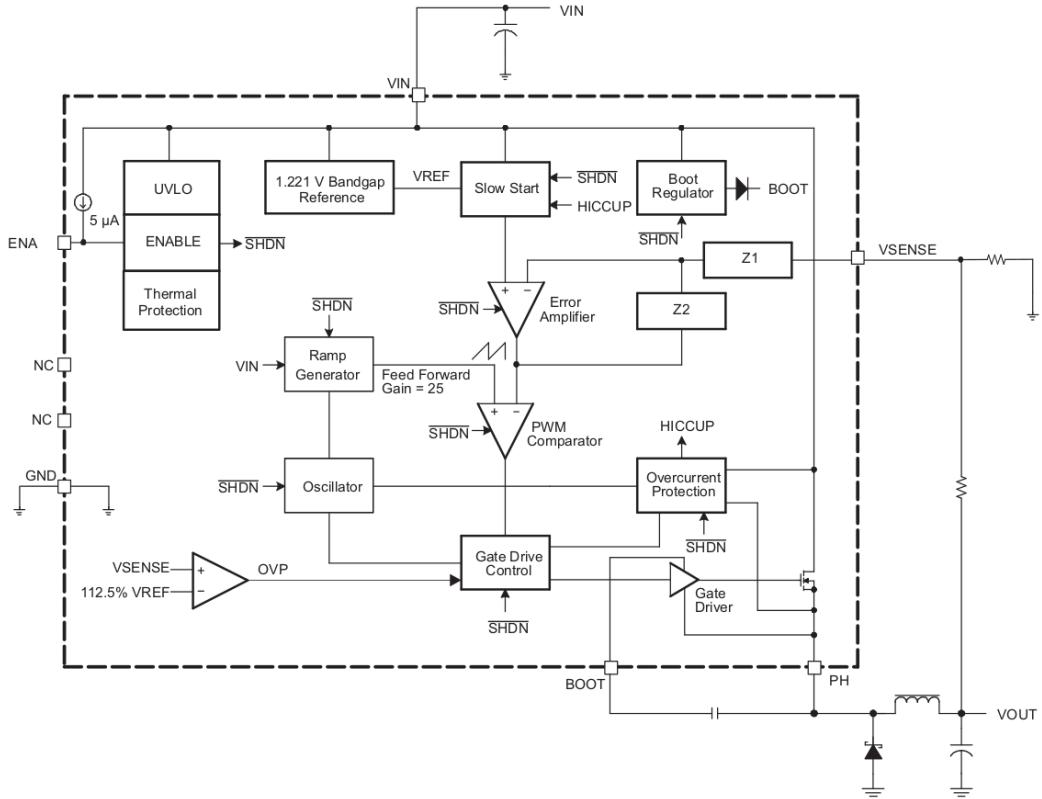


Figure 3.1: TPS5420D Block Diagram

$$I_{P2P} = V_{out} \frac{1 - D}{LF_{SW}} \quad (3.3)$$

Table 3.6: TPS560200 inductor requirements.

V <sub>out</sub>	L <sub>min</sub>	Current Rating	SRF <sub>min</sub>
1V	7.9μH	554mA	6MHz

### Downstream Current Draw

Table 3.7: Components downstream from the TPS560200 buck converter.

MFN	I <sub>Q</sub>	I <sub>max</sub>	Voltage Inputs
XC7A15T-FTG256	97mA	277mA	1V (VCCINT, VCCBRAM)

### PCB Layout Guidelines

The datasheet provides a recommended layout, shown in Figure 3.3.

### 3.1.5 LP2985A-10DBVR Linear Regulator

#### Description

The LP2985A is a low-dropout fixed-output regulator with a max output current of 150mA. Its functional block diagram is shown in Figure 3.4. It uses an op-amp to compare the voltage-divided output with a 1.23V reference. It then turns a PNP transistor on/off depending on the output voltage level relative to its 10V target.

#### Pinout

Table 3.8: LP2985A's pin descriptions.

#	Pin	Description
1	VIN	Voltage supply.
2	GND	Ground

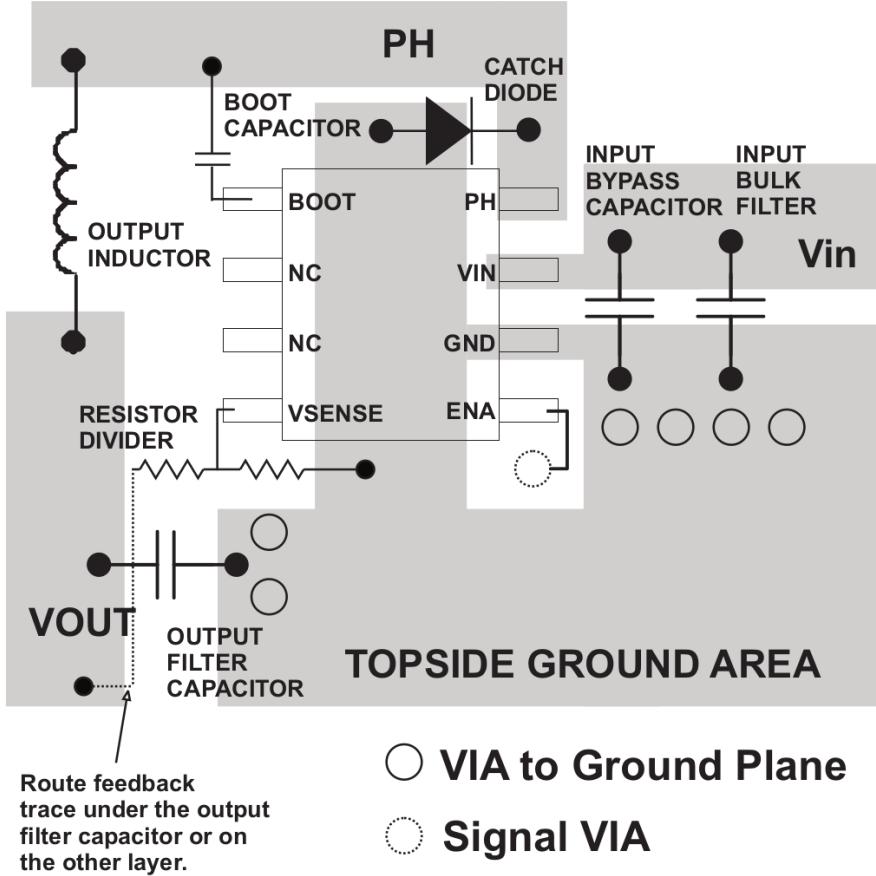


Figure 3.2: TPS5420D suggested PCB layout.

## PCB Layout

The input and output capacitors should be placed within 1cm of the input and output pins and have a low-impedance path to ground.

### 3.1.6 TPS7A91 LDO Voltage Regulator

#### Description

The TPS7A91 is a low-noise, low-dropout and adjustable voltage regulator. It has an RMS output noise of  $4.7\mu\text{V}$ . The regulator works by comparing the feedback voltage, at the inverting input of an error amplifier, with a 0.8V reference voltage at the non-inverting input. The output of the error amplifier is connected to the gate of an n-channel MOSFET whose drain is attached to the input voltage and whose source is attached to the output voltage. This negative feedback creates a stable equilibrium when the output voltage is at its set-point. The functional block diagram is shown in Figure 3.5.

The power-good function of one regulator is used to ensure that the 1.8V supply arrives at the FPGA before the 3.3V supply. The circuit uses an open-drain output with a pull-up resistor. If the output voltage goes below some threshold, the MOSFET will saturate and the PG line will be brought low. Otherwise, it will be pulled high.

#### Pinout

Table 3.10: TPS7A91 pinout.

#	Pin	Description
1, 2	OUT	Regulated output voltage. A $10\mu\text{F}$ or greater capacitor should be connected between this pin and ground.
3	FB	Feedback pin. The divided output voltage is compared against a 0.8V reference.
4	GND	Ground.
5	PG	A power good indicator that can signal to downstream devices when voltage is within some range of the desired level. The design doesn't use this and so the pin has been left floating.
6	SS_CTRL	Soft-start control pin. Tying this pin to the input voltage increases the soft-start charging current to $100\mu\text{A}$ , which reduces the startup time. This pin could have also been tied to ground if a slower startup time was desired.
7	EN	Enable. Tying this to the input voltage unconditionally enables this device.
8	NR/SS	Noise-reduction pin. A capacitor can be placed between this pin and ground to reduce output noise. This effectively acts like an RC filter. A capacitance between $10\text{nF}$ and $1\mu\text{F}$ is recommended. I've used $100\text{nF}$ . This pin also limits inrush current.
9, 10	IN	Input voltage pin. A bypass capacitor of $10\mu\text{F}$ or more is required.

## Component Selection

MLCC capacitors are recommended for input and output bypassing due to their low ESR, with preferences given to X5R and X7R types. Additionally, they should be derated by at least 50%. The recommended capacitance is  $10\mu\text{F}$  or greater at the input and output. I've used  $10\mu\text{F}$  at the input and the same at the output, with the option for another capacitor at the output if needed. The  $10\text{nF}$  feed-forward capacitor between FB and OUT is recommended by the datasheet to improve noise and PSRR performance. The voltage divider resistors are specifically mentioned in the datasheet to get the appropriate output values.

## PCB Layout

The recommended PCB layout is shown in Figure 3.6.

### 3.1.7 TPS7A7001DDA LDO Regulator

#### Description

The TPS7A7001DDA supports low dropouts up to 2A, which is important since it must accommodate a maximum current draw of 1.1A (see Table 3.1.3).

#### Pinout

Table 3.11: TPS7A7001DDA pinout.

#	Pin	Description
1, 4, 5	NC	No connect.
2	EN	Enable input. Connected to IN since unused.
3	IN	Input voltage.
6	OUT	Regulated voltage output.
7	FB	Feedback, compared to 0.5V reference.
8	GND	Ground.
9	EP	Exposed pad. Tied to ground.

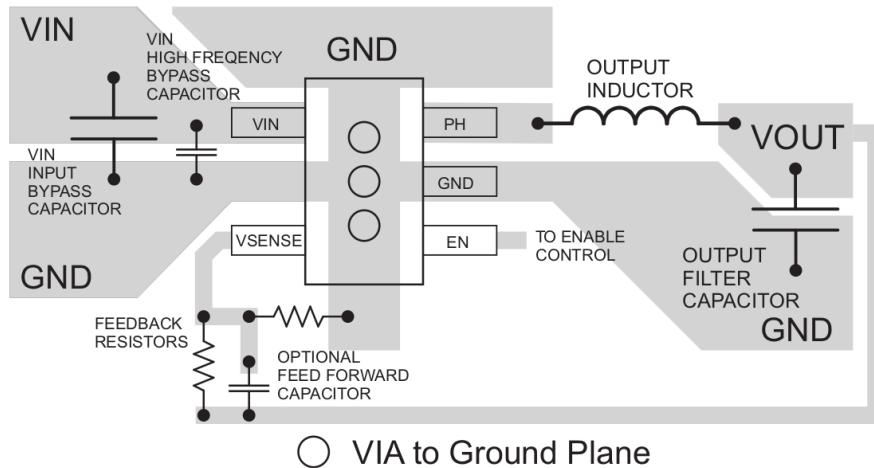


Figure 3.3: TPS560200 recommended PCB layout.

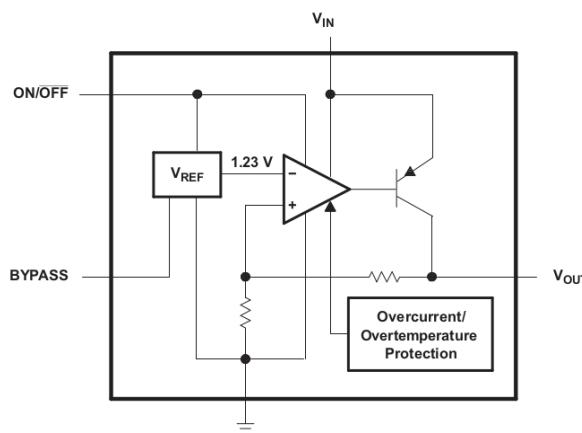


Figure 3.4: The LP2985A-10DBVR LDO regulator block diagram.

### Component Selection

An input capacitor of  $1 - 10\mu\text{F}$  and with low ESR is recommended. The output capacitor should be ceramic and can be anywhere from  $4.7 - 47\mu\text{F}$ . I've chosen  $10\mu\text{F}$  with the option for an additional capacitor if needed. The voltage divider resistors are specifically recommended by the datasheet.

### PCB Layout

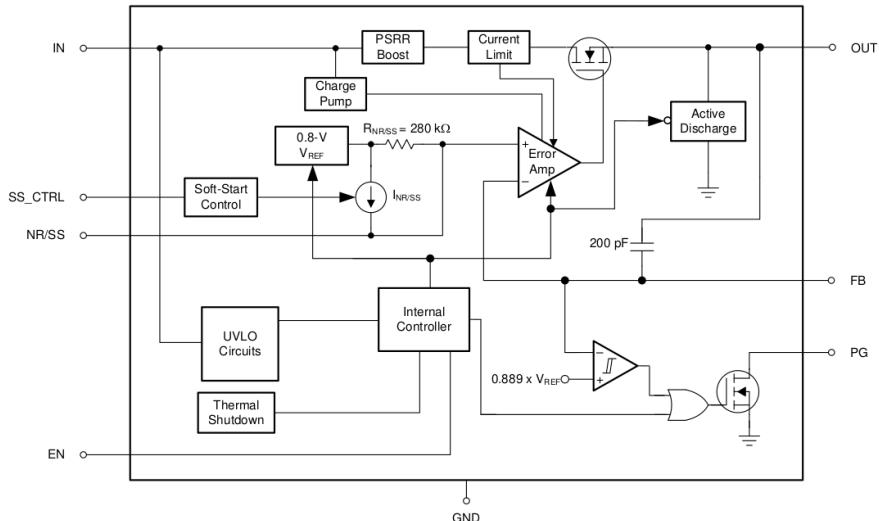
The recommended PCB layout is provided in [3.7](#).

### 3.1.8 LP5907MFX-3.0

#### Description

The LP5907MFX-3.0 is a low-noise and dropout voltage regulator used to power the VCO and reception-side amplifiers. It has a current rating of 250mA which is more than the maximum current load of the downstream components.

#### Pinout



**Figure 3.5:** TP7A91 block diagram.

**Table 3.12: LP5907MFX-3.0 pinout.**

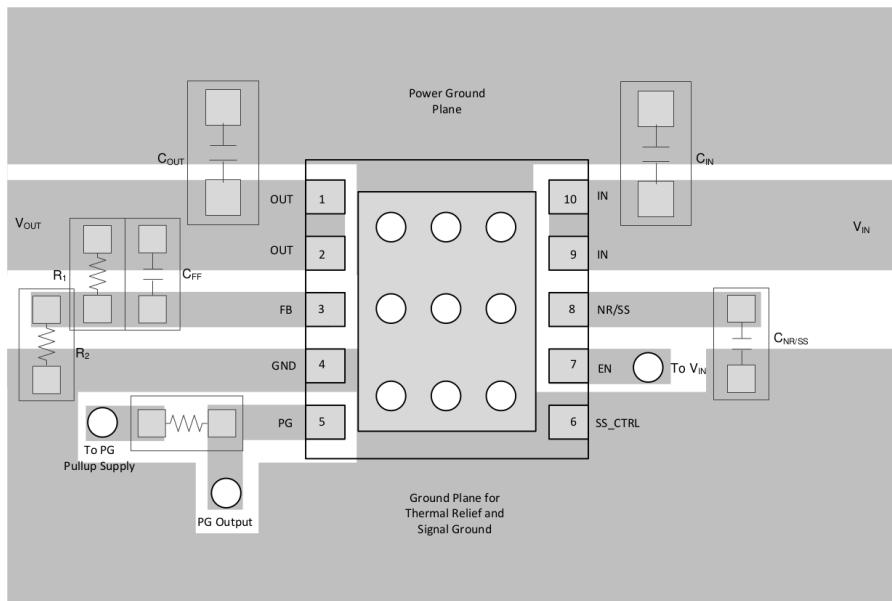
#	Pin	Description
1	IN	Voltage input.
2	GND	Ground.
3	EN	Enable. Tied to IN to keep the device unconditionally on.
4	NC	No connect.
5	OUT	1.8V output.

### Component Selection

The input and output capacitors should be  $1 - 10\mu\text{F}$ , with the input capacitor at least as large as the output capacitor. I've used  $10\mu\text{F}$  capacitors in this design.

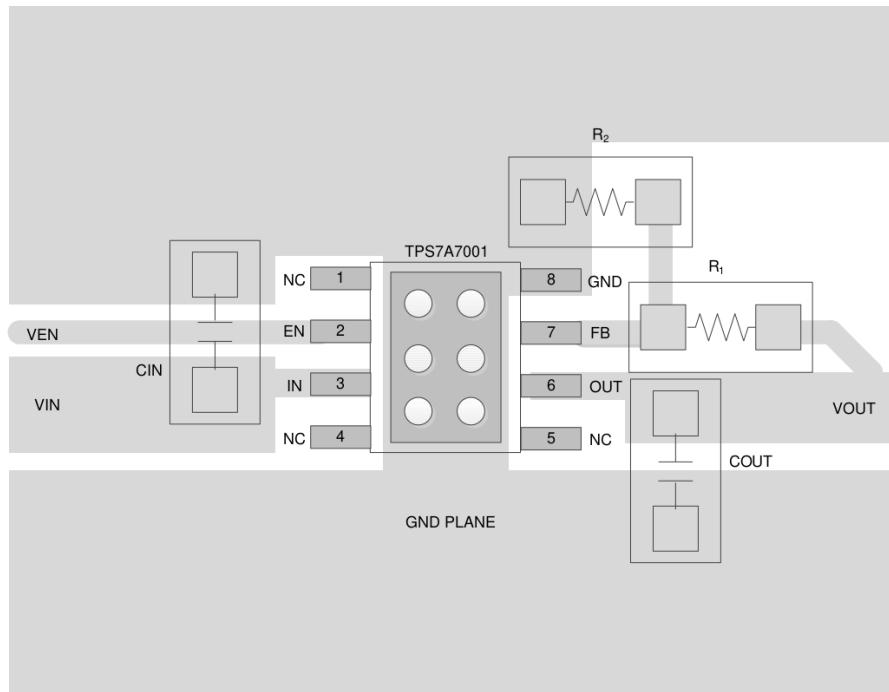
### PCB Layout

The recommended PCB layout is shown in Figure 3.8.



○ Denotes vias used for application purposes

**Figure 3.6:** TPS7A91 recommended PCB layout.



**Figure 3.7:** TPS7A7001DDA recommended PCB layout.

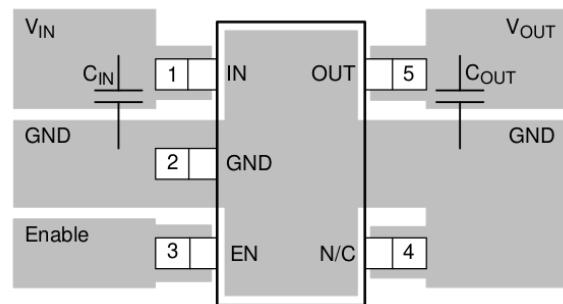


Figure 3.8: LP5907MFX-3.0 recommended PCB layout.

## 3.2 Top

*schematic*

### 3.2.1 Overview

The top-level schematic has two purposes: it instantiates the various submodules in the design and generates a 40MHz clock signal that is distributed to the [FPGA](#), [ADC](#) and [frequency synthesizer](#).

The [crystal oscillator](#) has its own 1.8V power supply and the [inverter](#) and [clock buffer](#) share their own 3.3V power supply. The LDO used is a very low noise LP5907. However, the PSRR of the LDO at the switching frequency of the [buck converter that feeds it](#) is greatly diminished from its lower frequency value (80dB at 1kHz and only about 40dB at 500kHz). So, ferrite bead pi filters are used at the LDO outputs to provide further noise suppression for higher frequencies. They also prevent noise generated by the clocks from reentering the power supply and affecting other devices.

### 3.2.2 KT2520K 40MHz TXCO

#### Description

The KT2520K crystal oscillator outputs a 40MHz clipped sine wave. It requires a DC-blocking capacitor  $\geq 1\text{nF}$  at the output since one is not included internally. I've used 100nF which is recommended by the [ADC](#) datasheet.

### 3.2.3 NC7SVU04 Inverter

#### Description

The NC7SVU04 is a high-speed logic inverter used to convert its clipped sine-wave input into a square wave output. It has a typical propagation delay of 1.5ns.

#### Component Selection

The inverter configuration is specified by the [ADC](#) datasheet. The voltage divider sets the DC bias point at  $V_{CC}/2$ , which in turn sets the duty cycle to 50%. The coupling capacitor is required because the crystal oscillator has low operational voltage and it allows the divider to set the DC bias point.

#### PCB Layout

The oscillator, inverter and buffer should be placed adjacent to the ADC, which is very susceptible to noise from clock jitter.

### 3.2.4 NB3N551 1:4 Clock Buffer

#### Description

The NB3N551 clock buffer duplicates the square wave input clock signal into 3 identical clock outputs that are fed to the [FPGA](#), [ADC](#) and [frequency synthesizer](#).

## **Component Selection**

A  $33\Omega$  source terminating resistor is used for the **FPGA** and **frequency synthesizer** clock lines because the traces leading to their clock pins are longer than 1 inch. This prevents noise from the FPGA and frequency synthesizer from affecting the clock fan-out. The source terminating resistor is not used for the ADC line because it is assumed that the fan-out buffer is immediately adjacent to the ADC. However, if the clock is placed farther away, the  $33\Omega$  must be used on this line as well.

## 3.3 FPGA

### 3.3.1 Overview

The FPGA has two main roles. It performs digital signal processing on data sent from the ADC and relays the processed data back to a host computer via an FT2232H which acts as a FIFO-USB interface. Secondly, the FPGA is used to configure and control other components on the board. In order to program the FPGA, we use a host computer with a JTAG interface via the FT2232H.

The FPGA stores and loads its configuration to/from an SPI flash memory device, W25Q32JV.

### 3.3.2 XC7A15T-FTG256 Xilinx FPGA

#### Description

#### Linked Sections

*pinout*

#### Documents

**Table 3.13: Important documents.**

URL	Description
<a href="#">Artix-7 FPGA family</a>	The main page that contains a collection of documents about the 7 series devices.
<a href="#">Package Pinout</a>	The various packages that the device comes in, along with the associated pin definitions.
<a href="#">Overview</a>	Contains general device capability information, such as number of logic cells, DSP blocks, etc.
<a href="#">PCB Design Guide</a>	Contains information about bypassing and other design considerations.
<a href="#">XADC</a>	Contains information about the FPGA's internal ADC.
<a href="#">Configuration Guide</a>	Describes how to configure the FPGA with a bitstream.

#### Power Supply Requirements

The FPGA requires that the VCCINT and VCCBRAM voltages be supplied first, followed by VCCAUX and then by VCCO. Additionally, all this must be done between 0.2 and 50ms. The required voltage levels are displayed in Table 3.3.2.

**Table 3.14: XC7A15T-FTG256 power supply requirements.**

Voltage Pin	Min	Typ	Max
V <sub>CCINT</sub>	0.95	1.00	1.05
V <sub>CCBRAM</sub>	0.95	1.00	1.05
V <sub>CCHAUX</sub>	1.71	1.80	1.89
V <sub>CCO</sub>	1.14	-	3.465

#### Bypassing

The PCB Design Guide above specifies fairly stringent requirements for bypassing and should be adhered to.

## PCB Layout

### 3.3.3 W25Q32JV Flash Memory

The CCLK\_0 pin is exported from the FPGA to the flash device to drive its operation and coordinates writes and reads to and from the device. DO is used by the FPGA to perform SPI reads from the flash memory device. It is connected to J14 of the FPGA. DI is connected to J13 of the FPGA and is used by the FPGA to send data to the flash memory device. CS is active low and is used by the FPGA to signal data transmission is about to occur. It is connected to L12 on the FPGA. WP (write protect) and HOLD are both active low pins and are used to prevent the status configuration registers from being written to and can pause the device when multiple devices share the same SPI signal, respectively. They are unused and thus connected to the 3.3V power supply. The device is powered with 3.3V (it supports a range of 2.7V to 3.6V). Table A.4 contains a list of all FPGA pins and their connections.

## 3.4 USB

In order to configure the FPGA we load the configuration bit stream onto the board using a USB cable and USB micro receptor on the PCB. The signal is then passed along to an [FT2232H](#) IC that translates the USB signal into JTAG data which it sends to the FPGA using the TCK, TDI, TDO and TMS pins. The schematic for this is shown in Figure 3.9. The FT2232H IC requires several power inputs: 3 VCORE input pins that require a 1.8V input voltage (this comes from VREGOUT, which is a pin that outputs a 1.8V signal from an internal voltage regulator), 1 3.3V VREGIN input (which serves as the input pin to drive the 1.8V regulated output), 4 3.3V VCCIO input pins, and 23.3V inputs (VPLL and VPHY) that are filtered with an LC filter.

OSCI and OSCO are the oscillator input and output, respectively. These must be connected to a 12MHz oscillator with a frequency tolerance less than 30ppm (ours is 10ppm). REF is a current reference that must be connected to a  $12k\Omega$  resistor to ground. DM and DP are the USB data signal minus and plus lines, respectively. TEST should be connected to ground. RESET# (the # indicates an active low pin) is connected to a pull-up resistor to 3.3V so the reset is deasserted whenever the input voltage is at a sufficiently high and stable level. PWREN# is an output that is 0 during normal operation. We don't need it here so we leave it floating. SUSPEND# is similar to PWREN#; it is low when the USB is in suspend mode. This is used as an input to the FPGA. BDBUS0-3 are used for the JTAG interface to configure the FPGA. In order, they are TCK, TDI, TDO and TMS.

### 3.4.1 FT2232H

#### Description

#### Configuration

The FT2232H is configured to use channel A with 245 synchronous FIFO mode and channel B with MPSSE interface mode for JTAG interfacing with the FPGA.

See this [Reddit post](#) for how to use the FT2232H to program the FPGA.

#### Linked Sections

#### *pinout*

**FIXME** The FT2232H device also communicates with the FPGA using a synchronous FIFO interface as described [here](#). This seems to be the way that data is sent between the FPGA and the host computer although I'm not clear how this works. In any event, it uses the ADBUS0-7 and ACBUS0-7 pins. The ADBUS pins are bidirectional pins that serve as the FPGA side translation of the USB data. In other words, they should allow the FPGA to read USB data from a host computer and send data back to that host computer through a USB cable. The ACBUS lines seem to be used to signal reads/writes/etc. It also seems to require the external EEPROM storage IC, [93LC46B](#) although I'm not sure why this interface requires additional, external memory.

### 3.4.2 93LC46B 1k EEPROM

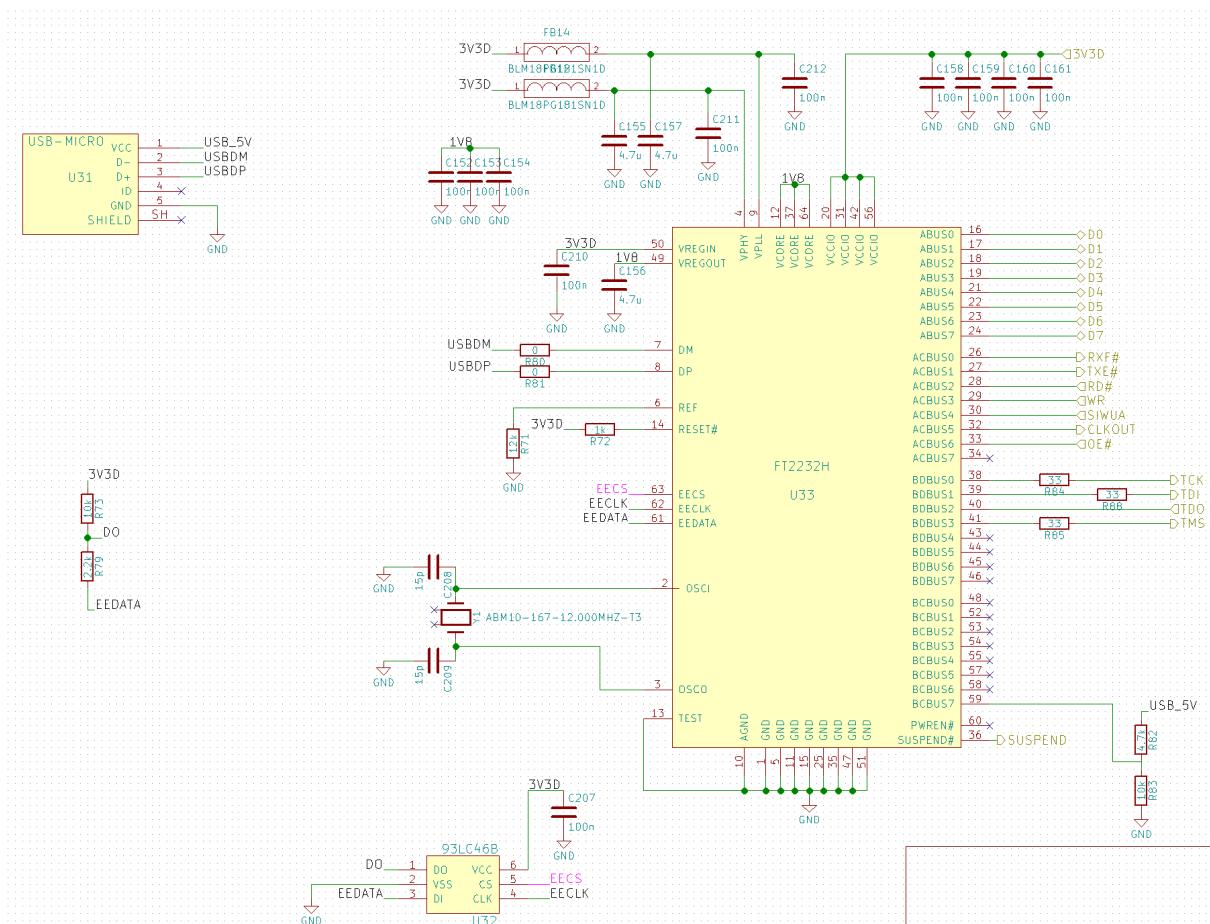


Figure 3.9: The configuration bit stream is loaded onto the FPGA using a USB-JTAG interface.

## 3.5 ADC

*schematic*

### 3.5.1 Overview

The ADC is used to digitize signals amplified by the IF [ADA4940-2](#) differential amplifiers before sending them to the [FPGA](#) for processing.

### 3.5.2 LTC2292

#### Description

The LTC2292 is a 40MHz, 12-bit differential input ADC. It has a max differential input voltage of 2V and uses two's complement output encoding which makes the minimum detectable (LSB) voltage magnitude slightly less than 0.5mV. The sampling frequency sets the Nyquist frequency at 20MHz, well above the several hundred kHz that characterize our signal frequencies. By oversampling, we're able to relax anti-aliasing filter requirements, which improves bandwidth and resolution.

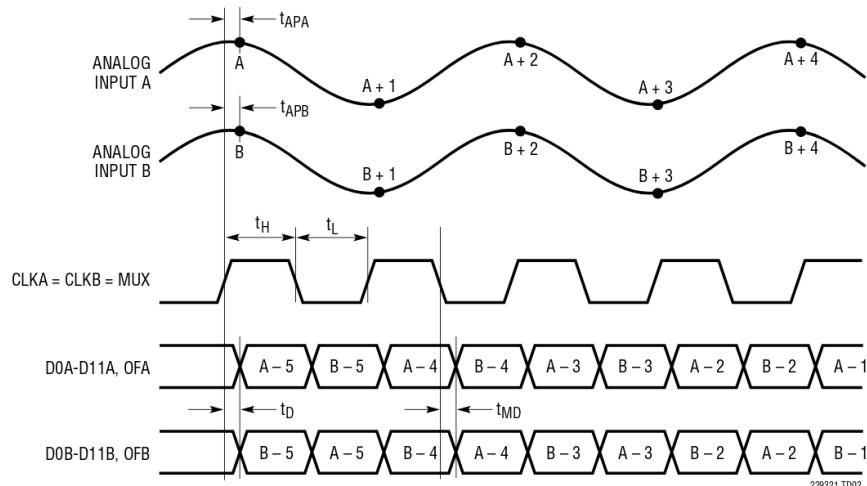


Figure 3.10: Multiplexed digital output bus timing for the LTC2292 ADC.

#### Linked Sections

*pinout*

#### Component Selection

**Fixme Fatal!**

**Fixme Fatal:** The part about the input filter should get its own section.

The analog inputs employ anti-aliasing filters. The filters provide several benefits: (1) they reduce aliasing by attenuating signals above the Nyquist frequency, (2) they limit wideband noise at the input to the ADC input, which is important because the converter has a 575MHz full-power bandwidth, and (3) they isolate the [IF amplifier](#) from ADC noise at the sampling frequency. Lastly, the capacitors act as a necessary charge source for the ADC input capacitor. The two outer 100pF capacitors (between the signal lines and ground) provide CMR low-pass filtering with a cutoff frequency of 32MHz (equation given in Eq. 3.4). The capacitor between the signal lines provides differential low-pass filtering with a

cutoff frequency of 16MHz. A [post from TI](#) explains this filtering. It's also important to keep the series resistor value low, since the greater the resistance, the greater the Johnson noise.

$$f_c = \frac{1}{2\pi RC} \quad (3.4)$$

### PCB Layout

The 100nF capacitors connected between the REFxx pins should placed as close to the pins as possible.

The differential input traces should run parallel to one another and should be placed close together. Additionally, they should be made as short as possible.

## 3.6 TX

*schematic*

### 3.6.1 Overview

An RF frequency synthesizer and external VCO are used to generate a sine wave that is periodically ramped from 5.3GHz to 5.9GHz over 1ms with a 2ms delay between ramps. The signal is then power-amplified and a portion of the resulting signal is sent to an SMA connector for transmission via an antenna and the remainder is kept on the board for mixing with the received signal. Most of the power is directed for transmission.

### 3.6.2 ADF4158 Frequency Synthesizer

#### Description

The [ADF4158](#) is a 6.1GHz fractional-n frequency synthesizer. A block diagram describing its functionality is shown in Figure 3.11.

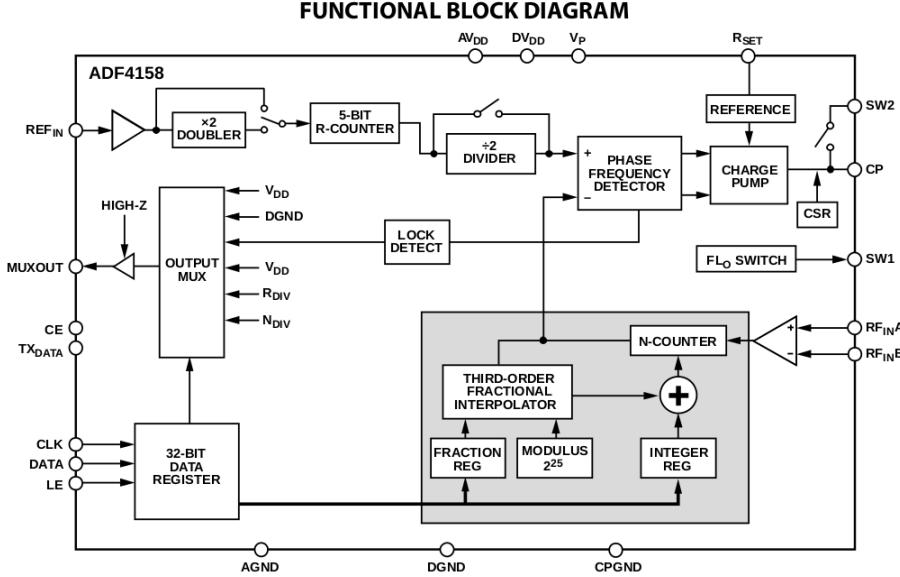


Figure 3.11: ADF4158 block diagram.

The ADF4158 relies on an external VCO, described in § 3.6.4, whose output frequency is given by Equation 3.5. The output resolution is  $f_{\text{RES}} = f_{\text{PFD}}/2^{25}$  (see Equation 3.5 and its corresponding parameter table for an explanation of  $f_{\text{PFD}}$ ). The  $2^{25}$  arises from the FRAC value (set in registers 0 and 1) which is given 25 bits.

$$\begin{aligned} \text{RF}_{\text{OUT}} &= f_{\text{PFD}} \times (\text{INT} + (\text{FRAC}/2^{25})) \\ f_{\text{PFD}} &= \text{REF}_{\text{IN}} \times [(1 + D) / (R \times (1 + T))] \end{aligned} \quad (3.5)$$

Parameter/Variable	Description
$\text{RF}_{\text{OUT}}$	The VCO's output frequency. This is the frequency that's amplified for transmission.
$f_{\text{PFD}}$	The input frequency to the PFD post prescaling. In our case this is 20MHz.

Parameter/Variable	Description
INT	The N counter that has a multiplicative effect on the VCO output frequency.
FRAC	FRAC is the numerator of the fractional number added to INT. This is what distinguishes fractional-n synthesis from integer-n synthesis. It allows greater precision for the VCO output frequency without significantly increasing the prescalers and N counter.
REF <sub>IN</sub>	The reference input frequency, which in our case is a 40MHz clock signal from the fanout buffer on the top level of the schematic.
D	The doubler bit, which can be 0 or 1. If set to 1, the REF <sub>IN</sub> frequency is doubled before arriving at the R counter.
R	The input prescaler.
T	The divide- by-2 bit, which can be 0 or 1 and divides the frequency by 2 between the R prescaler and PFD.

## Linked Sections

*pinout*

## Waveform Generation

The ADF4158 is capable of producing several different waveforms. The one used in this design is a sawtooth ramp in frequency as a function of time, shown in Figure 3.12. There are 3 different parameters that determine the shape of a ramp: (1) frequency deviation (the amount the frequency increases at each time step), (2) timeout interval (the amount of time between each time step) and (3) the number of time steps. This is shown diagrammatically in Figure 3.13. The equations governing these parameters are given in Equation 3.6. The number of steps is set directly in register 6. In our configuration  $f_{DEV} = 300\text{kHz}$  and Timer =  $0.5\mu\text{s}$ , which given that the number of steps is equal to 2000 and the starting frequency is 5.3GHz, the sawtooth will ramp from 5.3GHz to 5.9GHz in 1ms. We also use a delay between bursts of 2ms. Equation 3.7 is used to derive this.

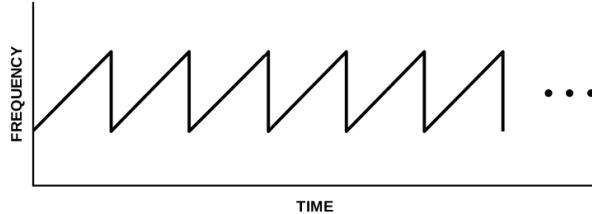
$$f_{DEV} = (f_{PFD}/2^{25}) \times (\text{DEV} \times 2^{\text{DEV\_OFFSET}}) \quad (3.6)$$

$$\text{Timer} = \text{CLK}_1 \times \text{CLK}_2 \times (1/f_{PFD})$$

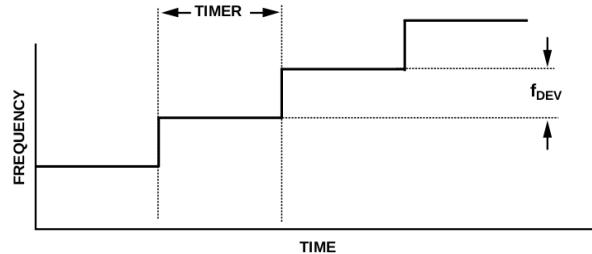
Parameter/Variable	Description
$f_{DEV}$	The frequency deviation for each frequency jump during ramp.
$f_{PFD}$	The input frequency to the PFD post prescaling. In our case this is 20MHz.
DEV	A 16-bit value set in register 5.
DEV_OFFSET	A 4-bit word set in register 5.
Timer	The time between each frequency hop.
CLK <sub>1</sub>	A 12-bit clock divider set in register 2.
CLK <sub>2</sub>	Another 12-bit clock divider set in register 4.

$$\text{Delay} = t_{PFD} \times \text{CLK}_1 \times \text{Delay Start Word} \quad (3.7)$$

Parameter/Variable	Description
Delay	The delay between bursts. This is shown graphically in Figure 3.14.
$f_{PFD}$	The input frequency to the PFD post prescaling. In our case this is 20MHz.
CLK <sub>1</sub>	A 12-bit clock divider set in register 2.
Delay Start Word	A 12-bit value set in register 7.



**Figure 3.12:** Sawtooth ramp.



**Figure 3.13:** Waveform timing.

### Configuration Registers

The ADF4158 contains 8 configuration registers. The configurations are shown in the tables below. All reserved bits should be set to 0. The control bits are the least significant 3 bits of each register and are set to the register number for each register (e.g. register 0 is 000 and register 1 is 001). I've left these out of the tables because their values are obvious.

**Table 3.18: FRAC/INT REGISTER (R0) MAP**

Bit	Mnemonic	Value	Description
3–14	FRAC(MSB)	0	This sets the 12 most significant bits of FRAC. We leave the fractional value at 0.
15–26	INT	265	This is the feedback, or N, counter.
27–30	MUXOUT Control	15	This enables “readback to muxout” which allows interrupting waveform generation and reading back the frequency at the time of interrupt. The functionality is not fully setup on the board(muxout connects to a DNP NMOS) and TX_DATA, which can trigger the interrupt, is set to 0 by the FPGA HDL and left there.
31	Ramp On	1	This bit enables the ramp.

**Table 3.19: LSB FRAC REGISTER(R1) MAP**

Bit	Mnemonic	Value	Description
3–14	Reserved	0	All reserved bits set to 0.
15–27	FRAC(LSB)	0	This sets the 13 least significant bits of FRAC. We leave the fractional value at 0.
28–31	Reserved	0	All reserved bits set to 0.

**Table 3.20: R-DIVIDER REGISTER(R2) MAP**

Bit	Mnemonic	Value	Description
3–14	CLK <sub>1</sub> Divider	10	One of the determinants of the duration of a time step in waveform generation. See § 3.6.2 for more details.

15–19	R-Counter	1	This 5-bit segment is used to divide the frequency of the reference signal before it enters the PFD. We leave it at 1 and thus do not use it to divide the frequency.
20	Reference Doubler	0	We leave this at 0 and thus do not use the doubler to double the reference signal frequency before input to the PFD. The maximum input frequency for the PFD is 30MHz and so doubling our 20MHz signal (we used the divider to divide the 40MHz signal by 2) would violate this condition.
21	RDIV2	1	Inserts a divide-by-2 toggle flip-flop between the R-counter and PFD. This provides a 50% duty cycle that allows cycle slip reduction to be used which improves lock times.
22	Prescaler	1	The prescaler limits the INT value and through that the maximum frequency to 3GHz. Since we have an INT value of 265 and our maximum frequency is almost double 3GHz we set this to 1.
23	Reserved	0	All reserved bits set to 0.
24–27	Charge Pump Current Setting	0	Sets the current to the minimum value which is 0.31mA and is the level necessary to use cycle slip reduction which we are.
28	CSR Enable	1	Enables cycle slip reduction which provides better lock times.
29–31	Reserved	0	All reserved bits are set to 0.

**Table 3.21: FUNCTION REGISTER(R3) MAP**

Bit	Mnemonic	Value	Description
3	Counter Reset	0	When this is set to 1, the synthesizer counters are held in reset. For normal operation we set this to 0.
4	Charge Pump Three-State	0	Holds the charge pump in three-state mode if set to 1. For normal operation it must be set to 0.
5	Power-Down	0	Setting this to 1 powers down the device. Setting it to 0 allows normal operation.
6	PD Polarity	1	Set to 1 for positive VCO characteristics. Set to 0 for negative VCO characteristics. Since our VCO outputs a positive voltage signal we set this to 1.
7	LDP	0	Sets the minimum number of PFD cycles before a lock detect can be set.
8	FSK Enable	0	Disables FSK modulation.
9	PSK Enable	0	Disables PSK modulation.
10–11	Ramp Mode	0	Sets the waveform as a continuous sawtooth.
12–13	Reserved	0	All reserve bits are set to 0.
14	SD Reset	0	Setting this to 0 resets the $\Sigma - \Delta$ modulator on each write to register 0, which is the recommended operation. Setting this to 1 disables resetting the modulator.
15	N SEL	0	When set to 1, this creates an additional delay in setting INT and FRAC which can prevent the PLL overshooting. Since we set INT once and do not update it, this is not necessary and we leave it as 0.
16–31	Reserved	0	All reserve bits are set to 0.

**Table 3.22: TEST REGISTER(R4) MAP**

Bit	Mnemonic	Value	Description
3–6	Reserved	0	All reserved bits are set to 0.
7–18	CLK <sub>2</sub> Divider	1	This is used to set the timeout interval in ramp generation. See § 3.6.2 for more information.
19–20	CLK DIV Mode	3	This enables ramp divider mode, which specifies that CLK <sub>1</sub> and CLK <sub>2</sub> are used for ramp generation.
21–22	Readback to MUXOUT	3	Confusingly, this has been set to 3, which corresponds to neither of the supported values. Since we don't actually use the MUXOUT, this seems to be fine. If, at some point in the future, we do use the MUXOUT we will probably need to fix this.
23–24	Negative Bleed Current	0	This setting can help improve performance in the dead zone. We've disabled it. Note that this setting and readback to MUXOUT cannot simultaneously be enabled. To understand this setting better refer to <a href="#">AN-1154 Application Note</a> .
25	Reserved	0	All reserved bits are set to 0.
26–30	Σ – Δ modulator mode	0	0 enables this during normal operation. We can set it to 14 when FRAC=0. Even though we've set FRAC to 0, we have left this as 0 which seems strange. It shouldn't cause anything to malfunction, but may cause the ADF4158 to draw more power. We should experiment with setting this to 14 when using the actual board.
31	LE SEL	0	LE is the load enable pin which we use to load data onto the ADF4158's internal registers. Setting this to 0 enables the default operation of using the pin to set LE. Setting it to 1 would synchronize it with the reference signal.

**Table 3.23: DEVIATION REGISTER (R5) MAP**

Bit	Mnemonic	Value	Description
3–18	Deviation Word	31457	This is used to set the size of successive frequency jumps during ramp. See § 3.6.2 for more information.
19–22	Deviation Offset Word	4	This is also used to set the size of successive frequency jumps during ramp. See § 3.6.2 for more information.
23	Deviation Select	0	Setting this bit to 1 is used for FSK as described on page 28 of the datasheet. Since we do not use FSK we leave this as 0.
24	Ramp 2 Enable	0	Setting this bit to 1 allows a second ramp with different settings than the first. We only need the first ramp.
25	FSK Ramp Enable	0	Setting this bit to 1 uses FSK. Again, we do not use FSK and so leave this bit as 0.
26–27	Interrupt	0	Sets the type of interrupt used to read the value of INT and FRAC of the ramp at a given moment. We don't read these values and therefore leave this as 0, which corresponds to interrupt off.
28	PAR Ramp	0	Setting this bit to 1 allows a parabolic ramp which we don't use.
29	Tx Ramp CLK	0	Setting this to 0 uses the clock divider (instead of the TX data clock) for clocking the ramp.
30–31	Reserved	0	

**Table 3.24: STEP REGISTER (R6) MAP**

Bit	Mnemonic	Value	Description
3–22	Step Word	2000	This determines the number of steps in a ramp. To understand this see § 3.6.2 on waveform generation.
23	Step SEL	0	This bit is used when 2 different ramps are needed (for instance with FSK). As we don't need this functionality we leave it off and set this bit to 0.
24–31	Reserved	0	

**Table 3.25: DELAY REGISTER (R7) MAP**

Bit	Mnemonic	Value	Description
3–14	Delayed Start Word	4000	Sets the ramp start delay. We do not use a start delay, but we do use this to delay between ramps.
15	Delayed Start Enable	0	We do not use a start delay.
16	Delay Clock Select	1	Increases the period of the delay clock by multiplying the period of the PFD clock by CLK <sub>1</sub> . This creates an effective period of 500ns.
17	Ramp Delay	1	We enable a delay between ramp bursts.
18	Ramp Delay Fast Lock	0	Disables the ramp delay fast lock function.
19–31	Reserved	0	

### Programming the Configuration Registers

The write timing used to program the internal configuration registers is shown in Fig. 3.16. The maximum clock frequency is 20MHz, which can be achieved by dividing the reference clock frequency by 2. Additionally, LE must be brought low at least half a clock period before data is clocked into the registers and held low for at least a quarter of a period after the write ends. It then must be pulsed high for half a period before it can be brought low again and another register write can occur. As shown in the diagram, the data is sent MSB first and the last 3 bits are the control bits (which specify the destination register), also sent MSB first. The registers must be configured in a specific order, detailed in the “INITIALIZATION SEQUENCE” section of the datasheet, and copied below for convenience.

1. Delay register (R7)
2. Step register (R6)—load the step register (R6) twice, first with STEP SEL = 0 and then with STEP SEL = 1
3. Deviation register (R5)—load the deviation register (R5) twice, first with DEV SEL = 0 and then with DEV SEL = 1
4. Test register (R4)
5. Function register (R3)
6. R-divider register (R2)
7. LSB FRAC register (R1)
8. FRAC/INT register (R0)

### 3.6.3 TLV172 Operational Amplifier

#### Description

The TLV172 op-amp is used to produce a gain of 2 to match the CP output of the ADF4158 to the VTUNE input of the VCO. This is necessary since the charge pump supports a tune voltage of up to 5.5V but the VCO has a tune range of 0V to 10V. A non-inverting amplifier configuration is used to produce the necessary gain.

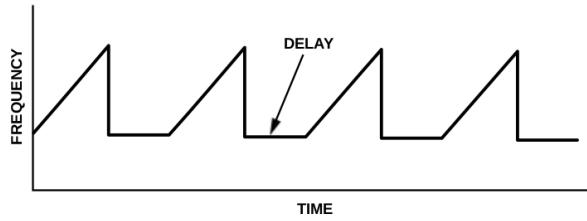


Figure 3.14: Delay between ramps for sawtooth mode.

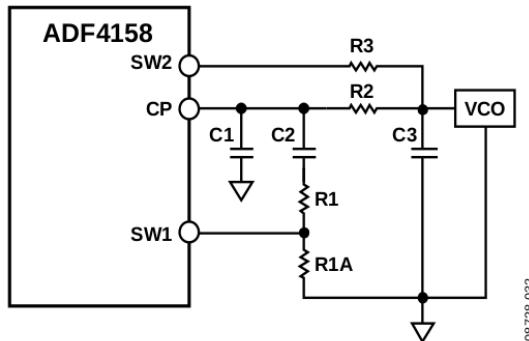


Figure 46. Fast-Lock Loop Filter Topology—Topology 1

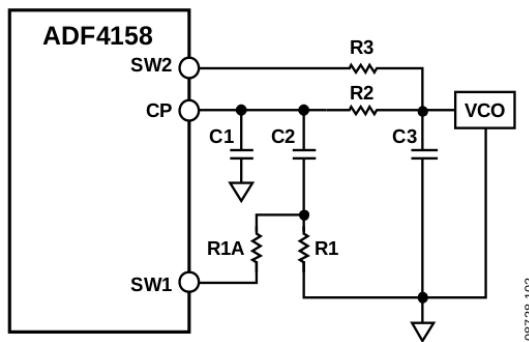


Figure 47. Fast-Lock Loop Filter Topology—Topology 2

Figure 3.15: Fast lock topologies.

### Component Selection

The 100nF bypass capacitor is recommended by the datasheet.

### PCB Layout

The recommended layout for the TLV172 op amp is shown in Fig. 3.17.

### 3.6.4 HMC431LP4RF VCO

The [HMC431LP4RF](#) is a radio-frequency VCO.

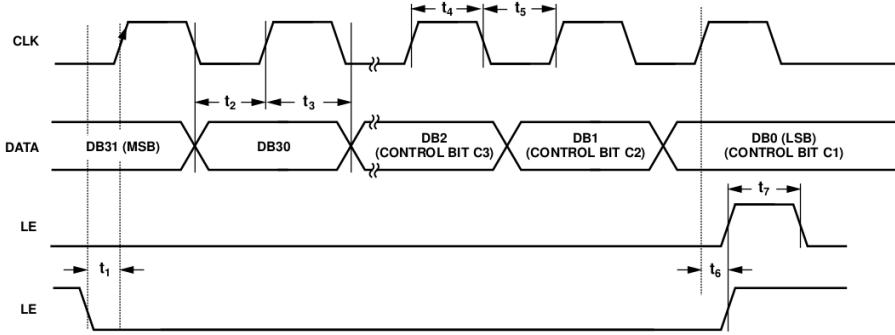


Figure 3.16: ADF4158 write timing diagram.

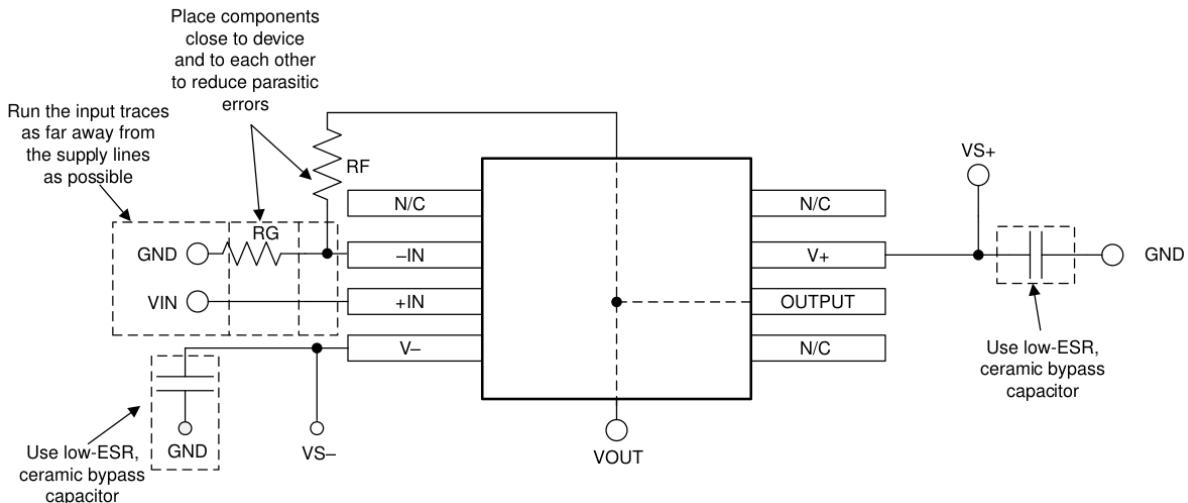


Figure 3.17: TLV172 op-amp recommended PCB layout.

### 3.6.5 DC4759J5020AHF Directional Coupler

#### Description

The DC4759J5020AHF is a directional coupler with a 20dB coupling factor, 0.17dB insertion loss and 10.3dB directivity. It is used to redirect some of the transmission power back to the mixer's local oscillator input. A directional coupler is a 4-terminal device, whose general form is shown in Fig. 3.18. The coupling factor gives the amount of input power that is redirected to the coupled port, the insertion loss gives the amount of input power that is transmitted through to the output port and the directivity is a measure of the coupler's ability to isolate the coupled and isolation ports. The actual equations are given in Eq. 3.8, Eq. 3.9 and Eq. 3.10. In an ideal coupler, all input power is either transmitted through or coupled. However, in all real directional couplers, some power is directed to the isolation port. In our case 25.8dBm is directed for transmission, 6dBm is coupled, and -4.3dBm is sent to the isolated port.

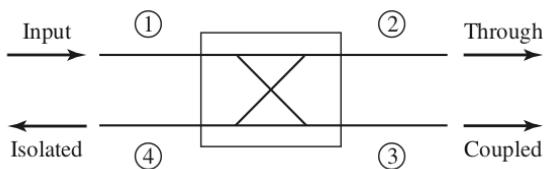


Figure 3.18: Directional coupler.

$$C = 10 \log \frac{P_1}{P_3} \quad (3.8)$$

$$L = 10 \log \frac{P_1}{P_2} \quad (3.9)$$

$$D = 10 \log \frac{P_3}{P_4} \quad (3.10)$$

### PCB Layout

The recommended PCB layout is shown in Fig. 3.19, where the leftmost pads correspond to the input and direct pins. All PCB traces leading from the pads should have a  $50\Omega$  characteristic impedance.

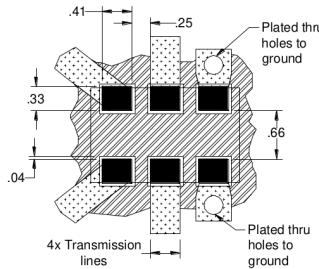


Figure 3.19: DC4759J5020AHF recommended PCB layout.

### 3.6.6 PD4859J5050S2HF Wilkinson Power Divider

#### Description

The PD4859J5050S2HF is a Wilkinson power divider that equally divides the input power between the two output ports. We use one after the VCO to share its 2dBm output power between the power amplifier and the RF<sub>IN</sub> port of the frequency synthesizer.

#### PCB Layout

The recommended layout is shown in Fig. 3.20. Ensure the location of the external  $100\Omega$  0603 resistor matches the location shown in the figure. All ports have a  $50\Omega$  characteristic impedance which must be matched by the input and output traces.

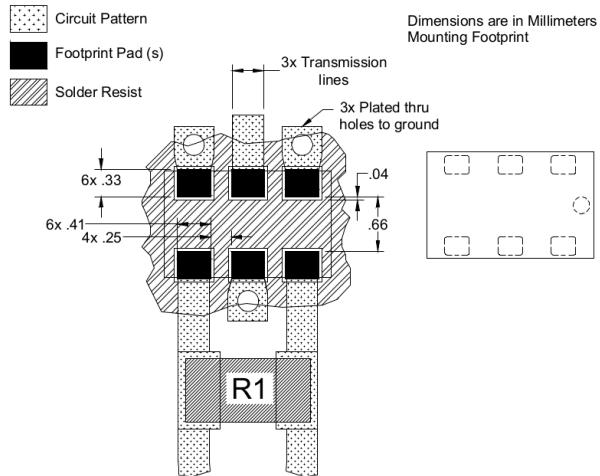
### 3.6.7 PAT1220 RF Attenuator

#### Description

The PAT1220 is a simple resistive attenuator that can be used to preserve the shape of a signal but decrease its power.

We use a 5dB attenuator between the VCO and power amplifier in order to set the power amplifier's output power to its typical value of 26dBm as specified by the datasheet (it has a small-signal gain of 32dB). This is enough power for a small radar (see § 2.1) and is sufficiently below the 1dB compression point, which should ensure good linearity.

I've placed a 3dB attenuator between one of the Wilkinson power divider outputs and the RF<sub>IN</sub> port of the frequency synthesizer. This shouldn't be strictly necessary, since the max power of the RF<sub>IN</sub> port is 0dBm. However, using  $-1\text{dBm}$  would be playing it a bit close. Additionally, the 2dBm output of the VCO is a typical power output, not the max power, which makes foregoing the attenuator even more



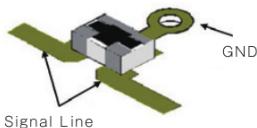
**Figure 3.20:** PD4859J50502SHF recommended PCB layout. Note the location of the resistor.

dangerous. Finally, the  $\text{RF}_{\text{IN}}$  port supports an input power of as low as  $-10\text{dBm}$ , so we have plenty of room on the downside.

The last attenuator (6dB) is used at the coupled port of the [directional coupler](#), on its way to the local oscillator input of the [mixer](#). Again, the unattenuated 6dBm should be ok (the max input power of the LO is 10dBm). However, using the attenuator brings the LO power down to the typical value specified by the mixer datasheet. To make sure our devices operate properly, we might as well use the conditions recommended by the datasheet.

### PCB Layout

The recommended layout is shown in Fig. 3.21. The ports are matched for a  $50\Omega$  characteristic trace impedance.



**Figure 3.21:** PAT1220 recommended PCB layout.

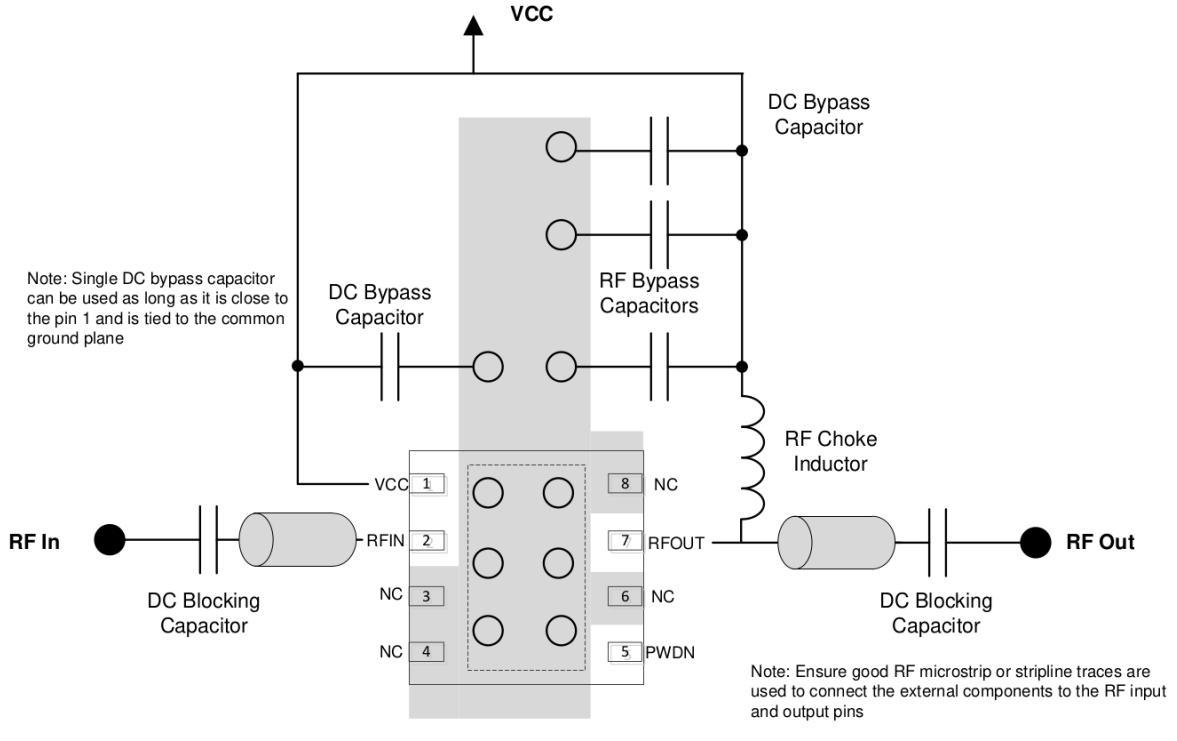
### 3.6.8 SE2567L Power Amplifier

## 3.7 RX

### 3.7.1 SKY65404 LNA

### 3.7.2 TRF37A73 Gain Block

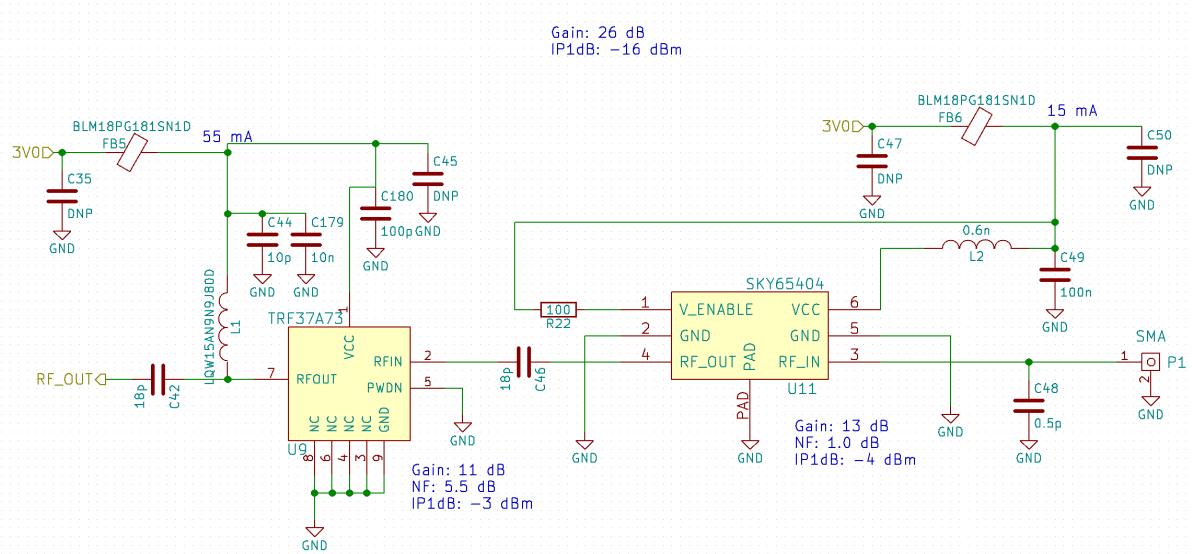
#### PCB Layout



**Figure 3.22: TRF37A73 recommended PCB layout.**

The sheets RX1 and RX2 are identical. They each consist of two amplifiers connected in series, shown in Figure 3.23. The first amplifier is a [SKY65404](#) LNA which operates in the 4.9GHz-5.9GHz range, has a gain of 13dB, a NF of 1dB and a P1dB of -4dBm. It is hooked up exactly as specified in the datasheet, with the addition of a ferrite bead filtering its power supply.

The second amplifier is a [TRF37A73](#) RF gain amplifier. It is wired up as recommended in the datasheet, with the addition of a ferrite bead to filter the power supply. Values for the various capacitors and inductor are left out of the datasheet. A 100pF capacitor is used to short high frequency noise to the power supply, which is typical of microwave devices. **{START INCOMPLETE}** I am not sure how the values for the RF bypass capacitors, the inductor, and the DC blocking capacitors was chosen. Additionally, I'm not sure how he arrives at a gain of 26dB, since I've read that gains in series should be additive (and hence 24dB), and I'm not sure where the IP1dB value of -16dBm comes from **{ENDINCOMPLETE}**.



**Figure 3.23:** One of two RX schematic sheets. Both sheets are identical and consist of two amplifiers connected in series.

## 3.8 Mixer

### 3.8.1 Overview

A mixer modulates the original RF transmission signal with the two amplified RF reception signals to produce IF signals that encode the distance and incident angle to the remote object (see discussion in ??).

### 3.8.2 5400BL15B050E RF Balun

#### Description

The 5400BL15B050E is a balun that supports frequencies of 4.9 – 5.9GHz. It is suggested by the [mixer](#) datasheet for downconversion from RF to IF.

### 3.8.3 ADL5802 Mixer

#### Description

The ADL5802 incorporates two Gilbert cells that allow modulating a local oscillator signal with two separate RF signals for upconversion or downconversion. It's used here for downconversion to IF. The mixer supports input frequencies of 100MHz – 6GHz and output frequencies of about 30kHz – 600MHz. This fits our requirements which have input frequencies staying below 5.9GHz and output frequencies on the order of several hundred kHz.

#### Pinout

#### Component Selection

The input baluns and 3pF capacitors are specified by the datasheet for the 5.3 – 5.9GHz frequency we are using. The input interface is shown in Fig. 3.24, which is taken directly from the datasheet. Notice that the LO positive balanced signal should be connected to LOIN and vice versa.

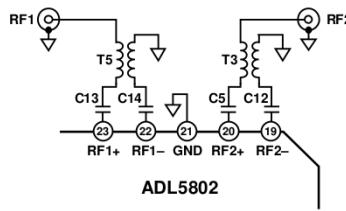


Figure 69. ADL5802 RF Interface

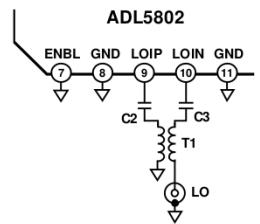


Figure 3.24: ADL5802 input interface.

## **PCB Layout**

The RF and LO input interfaces are designed for a differential input impedance of  $50\Omega$ . This is already the differential balanced impedance of the baluns, so we do not need to perform any additional impedance matching at the inputs. The inputs require AC coupling and the datasheet recommends  $3\text{pF}$  coupling capacitors placed between the balun outputs and pin inputs. It also shows that the positive balun output of the local oscillator should be hooked up to the positive pin input.

## 3.9 IF

### 3.9.1 Overview

A differential amplifier is used to amplify the output of the mixer before quantization by the ADC.

### 3.9.2 ADA4940-2 IF Differential Amplifier

#### Description

The ADA4940-2 supports a max differential voltage at its input pins of  $\pm 1V$ . **Fixme Fatal: How do I know that the ADL5802 outputs a differential voltage in this range. There are voltage gain numbers on the mixer datasheet. However, I'm also confused about the power input to the mixer.** Fixme Fatal!

#### Pinout

Table 3.26: The ADA4940-2 ADC pinout.

#	Pin	Description
1	-IN1	
2	+FB1	
3, 4	+VS1	Positive supply voltage for the first differential amplifier. This is tied to +3.3V.
5	-FB2	
6	+IN2	
7	-IN2	
8	+FB2	
9, 10	+VS2	Positive supply voltage for the second differential amplifier. Also tied to +3.3V.
11	VOCM2	Common-mode voltage of the second differential amplifier. This is set to 1.5V by the ADC.
12	+OUT2	Amplifier 2's positive differential output.
13	-OUT2	Amplifier 2's negative differential output.

#### Component Selection

The resistor selection determines the closed-loop gain according to Eq. 3.11, and whose values correspond to those shown in the block diagram in Fig. 3.25. We've used  $R_F = 8.2k\Omega$  and  $R_G = 549\Omega$ , yielding a differential gain of 15.

$$V_{+OUT} - V_{-OUT} = (+D_{IN} - (-D_{IN})) \times \frac{R_F}{R_G} \quad (3.11)$$

The components between ADL5802 and the IF amplifier form a high-pass filter with a transfer function shown in Fig. 3.26. The filter has a flat gain of  $-10dBV$  from about 30kHz through several hundred kHz and still stays below  $-5dBV$  up to 1MHz. The phase angle is also mostly flat at 0 in this region. The transfer function was performed using Ngspice with KiCad, and the schematic for it is shown in Fig. 3.27.

#### PCB Layout

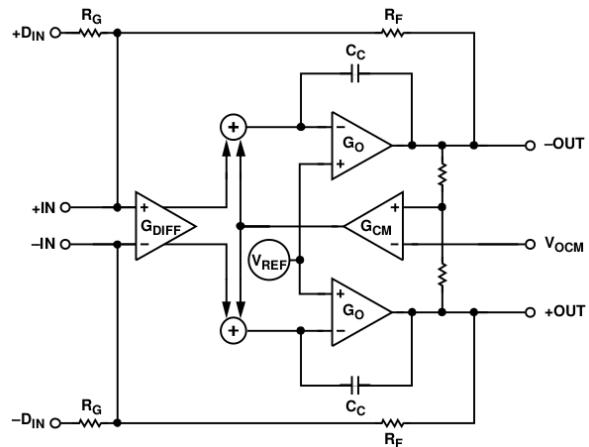


Figure 3.25: ADA4940-2 block diagram.

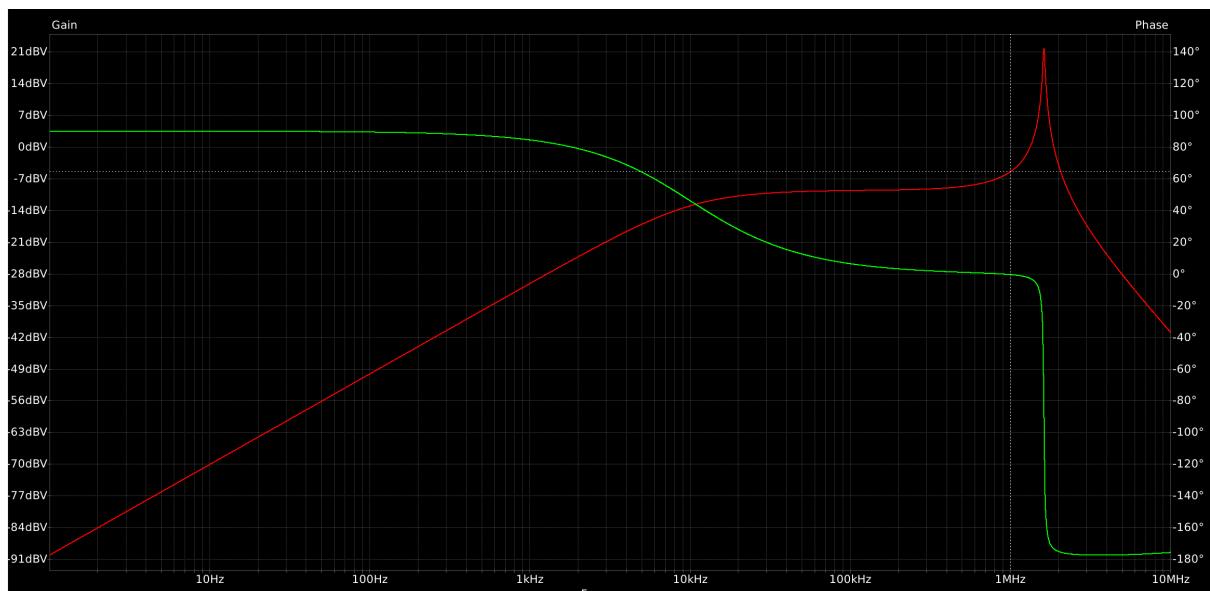
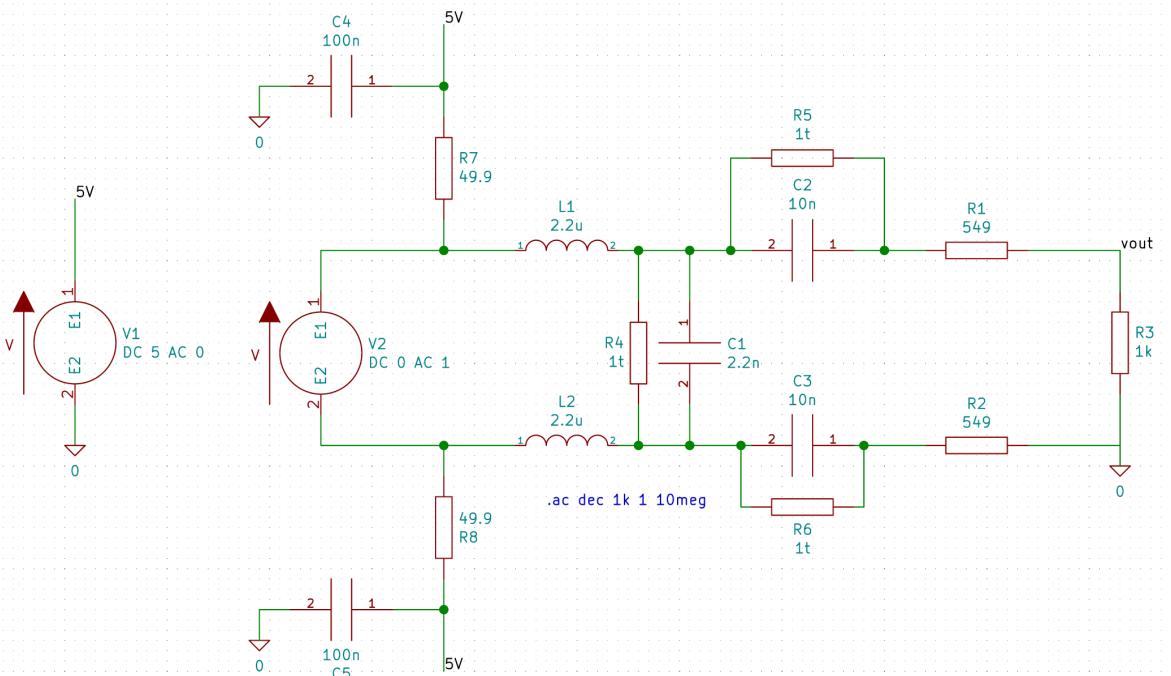


Figure 3.26: High-pass filter at the IF amplifier differential inputs.



**Figure 3.27:** Schematic for the Ngspice simulation of the high-pass filter. The  $1T\Omega$  resistors in parallel with the capacitors provide a DC current path to ground and are necessary for the simulation to work.

# Chapter 4

## PCB

### 4.1 General Layout

**Fixme Fatal:** This should be rewritten for my layout.

The radar is constructed using a 4-layer board and uses both surfaces of the board. The front layer contains nearly all of the board's components while the back layer contains a few surface mount resistors and capacitors. The top layer primarily contains signal traces for top layer SMD components. In particular, it connects many of the signal traces of the ADC to the FPGA, which is placed next to it. Note, however, that most of the signal traces extending from the FPGA only start on the top layer but travel through layer 3. The buck converters and subsequent linear regulators are placed near the top of the board, not necessarily near the components they drive. In addition to the large number of signal traces, the top copper layer contains a large ground plane around the periphery of the board. The 2nd layer is entirely a ground plane. The 3rd layer is largely a ground plane, although it also contains a significant number of traces extending from the FPGA as well as a few other components. The 4th layer primarily contains large power planes for each of the different voltages driving logic in the design. It is worth noting that even though it contains significant power planes, it still has a ground plane that is the largest copper fill zone in this layer. The PCB also has 3 large corner mounting vias with smaller vias placed in a circle in the large via's annular ring. The reason for the small vias is to ensure a continued connection to GND (the mounting vias are connected to GND) even if a screw thread strips too much copper from the main via. Additionally, it helps prevent the PCB from being crushed if too much torque is used to tighten the screw. The 4th corner is occupied by the connections to the DC barrel jack. Power rail traces are made 0.5mm in width whereas signal traces are 0.2mm in width. Grounded vias are placed liberally throughout the design. They have a diameter of 0.46mm and a drill hole size of 0.254mm. I've included several screenshots of the PCB and highlighted important components (Figures 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10, 4.11, 4.12).

### 4.2 Board Layout

There should be a section here on board layout. I.e. signal plane, ground plane, power plane, etc. See High Speed Digital Design for recommendations. Also calculate the capacitance between the power and ground plane. Btw, this is a great way to further filter noise from the power supplies.

**Fixme Fatal:** I'm not exactly sure where it should go, but there should be a section that documents the use of vias, especially for high speed signals. Use page 258 of High Speed Logic to calculate the step response, and present the results here. Additionally, mention via best practices such as placing an adjacent ground via to any signal via to provide a current return path. Also, the use a multiple small vias instead of one large one to minimize inductance. While we're at it, it's probably also good to calculate trace inductance for

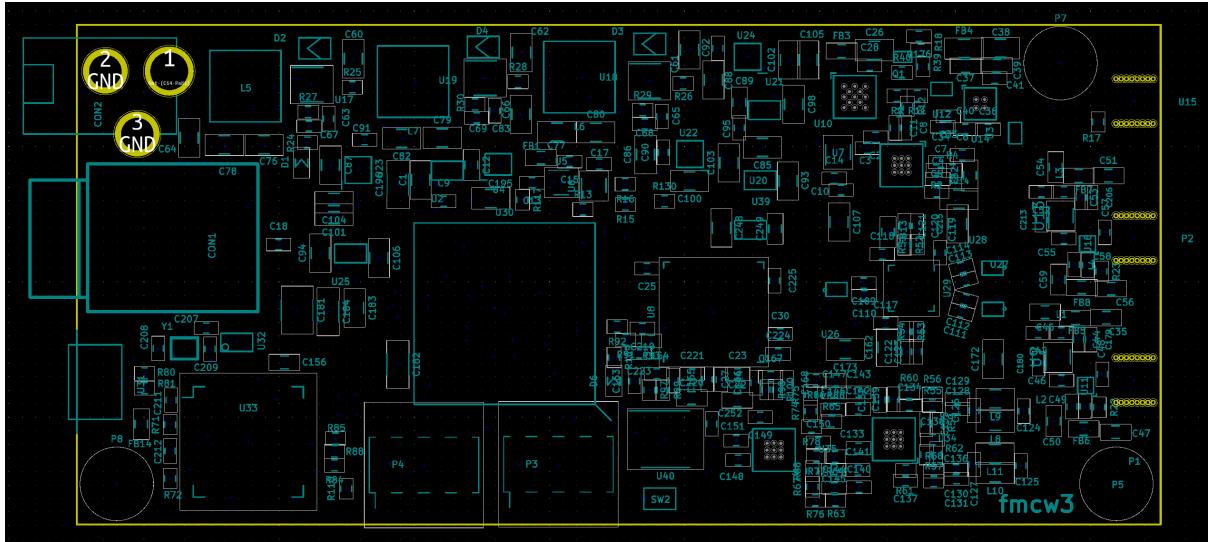


Figure 4.1: Board layout. The top left of the board is where the power source (barrel jack) is connected. The output of the 12V power source is connected to a power plane at the top left-middle of the board, that feeds into the buck converters. Large inductors connected to the buck converters are placed adjacent to their corresponding buck converters. The outputs of the buck converters feed into linear regulators that are mostly placed directly below the buck converters. This is also the region where the main crystal oscillator is placed and its associated fan-out buffer. Transmission circuitry (the frequency synthesizer and some RF amplifiers) are placed at the upper right side of the board near the antenna connectors which are placed on the right side of the board. Circuitry for signal reception are placed along the right side, adjacent to the antenna connectors. The mixer is placed slight inward from here, vertically centered but toward the right side of the board. Below this are intermediate frequency op-amps that feed the mixed signal into an ADC located just above it and to the left (U8). Located just to the left of the IF amplifiers and below the ADC is a flash memory IC (U40) which feeds data to the FPGA (U30), located just to the left of the ADC. Connectors below the FPGA (P3 and P4) can be used to externally monitor the FPGA. In the bottom left of the board is a component to convert USB data to UART data to configure the FPGA as well as a micro USB connection to connect to a host computer. On the left side of the board between the USB connection and barrel jack is a SD card reader that stores data that can be read back out the FPGA.

certain important signals. I'm not sure where the equation for this is, but it should be in High Speed Design.

### 4.3 RF Impedance Matching

Document via fencing used. Note the general rule that spacing between vias should not be more than the RF wavelength divided by 20. I believe the wavelength is 5cm, but check this and then put this in the documentation. For the impedance line width I've decided to go with the original design's 14.96mil. I'm a little skeptical of the Mantaro tool below which seems to not calculate effective impedance. Saturn PCB should be pretty good, and if you can get OpenEMS to do this that would be the best.

Also document the RF via. Note the parallel ground trace running below it (and the ground plane above it).

**Fixme Fatal!**

**Fixme Fatal: I don't think the text below is correct..**

I'm keeping it for the value of knowing the trace widths used by the original design. However, the idea that the trace widths are unimportant seems dubious. The PCB calculator built into KiCad should be

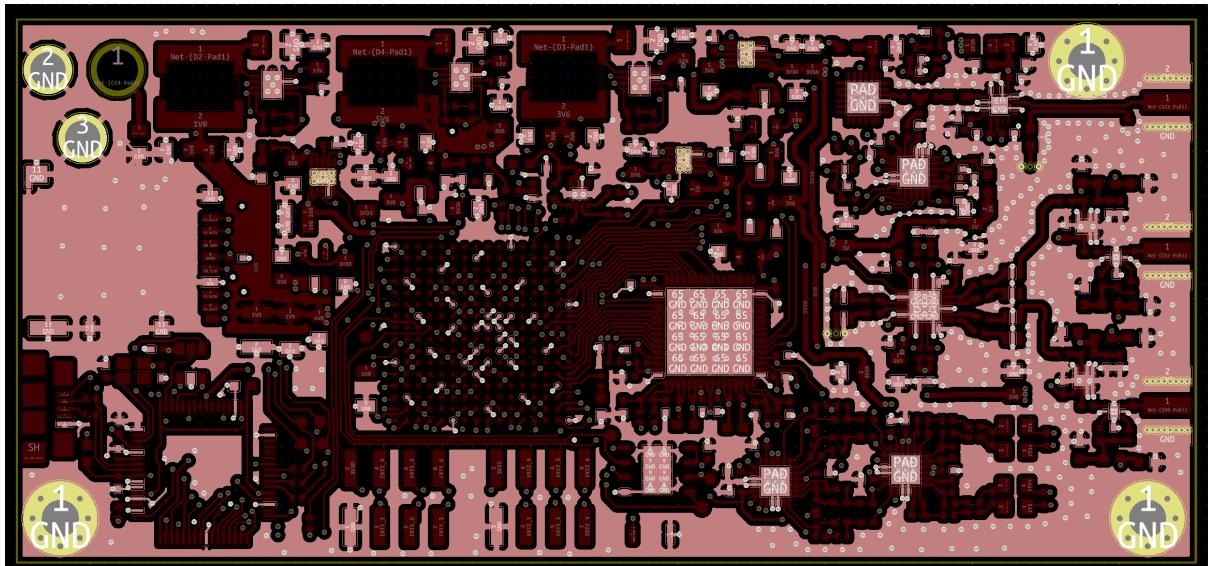


Figure 4.2: A significant portion of layer 1 is a ground plane and the other large part of it is signal traces connecting components. There is also a small 1V power plane toward the upper left not highlighted here.

used for this. Additionally, it is probably worth looking at the following guides: [Maxim: General Layout Guidelines for RF and Mixed-Signal PCBs](#), [Hackaday: Michael Ossmann makes you an RF design hero](#), [Analog](#). I would also look at [this tool](#) for creating a Wilkinson power divider. Also, the trace width for  $50\Omega$  resistors seems to have been more like 15mil.

Use [this Mantaro impedance calculator](#) to calculate trace widths. The proper width should be 11.98mil.

The right side of the board houses the RF circuitry (i.e. transmitter, receivers and SMA connectors). The signals are carried to the antennas (a patch-fed horn for transmission and a patch array for reception) via a  $50\Omega$  coaxial cable. All RF inputs and outputs for components should match this  $50\Omega$  impedance. The original layout does not seem overly concerned with the microstrip transmission line width between RF components. They are kept short and generally have a trace width of about 0.3mm. However, many of them are not even remotely straight and this doesn't seem to be an issue. Where possible the microstrips should be kept short, straight and with an unbroken ground plane beneath them. That seems to be all that is necessary for impedance matching. The patch antennas however will need to be appropriately hooked up in order to match the  $50\Omega$  impedance. This should be a relatively straightforward calculation. The setup Henrik uses seems to be the most logical one. He uses a single patch-fed horn antenna for transmission and a patch array for reception. The horn antenna is made of thin copper. More sophisticated horn antennas require the ability to weld and probably modeling software (e.g. CST).

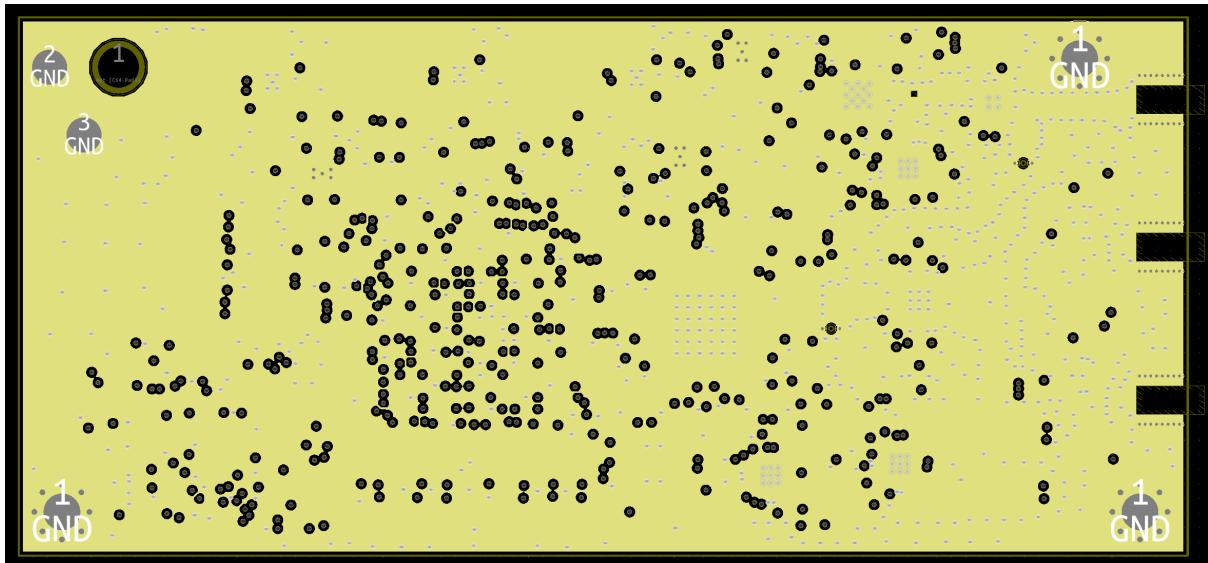


Figure 4.3: All of layer 2 is a ground plane.

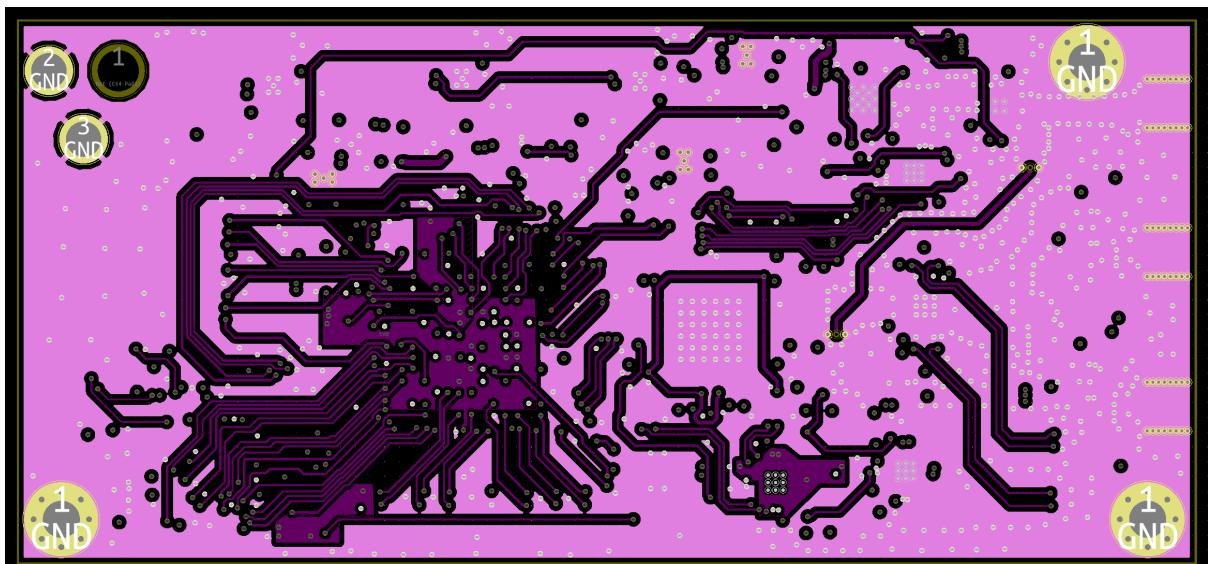


Figure 4.4: Most of layer 3 is a ground plane but there are also a substantial number of trace connecting to the FPGA. It does also contain 1V an 3.3V power planes.

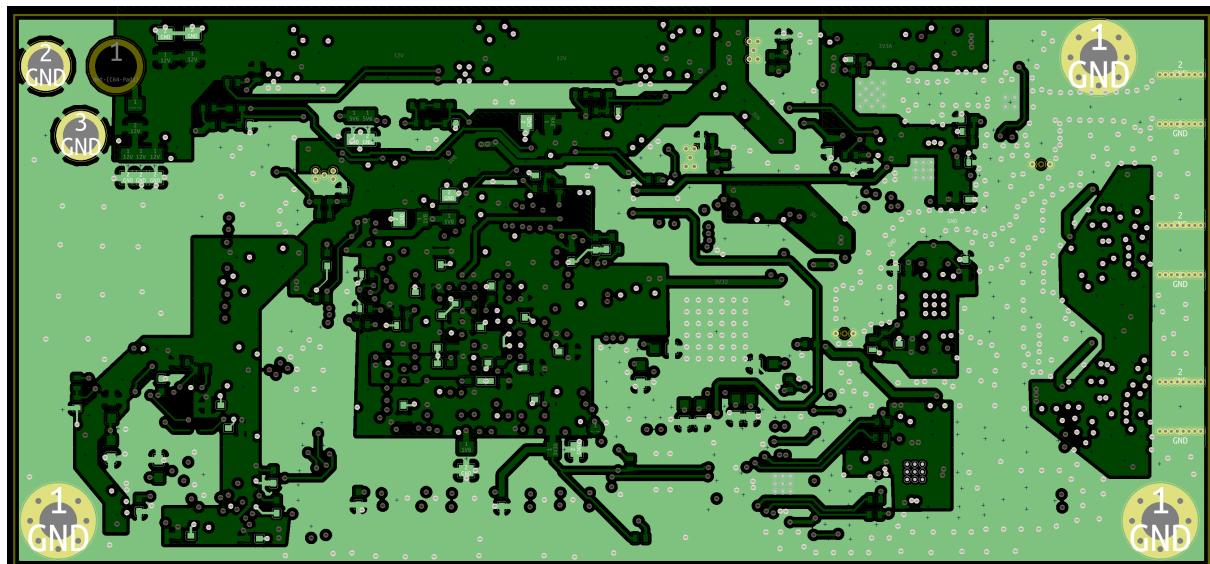


Figure 4.5: The 4th layer of the PCB contains a large ground plane with many vias interspersed.

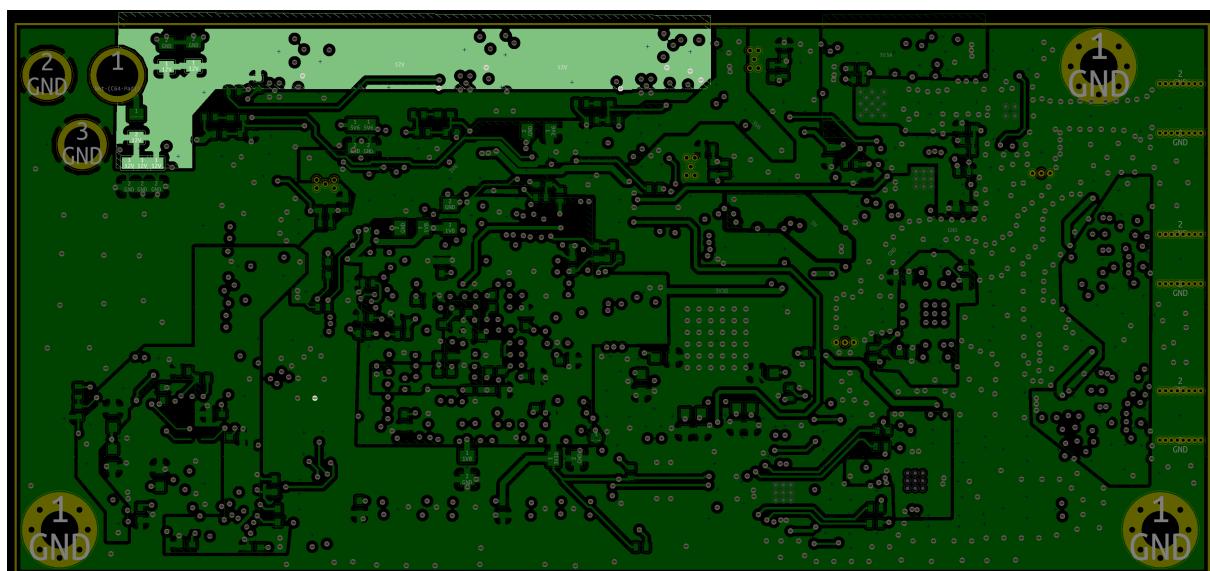


Figure 4.6: The 12V power plane is located at the top of the board adjacent to the D barrel jack and the buck converters it feeds.

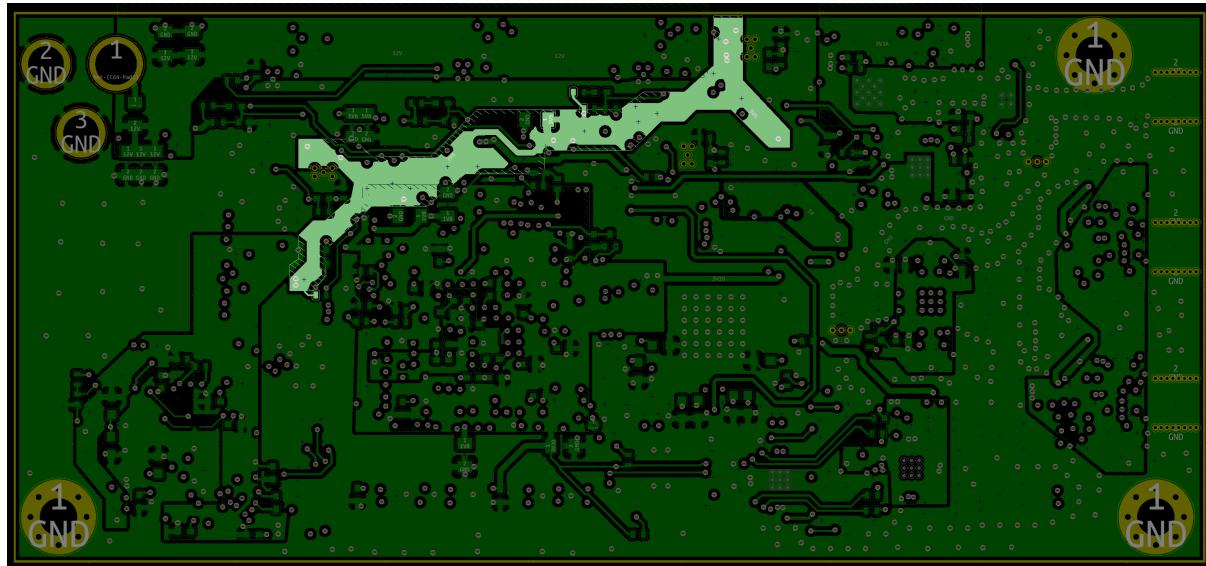


Figure 4.7: There is a 3.6V power plane that is the output of one of the buck converter and is used as the input to several linear regulators that output 1.8V 3.0V and 3.3V.

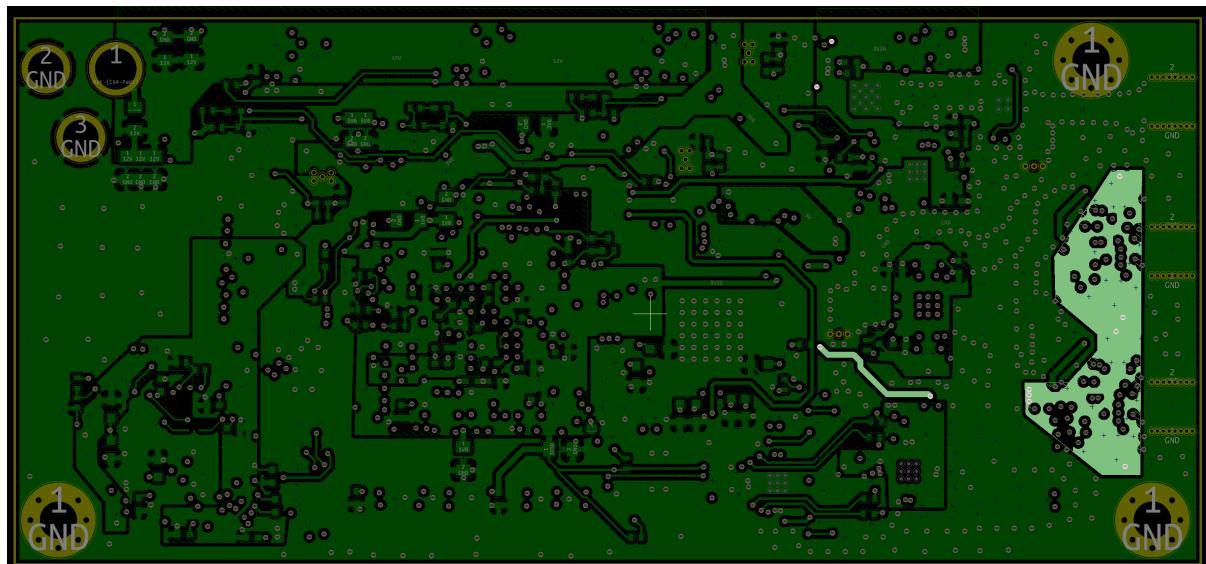


Figure 4.8: A 3V power plane is used to power components near the right side of the board (the right side of the board is where signal transmission and reception occur that amplify receive signals so they can be mixed with the transmitted signal and fed into the ADC before FPGA processing). Notably, the 3V power plane is located near the components but far from the linear regulator that outputs it.

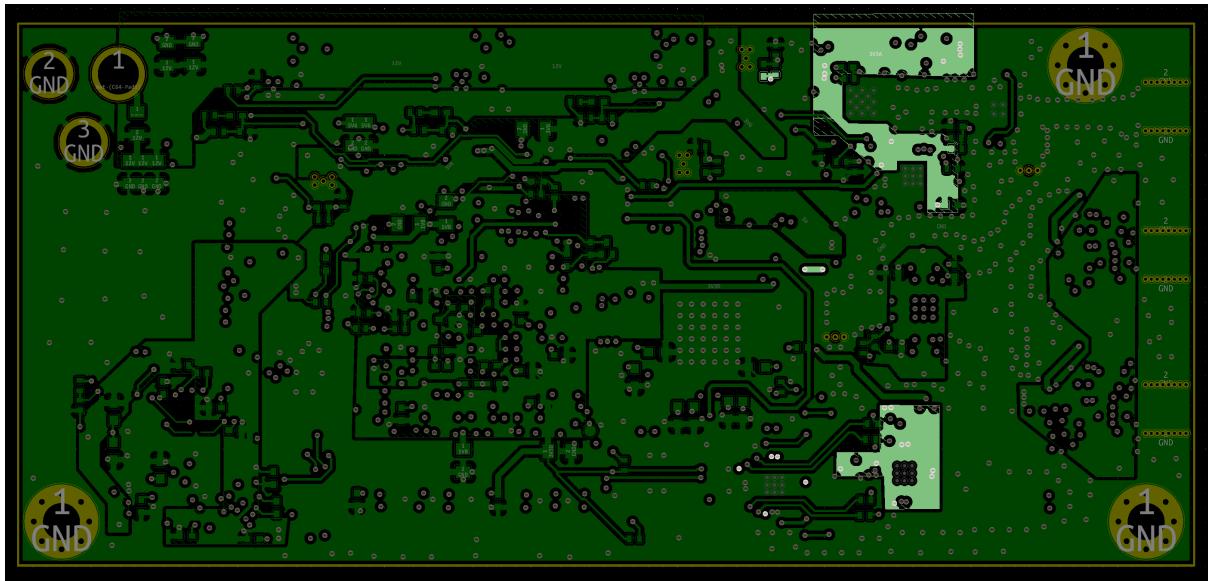


Figure 4.9: A 3.3V power plane is used to power several components for signal transmission, such as a frequency synthesizer, and RF amplifier. These, along with all other reception and transmission circuitry, are located on the right side of the board.

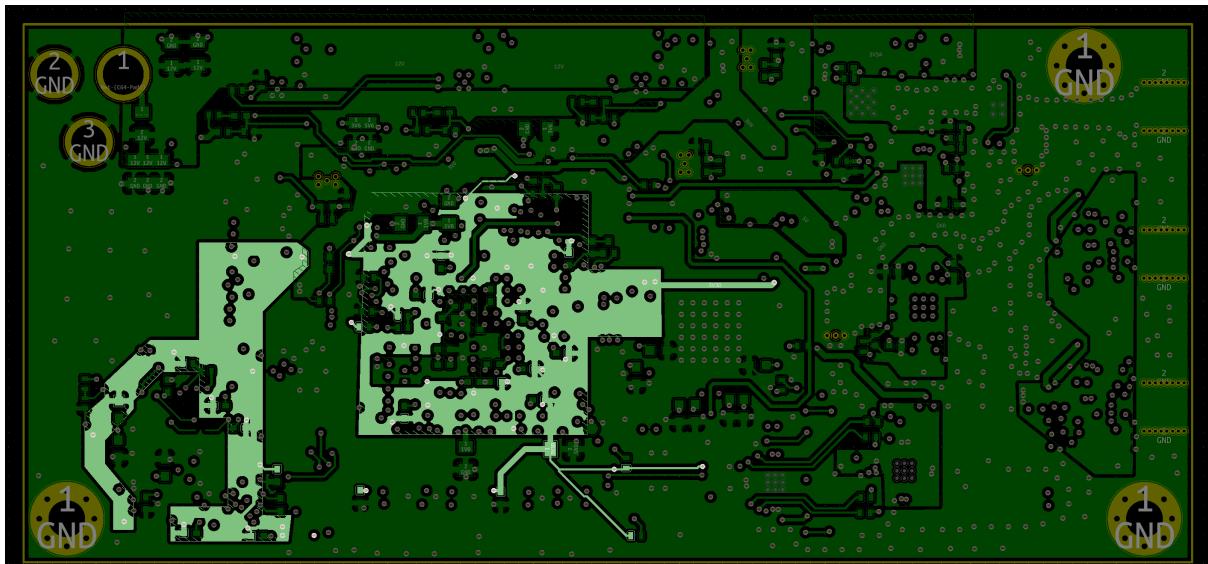


Figure 4.10: Another 3.3V power plane is used as one of the power inputs to the FPGA as well as to a USB-to-UART device (a configuration bit stream is sent from a host computer through a USB cable to the PCB where this device converts it into the proper UART format to be transmitted to the FPGA) and an ADC (the ADC converts the mixed transmitted-received signals to digital and then sends them to the FPGA for processing).

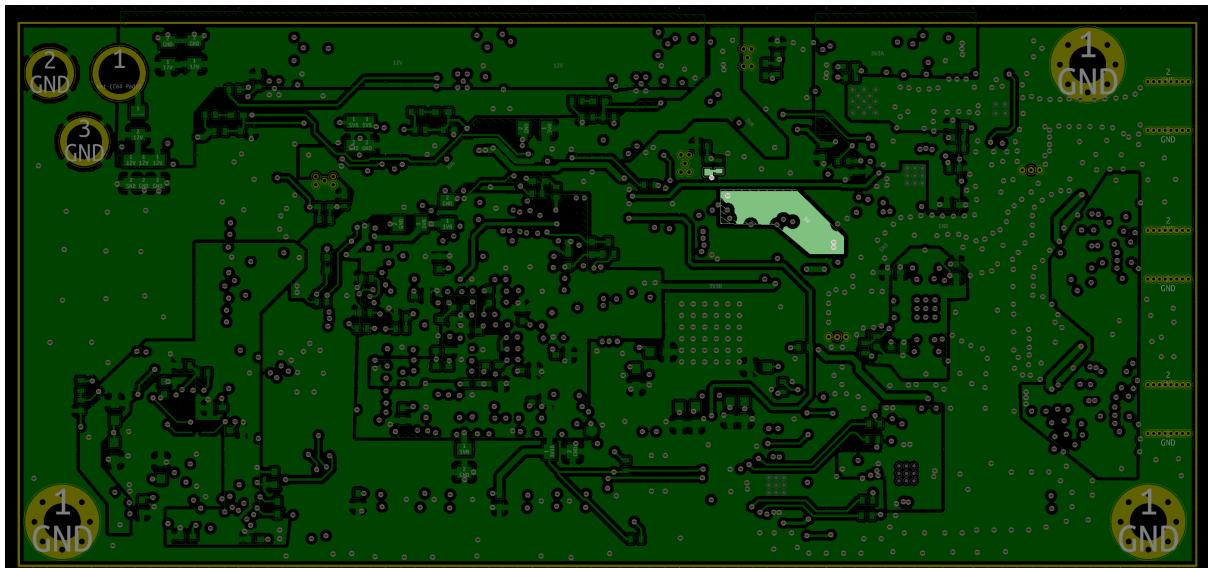


Figure 4.11: A 5V power plane powers one of the inputs to the frequency synthesizer for transmission.

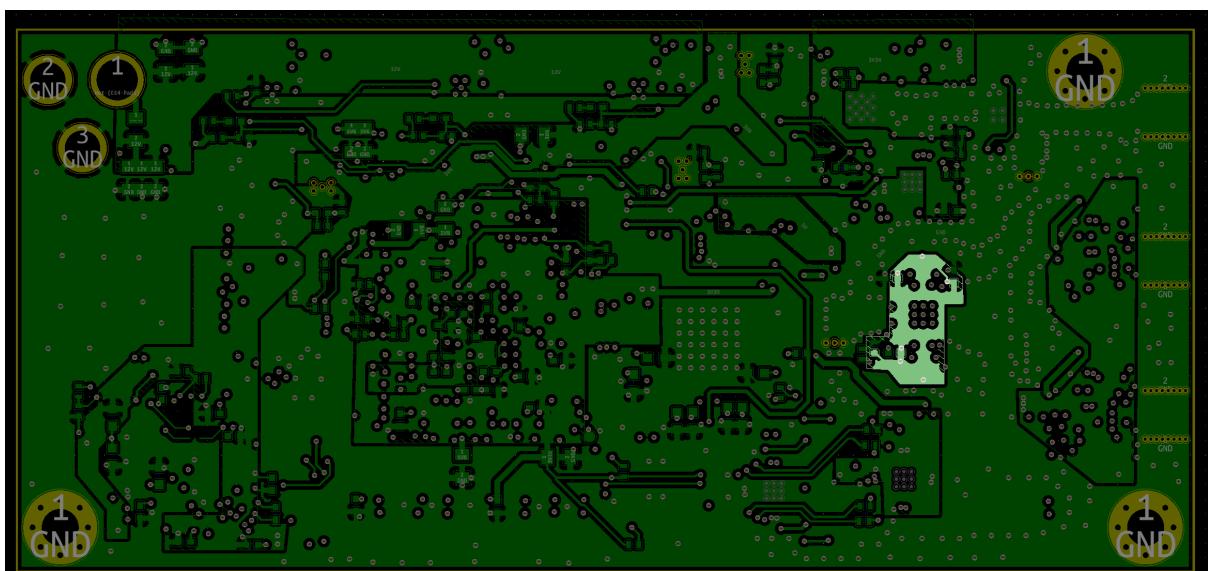


Figure 4.12: Another 5V power plane is used for to power devices after going through a ferrite bead.

# Chapter 5

## Antennas

### 5.1 Transmission

I'm using the [Triple Feed Patch Array antenna designed by Maarten Baert](#) for transmission. Although I'd eventually like to simulate and design my own antenna, this antenna is cheap, has fairly high gain (14dBi), has a radiation efficiency of about 75% and has almost nonexistent side-lobes. It's also undergone [testing at the Antenna Test Lab](#).

### 5.2 Reception

For reception, I'm using the patch array designed by Henrik Forstén. Again, I'd like to design and build my own antenna. However, Henrik's design is cheap and uses the proper spacing to allow beamforming.

# **Chapter 6**

## **Software**

### **6.1 OpenOCD**

OpenOCD is used to program the FPGA and flash.

### **6.2 LibFTDI**

LibFTDI is used to configure the FPGA and other components from the PC.

# Appendices

# Appendix A

## Pinouts

### A.1 ADF4158

Table A.1: All ADF4158 pin connections.

PIN	Mnemonic	DESCRIPTION
1	CPGND	The charge pump ground, which we set to the same ground as the rest of the circuit.
2, 3	AGND	Prescaler ground; also set to common ground.
4	RF <sub>IN</sub> B	The complement to the VCO output. We couple this to ground with a small capacitor: in this case, 10pF.
5	RF <sub>IN</sub> A	The VCO output. This goes through prescaling and then becomes the PLL input signal.
6, 7, 8	AV <sub>DD</sub>	The positive power supply for the RF part of the PLL. This takes 3.3V.
9	REF <sub>IN</sub>	The reference input, which is our 40MHz clock signal.
10	DGND	Digital ground. This uses the common ground.
11	SDGND	$\Sigma - \Delta$ modulator ground.
12	TX <sub>DATA</sub>	This pin can be used when employing FSK or PSK to transmit data. Since we are not using this we connect this pin to the FPGA but just set the value to GND.
13	CE	We must set this pin to high in order to enable the device.
14	CLK	A clock used to synchronize register configuration.
15	DATA	Serial data input to set the configuration registers.
16	LE	This pin is brought high in order to load data into the configuration registers.
17	MUXOUT	This allows internal parameters of the ADF4158 to be read externally. We don't currently use this in our design.
18	SDV <sub>DD</sub>	Power supply pin for the $\Sigma - \Delta$ modulator. We also set this to 3.3V.
19	DV <sub>DD</sub>	Power supply pin for the digital circuitry. Also 3.3V.
20, 21	SW1, SW2	FIXME: These pins are used for the fast-locking feature, which we use in our design. The typical topologies for this are shown in Figure 3.15. However, our design does not use either of these topologies.
22	V <sub>P</sub>	The charge pump power supply, which we set to 5V.
23	R <sub>SET</sub>	This pin sets the maximum charge pump current according to the equation $I_{CPmax} = 25.5/R_{SET}$ . We use 5.49k $\Omega$ for the resistor which gives a charge pump current of 4.6mA.
24	CP	The charge pump output that is amplified and feeds into the VCO. Obviously, because this is a charge pump we need to place a bypass capacitor to ground before the amplifier. Here we use 51pF.
25	EPAD	This is connected to GND.

## A.2 FT2232H

### *FT2232H Main Section*

**Table A.2: FT2232H pinout.**

#	Pin	Type	Description
1, 5, 11, 15 16–24	GND	power input	Ground.
25, 35, 47, 51	ADBUS[0:7]	bidirectional	D0–D7 FIFO data.
26	RXF#	output	Low when there is data available in the FIFO to be read by the FPGA. High otherwise.
27	TXE#	output	Low when there is room for data to be written to the FIFO.
28	RD#	input	When driven low, this places FIFO data onto D0–D7 each CLKOUT cycle (RXF# must also be low).
29	WR#	input	When low, D0–D7 is written to the FIFO for transmission every CLKOUT cycle (TXE# must also be low).
30	SIWUA	input	Can be driven low to flush pending FIFO data over the USB port to a computer regardless of the pending packet size.
32	CLKOUT	output	60MHz signal generated on chip and used to synchronize FIFO.
33	OE#	input	Output enable that must be driven low at least 1 period before driving RD# low to read data from FIFO.

## A.3 LTC2292

### *LTC2292 Main Section*

**Table A.3: LTC2292 pinout.**

#	Pin	Description
1–2, 15–16	AINA+, AINA-, AINB-, AINB+	The differential inputs for channels A and B. The input filters are explained in § 3.5.2.
3–6, 11–14	REFHA, REFLA, REFLB, REFHB	These are the high and low reference for channels A and B, respectively. Their connection is specified exactly by the datasheet.
7, 10, 18, 63	VDD	3.0V power supply.
8, 9, 21	CLKA, CLKB, MUX	40MHz clock inputs for channels A and B. Connecting the clock pins together with MUX multiplexes channels A and B together and causes the multiplexed output to be available on buses A and B. Fig. 3.10 shows the timing diagram for the multiplexed output. Since we only need one set of the identical signals, bus B is left floating.
17, 64, 65, 31, 50	GND, OGND	ADC, output and power grounds are all connected to the same ground plane.
39, 42	OVDD	Power supply for the output drivers.
43–48, 51–56	DA0–DA11	Digitized 12-bit output data.
57	OFA	Driven high when overflow or underflow occurs. This is fed to the FPGA to allow overflow/underflow detection.

26–30,	33–	DB0–DB11	The channel B data bus. Left floating (see description for CLKA, CLKB, MUX).
39		OFB	Similar to OFA, but for channel B. Also exported to the FPGA.
40		VCMA, VCMB	Exports a 1.5V signal to the IF differential amplifiers, which use it to set their common mode voltage. The $2.2\mu\text{F}$ capacitors are specified by the datasheet.
61, 20		NC	No connect.
24–25,	41–	NC	
42			
59, 22, 58,	SHDNA, SHDNB,		Allow the FPGA to control the ADC's operation. Pulling SHDNA and OEA low operates channel A normally, while bringing them both high puts channel A in sleep mode. Channel B works the same way.
23	OEA, OEB		
62, 19	SENSEA,		Tied to VDD, which specifies that the input voltage range of the differential signals for channels A and B is $1.5\text{V} \pm 1\text{V}$ (i.e. $1.5\text{V}$ common-mode voltage with a $2\text{V}$ range).
	SENSEB		
60	MODE		Tied to VDD, which specifies the output format as 2s complement and turns off the clock duty stabilizer, which should be unnecessary because the input clock has a 50% duty cycle.

## A.4 XC7A15T-FTG256

### *XC7A15T-FTG256 Main Section*

The FPGA pin names follow a logical syntax: they can be of the form IO\_LXXY\_ZZZ\_#, IO\_XX\_ZZZ\_#, or a specific name. If they have a specific name, they have a dedicated function described starting on page 26 of the package-pinout document. If they have the general form IO\_LXXY\_ZZZ\_# or IO\_XX\_ZZZ\_#, they can be used for several different dedicated functions, or as general purpose IO pins. L indicates that the pin can be used as a differential pair (differential signaling), where Y=P or N depending on whether the pin is the positive or negative side of the differential pair. XX gives a unique number identifier that can be used to associate the two different pins forming a differential pair. ZZZ represents one or more functions that the pin can be used for in addition to general purpose IO. # indicates the bank number, which separate the pins into one of several different regions. The package used in this design is FTG256C, which contains banks 0, 14, 15, 34 and 35. Bank 0 contains the dedicated configuration pins. Each bank has 4 pairs of clock capable inputs for differential or single ended clocks (there are no global clock pins).

**Table A.4: FPGA pinout. Displayed in alphanumeric order.**

Pin	Description
A01	GND.
A02	Connected to an external 1x1 pin header that is currently unused by FPGA logic.
A03	Connected to external 2x4 pin header that is currently unused by FPGA logic.
A04	Connected to same pin header as A03. Also unused.
A05	Same.
A06	One of the voltage supplies for bank 35. It uses 3.3V as with all the other voltage supplies to the main banks of the FPGA.
A07	Connected to same pin header as A03. Unused.
A08	A different 2x4 pin header. Unused.
A09	Connected to the same pin header as A08. Unused.
A10	Floating.
A11	GND.

A12	Connected as an output to the FT2232H USB-JTAG converter. Pulling this low allows the FT2232H device to output data to the FPGA through the ADBUS pins. Driving it high sets the ADBUS pins as inputs. Remember, the ADBUS pins serve as the bidirectional translation between JTAG data and USB data.
A13	SIWU (channel A). This pin is output to the FT2232H device and can be used to optimize USB data transfers (more info in the FT2232H datasheet). It is not currently used by the FPGA logic.
A14	Write output pin to the FT2232H device. When this is driven low, the FPGA writes data to the FT2232H. When it's driven high, the FPGA can perform a read from the FT2232H.
A15	Inputs a 60MHz clock signal that originated at the FT2232H. This clock is used to synchronize all data transfers between the FPGA and the FT2232H.
A16	A 3.3V input to bank 15.
B01	ADC_SHDN1. One of two ADC_SHDN outputs that, together with OEA (B02), controls the shutdown mode selection of the ADC. It is used by the digital FPGA logic. When both SHDN and OE are grounded, the ADC performs normally. When they are both pulled high, the ADC goes into sleep mode. There are two other states but they are not used by the FPGA logic.
B02	ADC_OE1. See pin B01. This is used for channel A.
B03	3.3V input for bank 35.
B04	Floating.
B05	Connected to the same 2x4 pin header as A03. Unused.
B06	Floating.
B07	Connected to the same 2x4 pin header as A03. Unused.
B08	GND.
B09	Connected to the same pin header as A08. Unused.
B10	Connected to the same pin header as A08. Unused.
B11	Floating.
B12	Floating.
B13	3.3V input for bank 15.
B14	RD#. A read active-low output pin to the FT2232H device. When this is driven low, the FPGA reads data from the FT2232H.
B15	TXE#. An active-low input from the FT2232H. FT2232H drives this pin low to signal sending data to the FPGA (i.e. a read for the FPGA).
B16	RXF#. An active-low input from the FT2232H. FT2232H drives this pin low to signal that it should read data. To the FPGA, this signals that it should write data.
C01	Floating.
C02	OF1. An input from the ADC. It is pulled high when an overflow or underflow occurs at channel A. It is currently unused by the FPGA logic.
C03	Floating.
C04	Floating.
C05	GND.
C06	Floating.
C07	Floating.
C08	Floating.
C09	Floating.
C10	3.3V input to bank 15.
C11	Connected to the same pin header as A08. Unused.
C12	Connected to the same pin header as A08. Unused.
C13	Floating.
C14	Floating.
C15	GND.
C16	FT_SUSPEND. An active-low input to the FPGA. FT223H drives this low when the USB is in suspend mode. It is currently unused by the FPGA logic.
D01	LED. Connects to an LED that is used by the FPGA to signal data processing.
D02	GND.

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D03	Floating.
D04	Floating.
D05	Floating.
D06	Floating.
D07	3.3V input to bank 35.
D08	Floating.
D09	Floating.
D10	Floating.
D11	Floating.
D12	GND.
D13	Floating.
D14	Floating.
D15	FT_D7. Bidirectional pin 7/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
D16	FT_D6. Bidirectional pin 6/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
E01	D10. Input pin 10/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
E02	D11. Input pin 11/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
E03	Floating.
E04	3.3V input to bank 35.
E05	Floating.
E06	Floating.
E07	CFGPVS_0. A dedicated pin that is part of the configuration logic of the FPGA. It is used to specify the voltage level used for all banks. Since we use 3.3V, we connect this pin to the same 3.3V voltage level.
E08	CCLK_0. An output pin exported from the FPGA to the flash memory device, W25Q32JV, to drive its operation and coordinate writes and reads to and from the device.
E09	GND.
E10	VCCBRAM. One of the two power supply pins to the FPGA's internal RAM. It requires 1.0V.
E11	Floating.
E12	Floating.
E13	Floating.
E14	3.3V power supply to bank 15.
E15	FT_D5. Bidirectional pin 5/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
E16	FT_D4. Bidirectional pin 4/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
F01	VCC0.35. 3.3V power supply to bank 35.
F02	D9. Input pin 9/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
F03	Floating.
F04	Floating.
F05	Floating.
F06	GND.
F07	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
F08	VCCBATT_0. Can be used for memory backup. We do not use it so we tie it to GND.
F09	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
F10	GND.
F11	VCCBRAM. One of the two power supply pins to the FPGA's internal RAM. It requires 1.0V.
F12	Floating.
F13	Floating.
F14	FT_D3. Bidirectional pin 3/7 of ADBUS, used to transmit data between the FPGA and FT2232H.

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F15	FT_D0. Bidirectional pin 0/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
F16	GND.
G01	D10. Input pin 10/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
G02	D7. Input pin 7/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
G03	GND.
G04	Floating.
G05	Floating.
G06	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
G07	GNDADC_0. The reference voltage for the onchip ADC.
G08	VCCADC_0. A 1.8V power supply used to power the onchip ADC.
G09	GND.
G10	VCCAUX. A 1.8V power supply for auxiliary circuits in the FPGA IC.
G11	Floating.
G12	Floating.
G13	GND.
G14	Floating.
G15	FT_D2. Bidirectional pin 2/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
G16	FT_D1. Bidirectional pin 1/7 of ADBUS, used to transmit data between the FPGA and FT2232H.
H01	D4. Input pin 4/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
H02	D5. Input pin 5/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
H03	D6. Input pin 6/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
H04	Floating.
H05	Floating.
H06	GND.
H07	VREFN_0. A dedicated pin that is used as a 1.25V reference GND voltage. Tied to GND.
H08	VP_0. A dedicated pin that is used as the XADC differential analog input (positive side). It is left floating and is unused.
H09	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
H10	DONE_0. A bidirectional dedicated pin. It is pulled high when configuration is done. It is connected to a pull-up resistor and an external connector, presumably for debugging purposes.
H11	Floating.
H12	Floating.
H13	Floating.
H14	Floating.
H15	VCC0_15. 3.3V power supply for bank 15.
H16	CARD_DETECT. Connects to the SD card. Currently unused by FPGA logic.
J01	Floating.
J02	VCC0_35. 3.3V power supply for bank 35.
J03	D3. Input pin 3/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
J04	MIX_ENBL. An enable pin that is output to the ADL5802 mixer. It is pulled low to enable the mixer and pulled high to disable it.
J05	Floating.
J06	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
J07	VN_0. A dedicated pin that is used as the XADC differential analog input (negative side). It is tied to GND and is unused.

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J08	VREFP_0. A dedicated pin that is used as a 1.25V reference input. It is tied to GND and unused.
J09	GND.
J10	VCCAUX. A 1.8V power supply for auxiliary circuits in the FPGA IC.
J11	GND.
J12	VCC0_15. 3.3V power supply for bank 15.
J13	SPI_MOSI. Used by the FPGA to send data to the flash memory device.
J14	SPI_DIN. Used by the FPGA to read data from the flash memory device.
J15	Floating.
J16	Floating.
K01	D2. Input pin 2/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
K02	D1. Input pin 1/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
K03	ADF_MUXOUT. Input from the frequency synthesizer. It indicates that a sweep is done.
K04	GND.
K05	Floating.
K06	GND.
K07	DXN_0. The cathode of two temperature-monitoring diode pins. It is not used and is therefore tied to GND.
K08	DXP_0. The anode of two temperature-monitoring diode pins. It is not used and is therefore tied to GND.
K09	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
K10	INIT_B. Indicates initialization of configuration memory. It is pulled high and is unused.
K11	VCCAUX. A 1.8V power supply for auxiliary circuits in the FPGA IC.
K12	Floating.
K13	Floating.
K14	GND.
K15	Floating.
K16	Floating.
L01	GND.
L02	D0. Input pin 0/11 of the ADC's channel A digital outputs. It is used to transmit data from the ADC to FPGA.
L03	Floating.
L04	Floating.
L05	Floating.
L06	VCC0_0. 3.3V power supply for bank 0 (i.e. the bank for dedicated configuration pins).
L07	TCK. An input pin originating at the output of FT2232H and is used to transmit the JTAG clock. It is not used by the FPGA logic.
L08	VCCINT. 1.0V power supply for the internal core logic of the FPGA.
L09	PROGRAM_B. Connected to a pushbutton switch and can be used to perform an asynchronous reset of the configuration logic.
L10	VCCAUX. A 1.8V power supply for auxiliary circuits in the FPGA IC.
L11	GND.
L12	SPI_CS. An output pin that can be brought low to indicate that a transmission will take place between the FPGA and flash storage device. It is currently left in the high-impedance state in FPGA logic, seemingly indicating that the flash storage device is not yet used.
L13	Floating.
L14	Floating.
L15	PUDC_B. Pulled low, which configures all I/O pins to enable their internal pull-up resistors.
L16	VCC0_14. 3.3V power supply to bank 14.
M01	OF2. An input from the ADC. It is pulled high when an overflow or underflow occurs at channel B. It is currently unused by the FPGA logic.
M02	ADF_DATA. A serial data output pin the frequency synthesizer.

M03	VCC0_34. 3.3V power supply to bank 34.
M04	Floating.
M05	Floating.
M06	Floating.
M07	TMS. Output pin that is fed into the FT223H as a mode select pin. It is unused by the current FPGA logic.
M08	GND.
M09	M0. Along with M1 and M2, this specifies the configuration mode of the FPGA. M[2:0] = 001 which indicates the FPGA acts as a master in an SPI interface. Because a DNP resistor is placed between M0 and 3.3V, it is not actually connected to the power supply. However, since all pull-up resistors should be enabled by pulling PUDC.B low, it should register a logic 1.
M10	M1. See M09.
M11	M2. See M09.
M12	Floating.
M13	VCC0_14. 3.3V power supply to bank 14.
M14	Floating.
M15	Floating.
M16	SD_DAT1. A data line to the SD card reader. Not currently used by the FPGA logic.
N01	ADF_LE. An output that connects to the ADF4158 frequency synthesizer. When it is pulled high, data stored in the ADF4158 shift registers is loaded into one of the 8 latches.
N02	ADC_SHDN2. See B01.
N03	Floating.
N04	Floating.
N05	GND.
N06	Floating.
N07	TDI. JTAG data input from FT2232H. It is not currently used by the FPGA logic.
N08	TDO. JTAG data output to FT2232H. It is not currently used by the FPGA logic.
N09	Floating.
N10	VCC0_14. 3.3V power supply for bank 14.
N11	CLK_REF. An input pin that takes the main 40MHz reference clock used by the FPGA. It is one of the outputs of the clock fanout buffer.
N12	Floating.
N13	Floating.
N14	SD_CLK. A clock that synchronizes activity with the SD card reader. It is not currently used by the FPGA logic.
N15	GND.
N16	SD_DAT0. A data line to the SD card reader. Not currently used by the FPGA logic.
P01	ADC_OE2. See pin B01. This is used for channel B.
P02	GND.
P03	ADF_TXDATA. Output pin that transmits data to be used by the ADF4158 frequency synthesizer for FSK or PSK transmission. This is unused by the FPGA logic.
P04	Floating.
P05	Floating.
P06	Floating.
P07	VCC0_14. 3.3V power supply for bank 14.
P08	Floating.
P09	Floating.
P10	Floating.
P11	Floating.
P12	GND.
P13	Floating.
P14	Floating.
P15	Floating.

P16 SD\_CMD. A pin used to communicate with the SD card reader. Currently unused by the FPGA logic.

---

R01 ADF\_CLK. An output clock used to synchronize the operation of the ADF4158 frequency synthesizer.

R02 Floating.

R03 ADF\_CE. An output pin to the ADF4158. When this pin is driven low, it powers down the frequency synthesizer.

R04 VCC0\_34. 3.3V power supply for bank 34.

R05 Floating.

R06 Floating.

R07 Floating.

R08 Floating.

R09 GND.

R10 Floating.

R11 Floating.

R12 Floating.

R13 Floating.

R14 VCC0\_14. 3.3V power supply for bank 14.

R15 SD\_DAT3. A data line to the SD card reader. Not currently used by the FPGA logic.

R16 SD\_DAT2. A data line to the SD card reader. Not currently used by the FPGA logic.

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T01 VCC0\_34. 3.3V power supply for bank 34.

T02 PA\_OFF. Output pin that connects to the base of a transistor and can be used to enable (high) or disable (low) the operation of the power amplifier, SE2567L.

T03 Floating.

T04 ADF\_DONE. Input pin that is unused by the FPGA logic.

T05 Floating.

T06 GND.

T07 Floating.

T08 Floating.

T09 Floating.

T10 Floating.

T11 VCC0\_14. 3.3V power supply for bank 14.

T12 Floating.

T13 Floating.

T14 Floating.

T15 Floating.

T16 GND.

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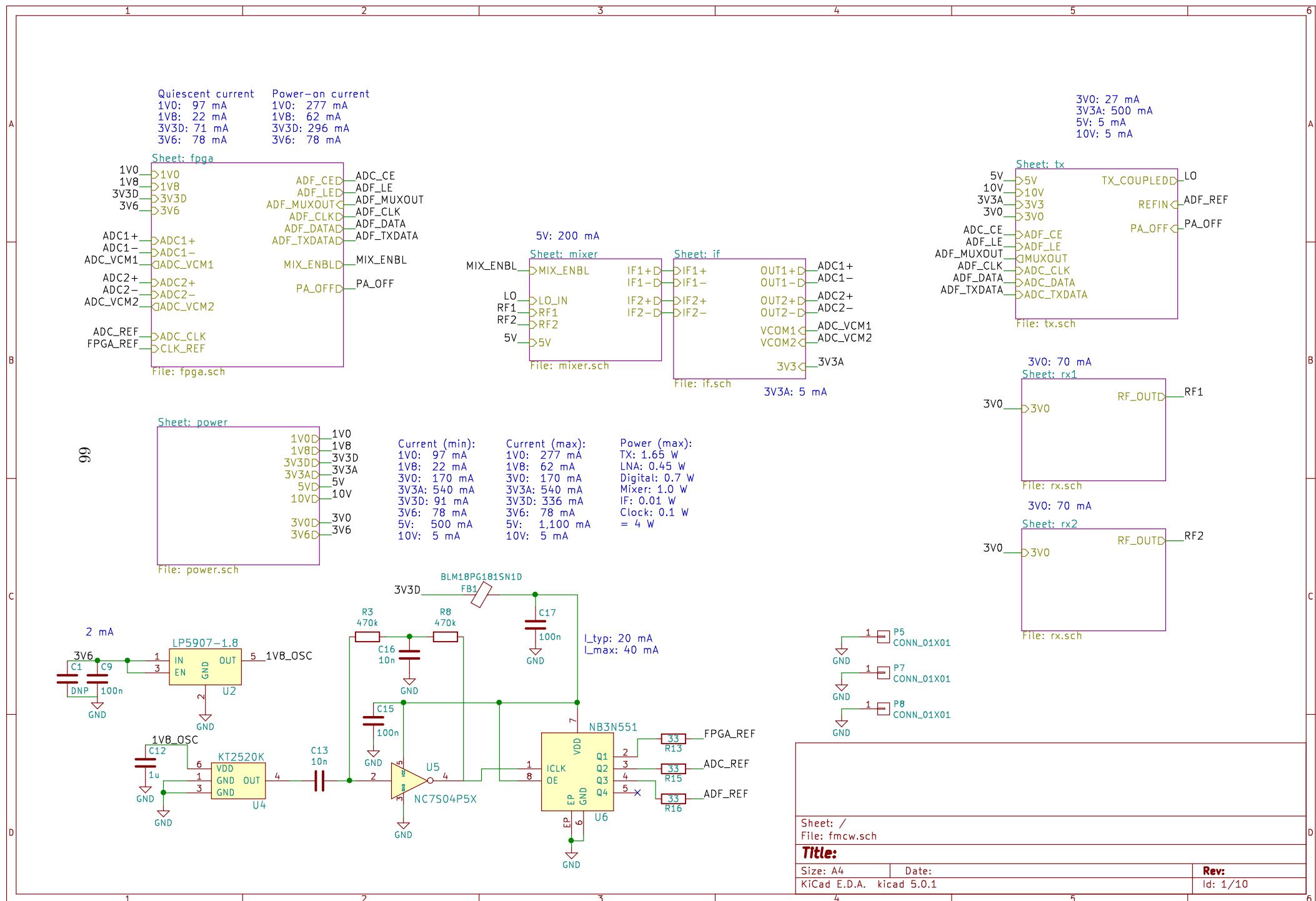
PROGRAM\_B\_0 is connected to a pushbutton switch and can be used to perform an asynchronous reset to the configuration logic. TDI, TDO, TMS, and TCK are used for the JTAG clock, data input, data output, and mode select, respectively. They are connected to the FT2232H IC that translates between USB signals and JTAG signals. They are used to configure the FPGA (which is also stored in the flash memory). M[2:0] specify the configuration mode for the FPGA. In our configuration, M0 is pulled high while the other 2 are pulled low, indicating a Master SPI interface. CFGBVS\_0 is used to specify the voltage level used for all banks. Since we use 3.3V, we connect this pin to the same 3.3V. The PUDC\_B pin is pulled low, which configures all I/O pins to enable their internal pull-up resistors. There is an SD card reader connected up to the FPGA, however, it is unused by the current FPGA code. VCCAUX is used for auxiliary circuits and must be 1.8V. VCCADC\_0 is also 1.8V and is used to power the on chip ADC. VCCINT powers the internal core logic of the FPGA and must be 1.0V. VCCBRAM is the power supply for the FPGA internal RAM, which requires 1.0V.

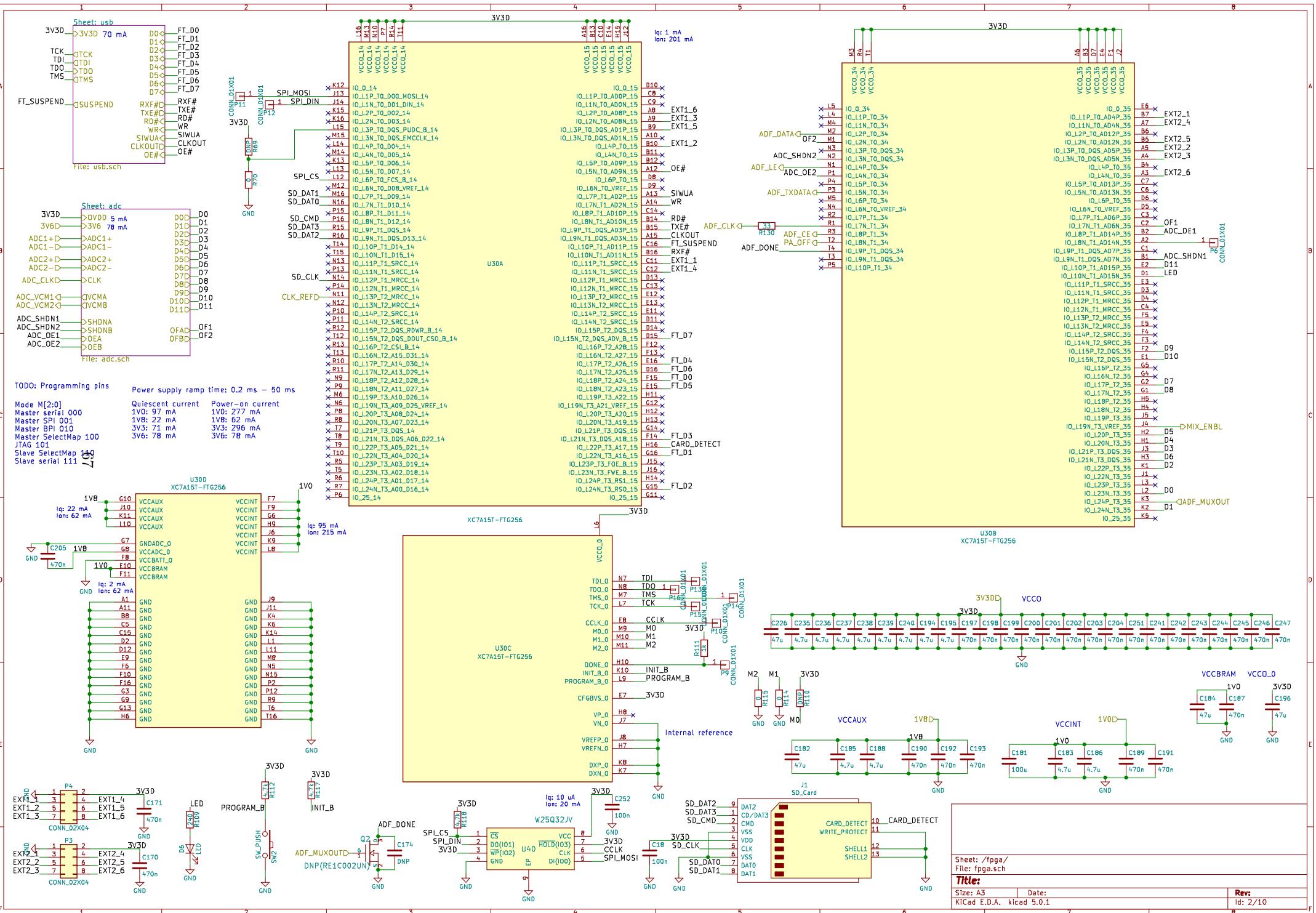
## **Appendix B**

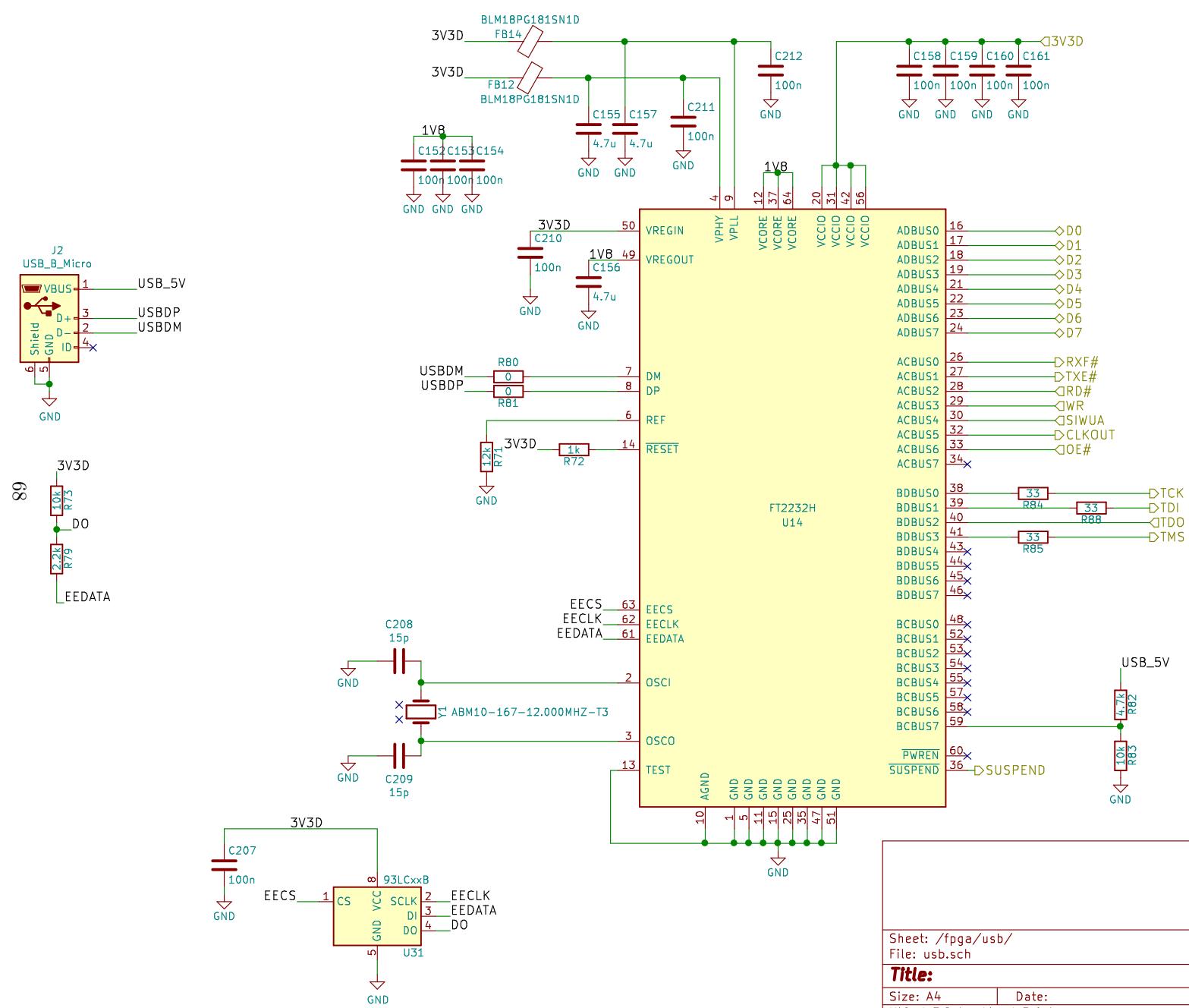
### **Links**

## **Appendix C**

### **Full Schematic**





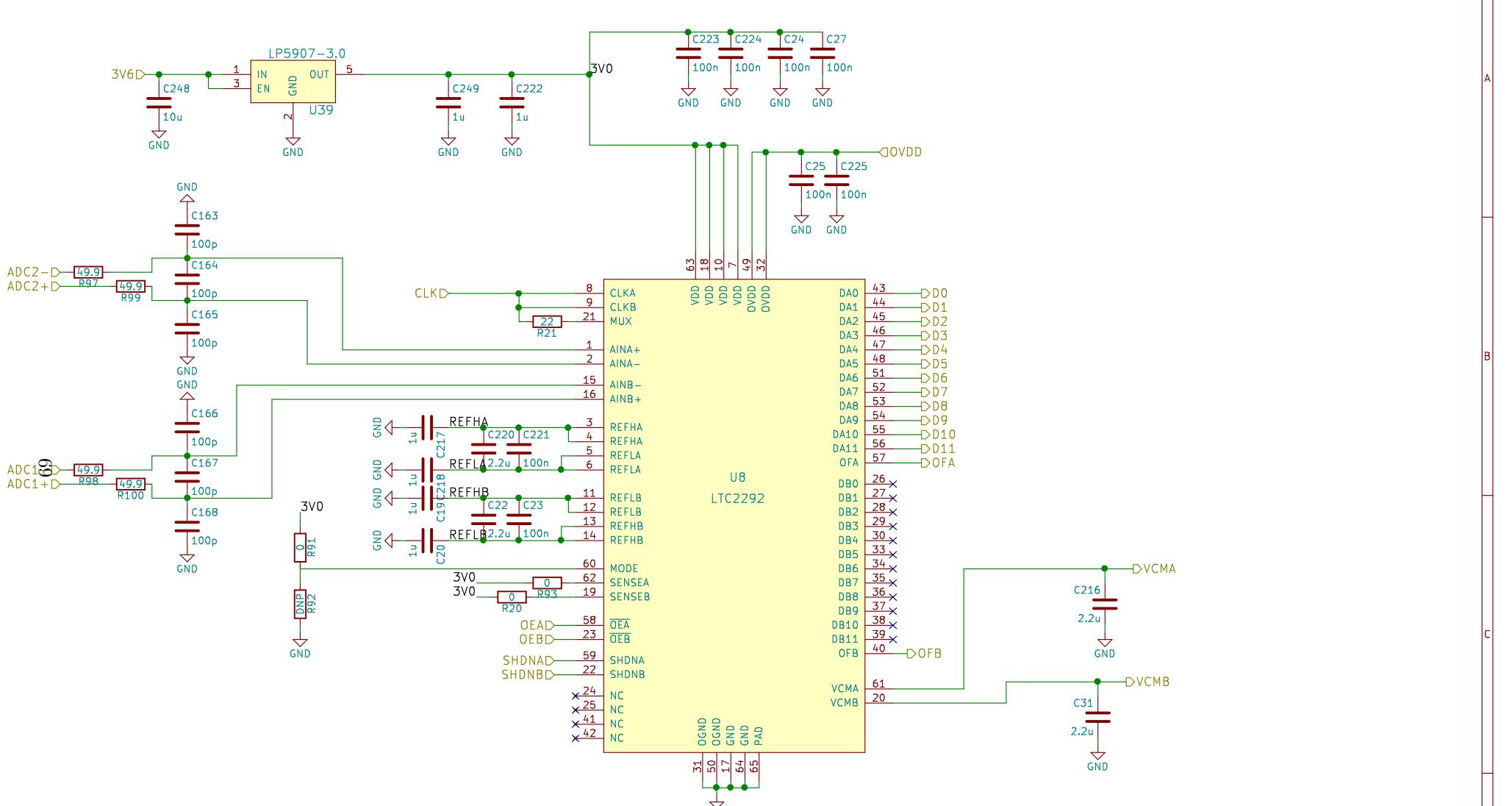


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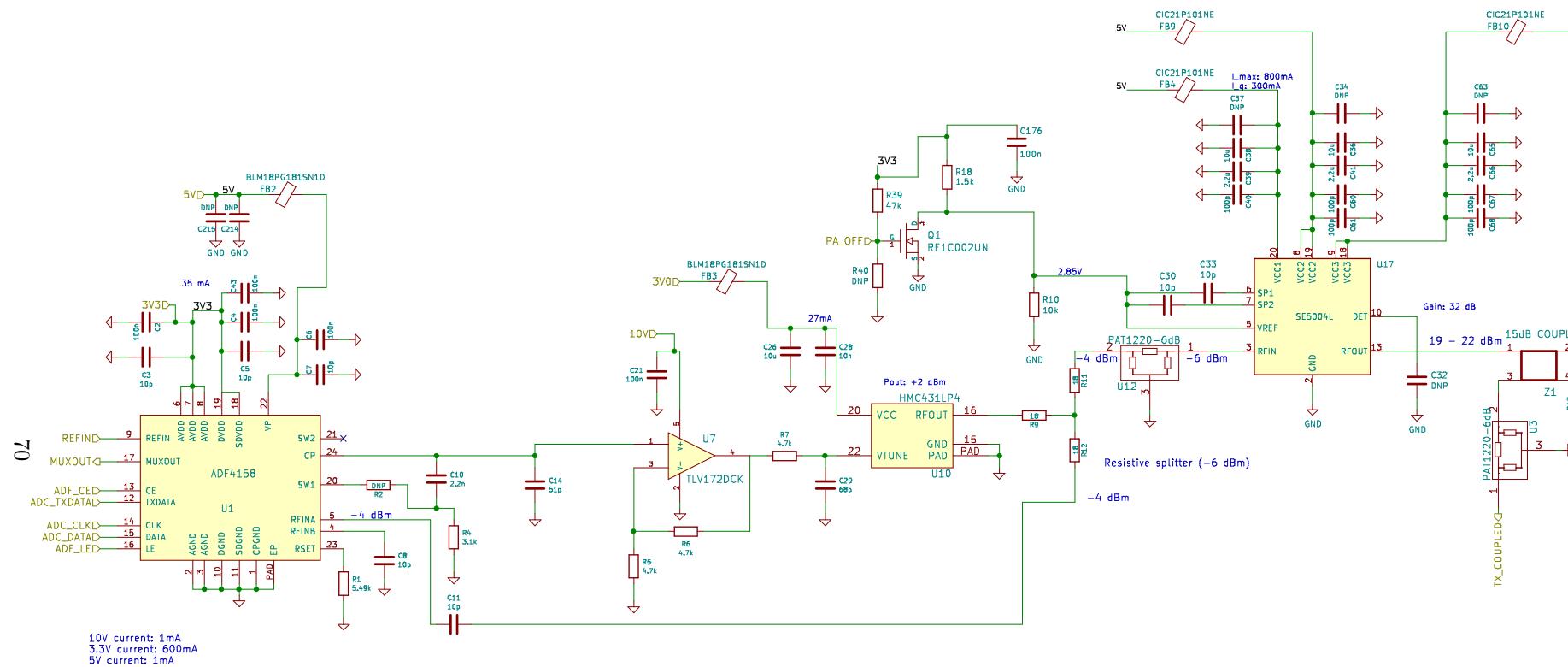


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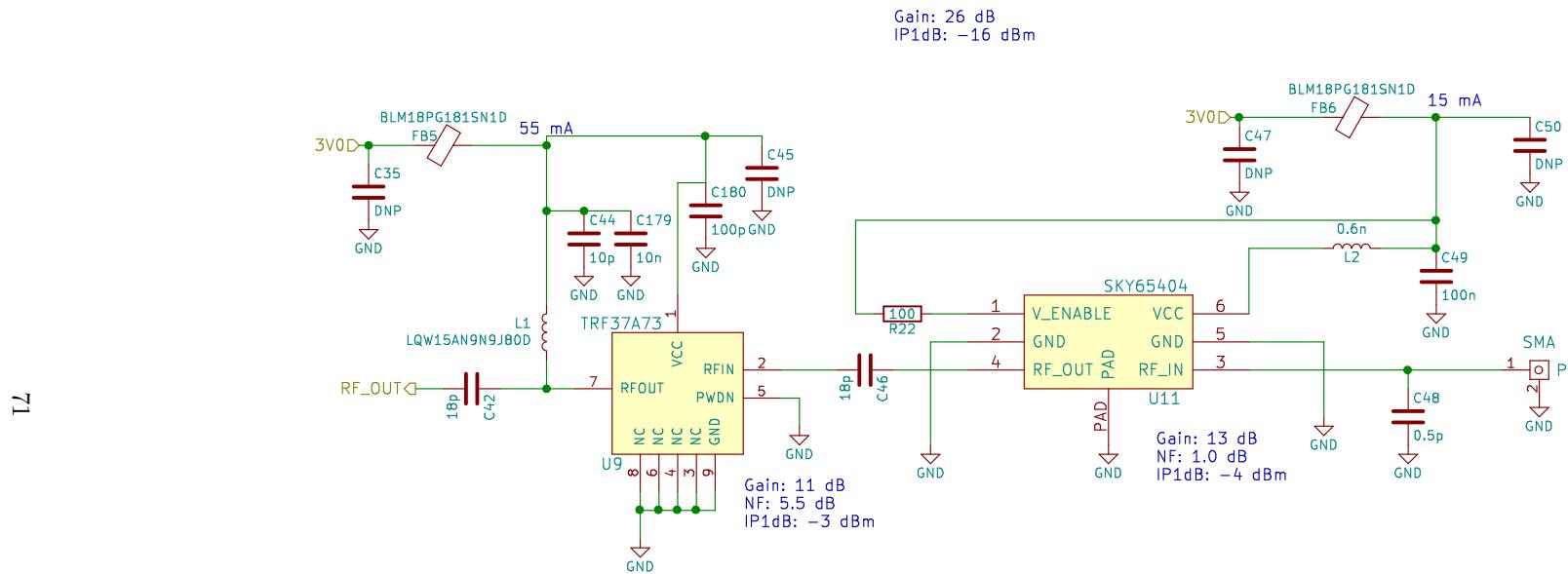
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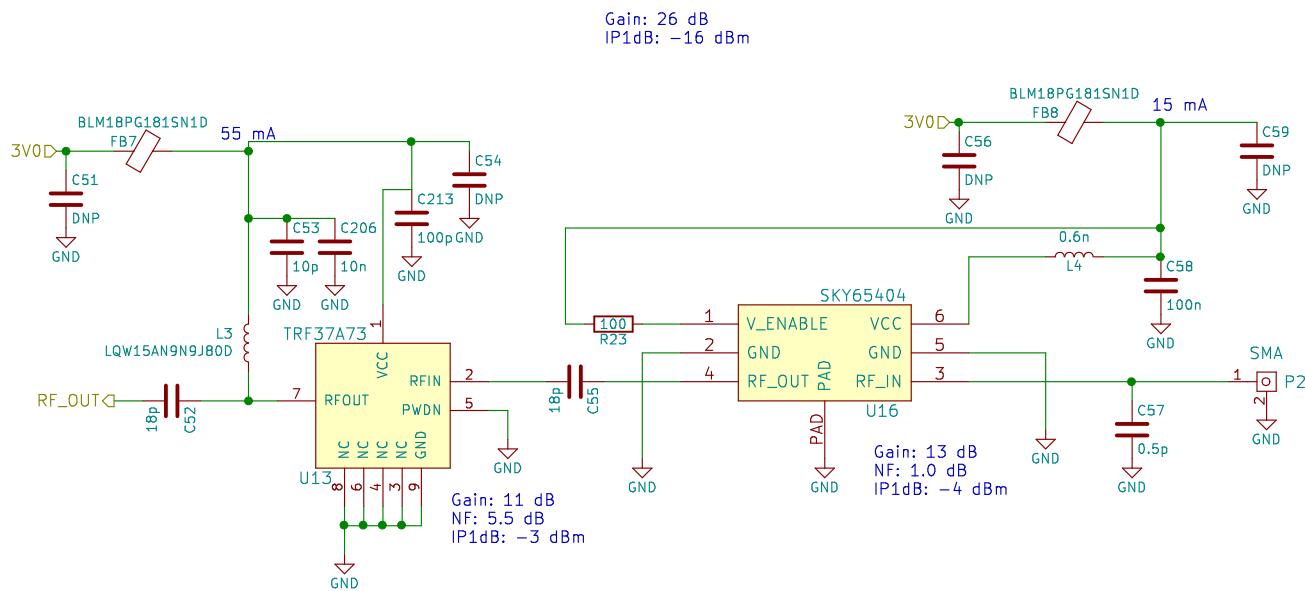
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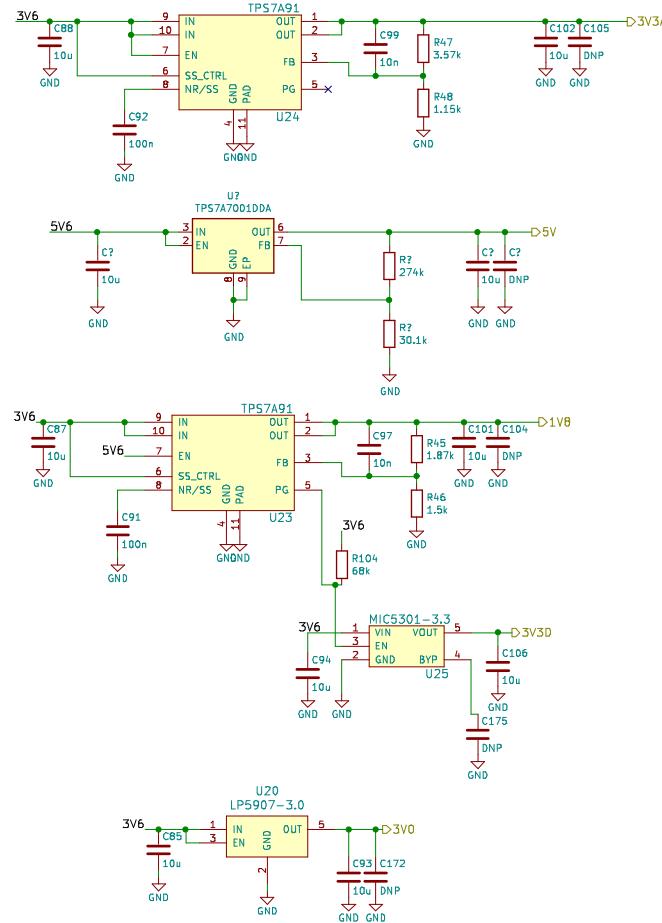
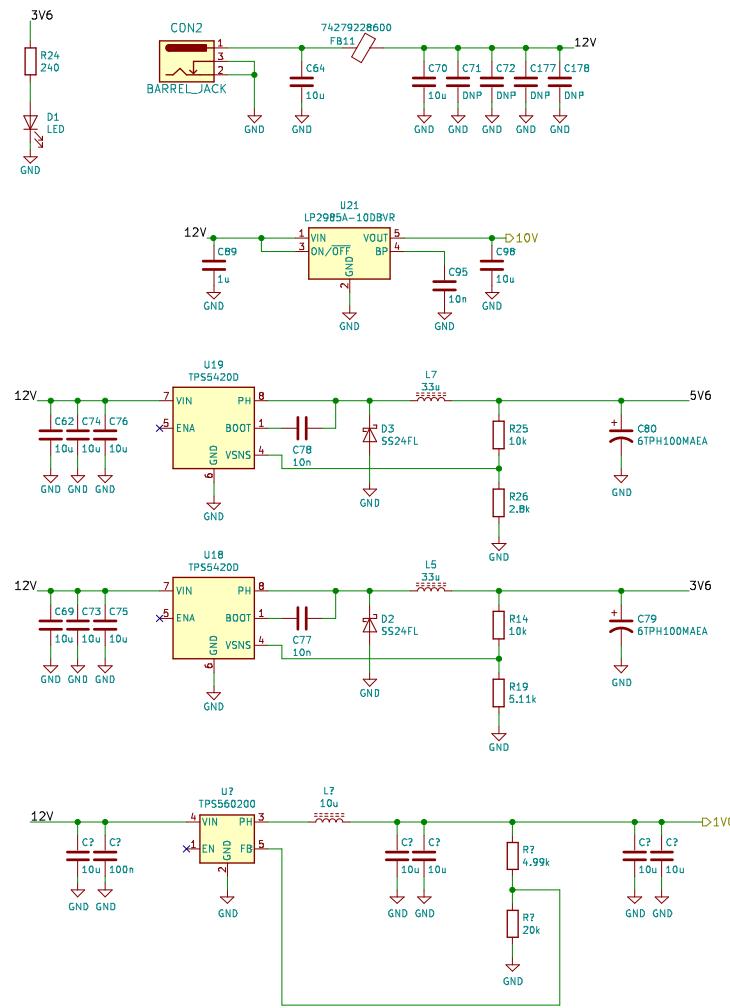
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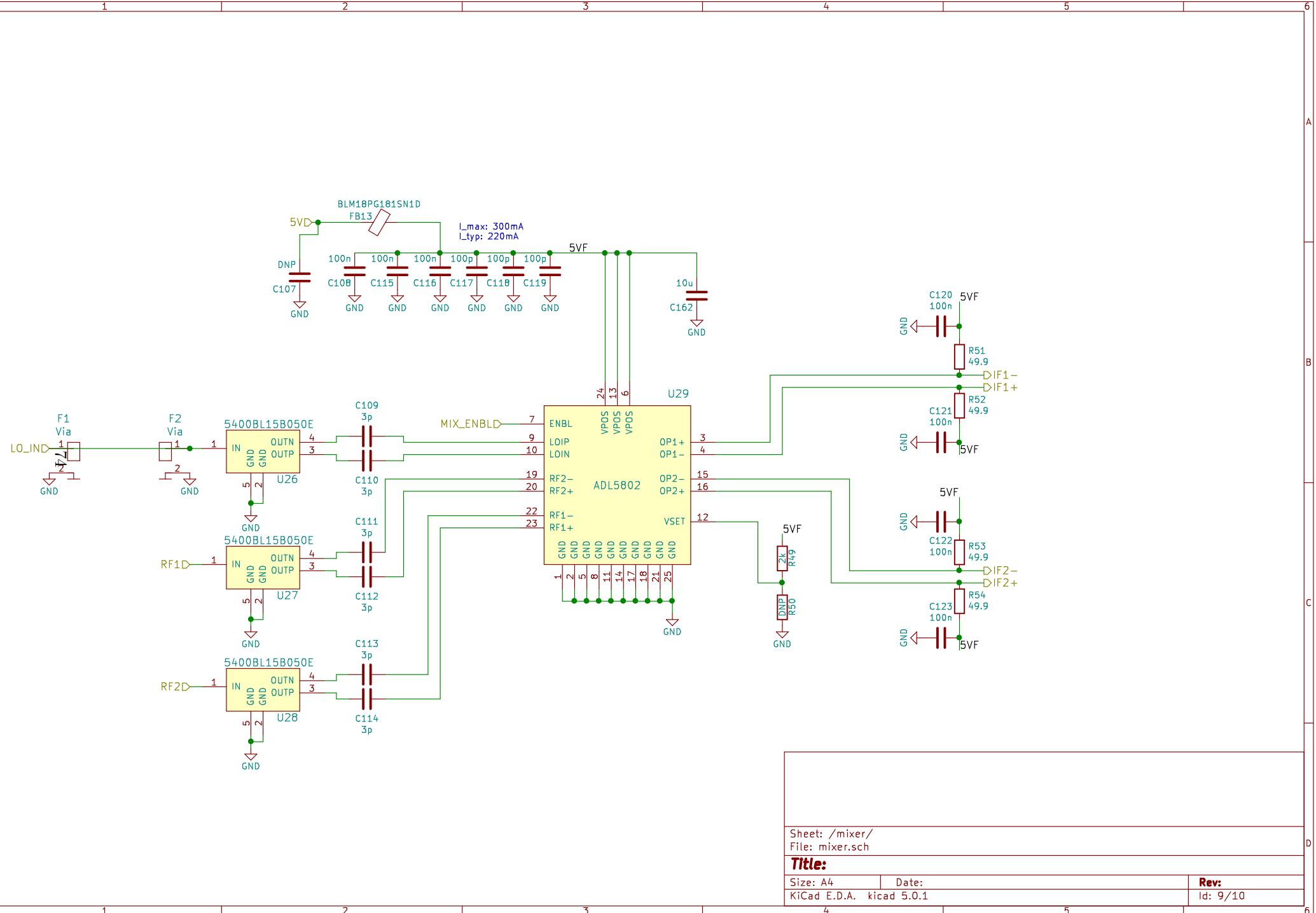
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KiCad E.D.A. kicad 5.0.1

Rev:  
Id: 7/10

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KiCad E.D.A. kicad 5.0.1	Rev: 8/10



Sheet: /mixer/  
File: mixer.sch

**Title:**

Size: A4 Date:  
KiCad E.D.A. kicad 5.0.1

Rev:  
Id: 9/10

