An Updated Emulated Architecture to Support the Study of Operating Systems

µMPS3

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27 Maggio 2020

The µMPS Project

What

An educational computer system architecture based around the MIPS R2/3000 microprocessor featuring

- a front-end emulator
- a set of I/O devices

When

1999	MPS
2004	µMPS
2011	µMPS2
2020	**µMPS3**

Where

Created

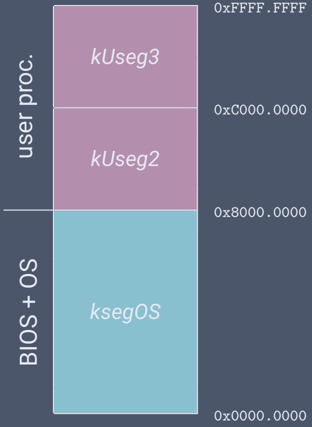
- University of Bologna
- Xavier University

Used

- all around the world

Address Space

µMPS2



user proc.

BIOS + OS

kUseg3

kUseg2

ksegOS

0xFFFF.FFFF

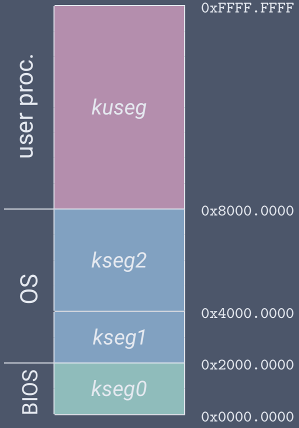
0xC000.0000

0x8000.0000

0x0000.0000

- Memory segmentation

µMPS3



user proc.

OS

BIOS

kuseg

kseg2

kseg1

kseg0

0xFFFF.FFFF

0x8000.0000

0x4000.0000

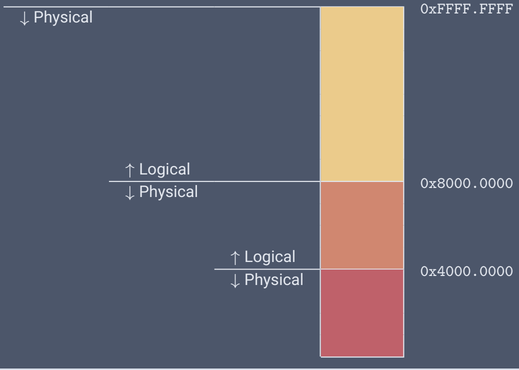
0x2000.0000

0x0000.0000

- Memory partitioning

Address Translation

TLB Floor Address



Possible options

- `0x4000.0000`
- `0x8000.0000`
- `VM OFF` (`0xFFFF.FFFF`)

Consequences

- *VM bit* removed

Mode of operation

Addresses below *TLB Floor Address* ↓

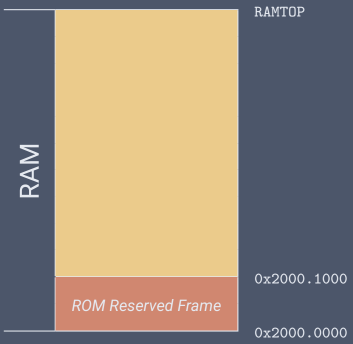
- considered physical
- exempt from address translation

Addresses above *TLB Floor Address* ↑

- considered logical
- subject to address translation

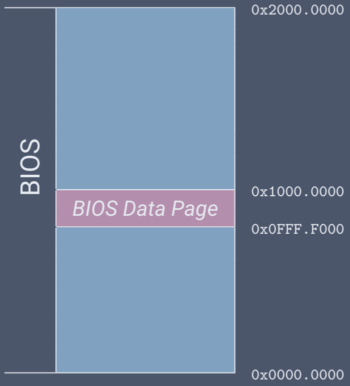
Exception Handling (1)

µMPS2 - ROM Reserved Frame



- space for just one processor state
- page table (memory segmentation)
- reentrant ROM (BIOS) handlers

µMPS3 - BIOS Data Page



- space for all 16 processors states
- different BIOS handlers per CPU

Exception Handling (2)

BIOS Data Page

0x1000.0000

0x0FFF.FA00

16× Pass Up Vectors

0x0FFF.F900

0x0FFF.F8C0

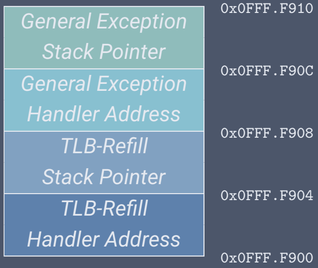
16× Processors States

0x0FFF.F000

Exceptions Types

- *general* exceptions
- *TLB-Refill* exceptions

Pass Up Vector



General Exception Stack Pointer 0x0FFF.F910

General Exception Handler Address 0x0FFF.F90C

TLB-Refill Stack Pointer 0x0FFF.F908

TLB-Refill Handler Address 0x0FFF.F904

0x0FFF.F900

Processors Initialization

Flash Device

Building Process

Graphical User Interface