

An Updated Emulated Architecture to Support the Study of Operating Systems

μMPS3

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What

An educational computer system architecture based around the MIPS R2/3000 microprocessor featuring

- ▶ a front-end emulator
- ▶ a set of I/O devices

When

- ▶ 1999 MPS
- ▶ 2004 μ MPS
- ▶ 2011 μ MPS2
- ▶ 2020 μ MPS3

Where

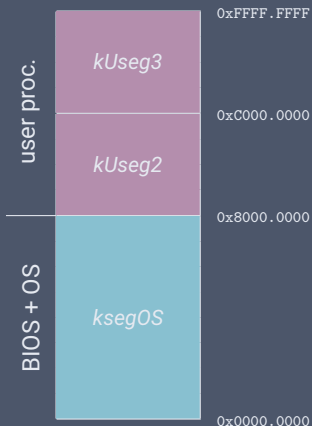
Created

- ▶ University of Bologna
- ▶ Xavier University

Used

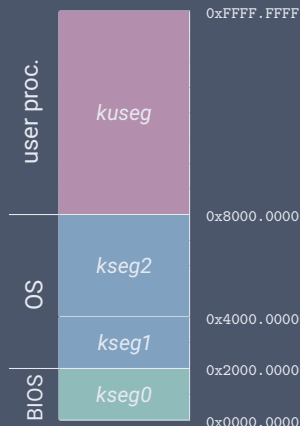
- ▶ all around the world

μMPS2



► Memory segmentation

μMPS3



► Memory partitioning

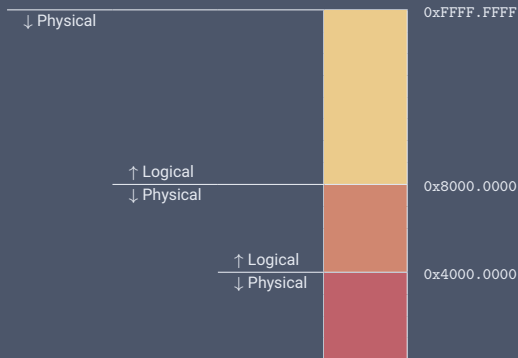
TLB Floor Address

Possible options

- ▶ 0x4000.0000
- ▶ 0x8000.0000
- ▶ VM OFF (0xFFFF.FFFF)

Consequences

- ▶ *VM bit* removed



Mode of operation

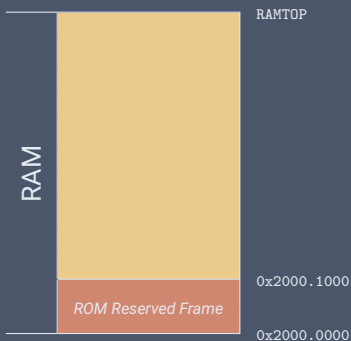
Addresses below *TLB Floor Address* ↓

- ▶ considered physical
- ▶ exempt from address translation

Addresses above *TLB Floor Address* ↑

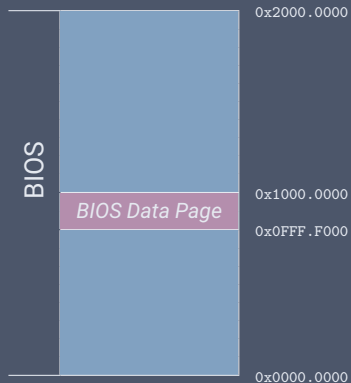
- ▶ considered logical
- ▶ subject to address translation

μMPS2 - ROM Reserved Frame



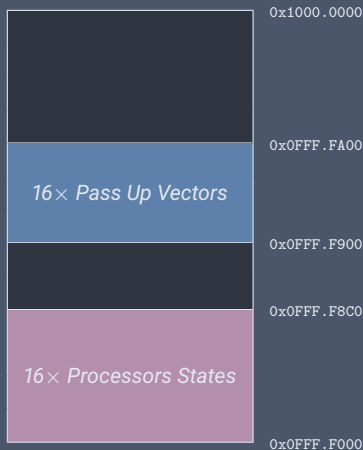
- ▶ space for just one processor state
- ▶ page table (memory segmentation)
- ▶ reentrant ROM (BIOS) handlers

μMPS3 - BIOS Data Page



- ▶ space for all 16 processors states
- ▶ different BIOS handlers per CPU

BIOS Data Page



Exceptions Types

- ▶ *general* exceptions
- ▶ *TLB-Refill* exceptions

Pass Up Vector

