# Intro to Side-Channel Analysis: Concepts and Techniques

## (AI-assisted) side-channel attacks on real-world crypto implementations

## Hardwear.io 2024 (Amsterdam) training, Lecture 1, Day 1

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October 21, 2024

# Training schedule

- Day 1: Intro to Side-channel attacks
  - Lecture: Side-channel attacks on crypto implementations
  - Two Assignments
- Day 2: Advanced attacks
  - Lecture: Leakage evaluation: TVLA and alternatives + Assignment
  - Lecture: Profiling attacks + Assignment
  - Lecture: AI basics
- Day 3: AI and SCA
  - Lecture: AI-assisted SCA
  - Assignments
  - Lecture: Leakage simulators
  - Lecture: Higher order attacks (if there is time)
  - Unfinished Excercises

# Day 1

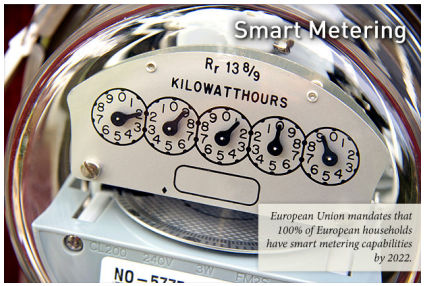
- Let's know each other!
- Basic concepts and principles – gray box, platforms, setups, side channels
- Side-channel leakage modeling
- Simple power analysis (SPA)
- Differential power analysis (DPA)
- Correlation power analysis (CPA)
- Assignments 1-2: Hands-on DPA attacks on software and hardware implementations
  - For now ignore the TVLA part
- Resources: `https://tinyurl.com/ysnznaka` [1]

[1] Full: `https://www.dropbox.com/scl/fo/bd9r3lvzbk7eilqgytroo/ADK3b5aUicY2hzshgYCCQ8g?rlkey=5uzcphdvbnhlhs4z6zal63tqc&st=j5al094h`

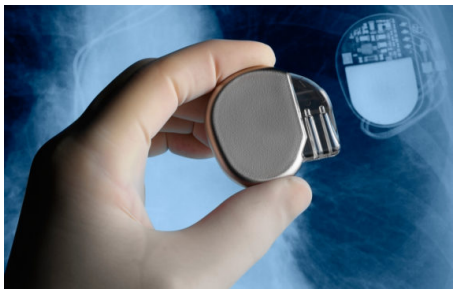
# Outline

# Introducing the side channel

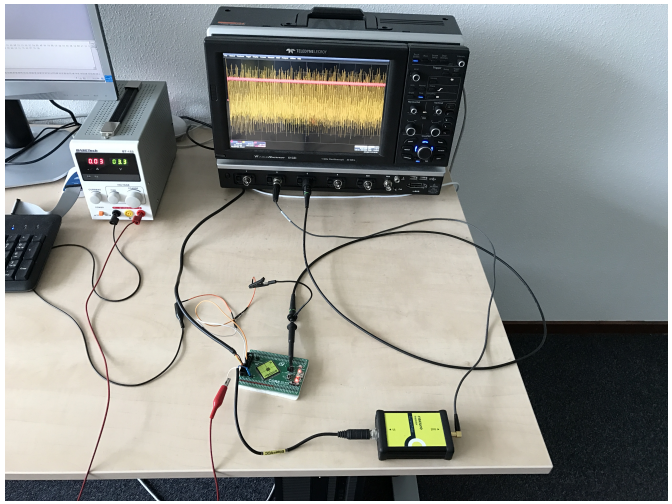
# Known challenge: embedded crypto devices






# Implementation attacks



# Relevance

**Minerva, October 3, 2019**

Researchers Discover ECDSA
Key Recovery Method

# Relevance

## TPM-FAIL, November 13, 2019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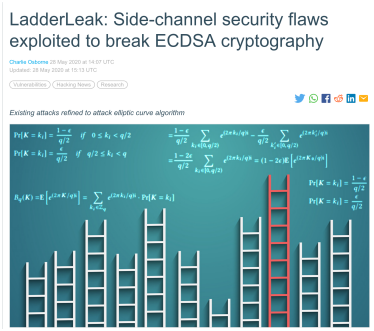
## LadderLeak, May 28, 2020

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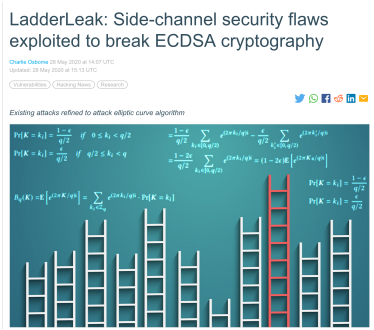


## SCA Titan: January 7, 2021

## Minerva, October 3, 2019

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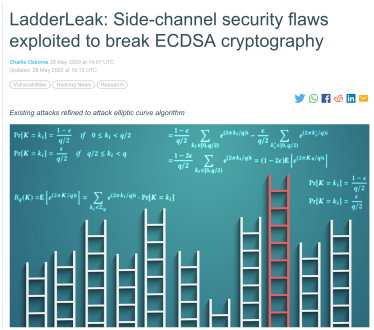


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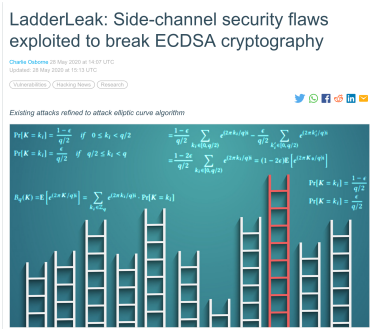


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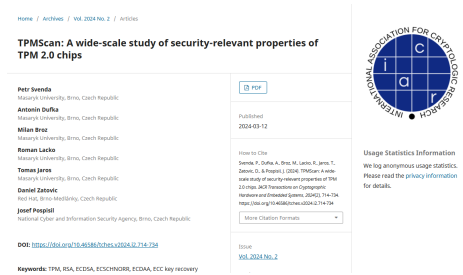
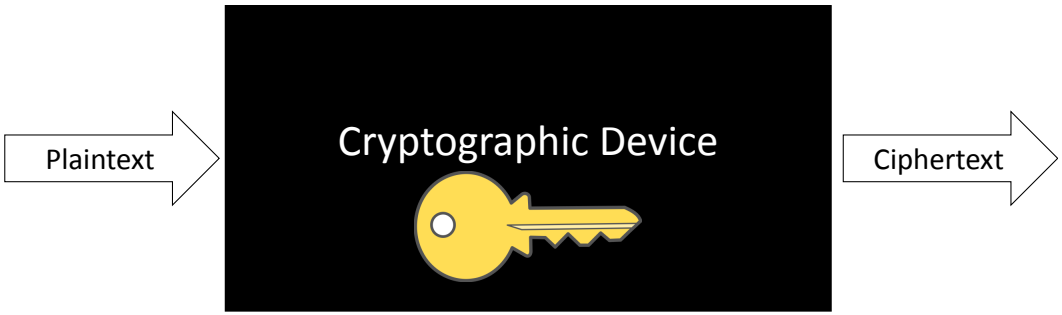



## EUCLEAK, Yesterday

# Blackbox scenario

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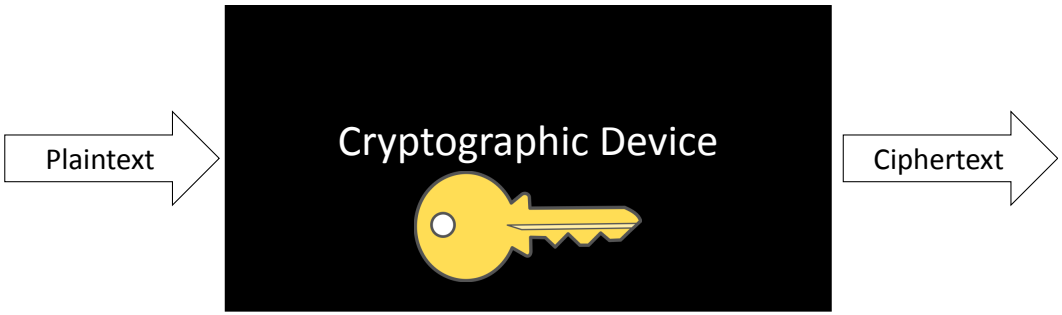


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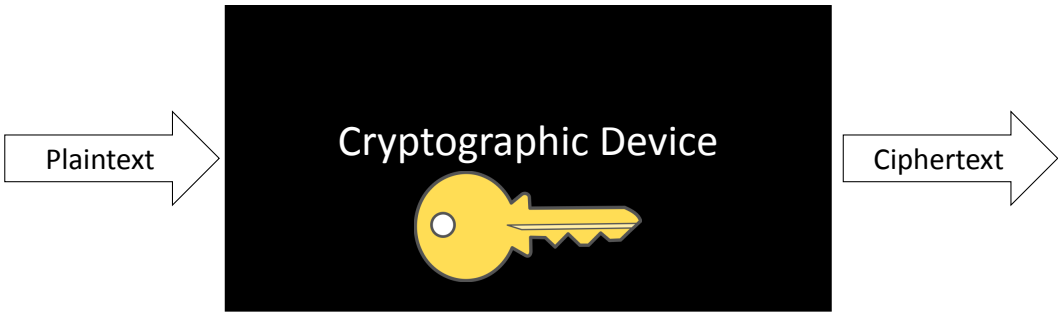


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- Examples: execution/reaction time, power consumption, electromagnetic emission, sound

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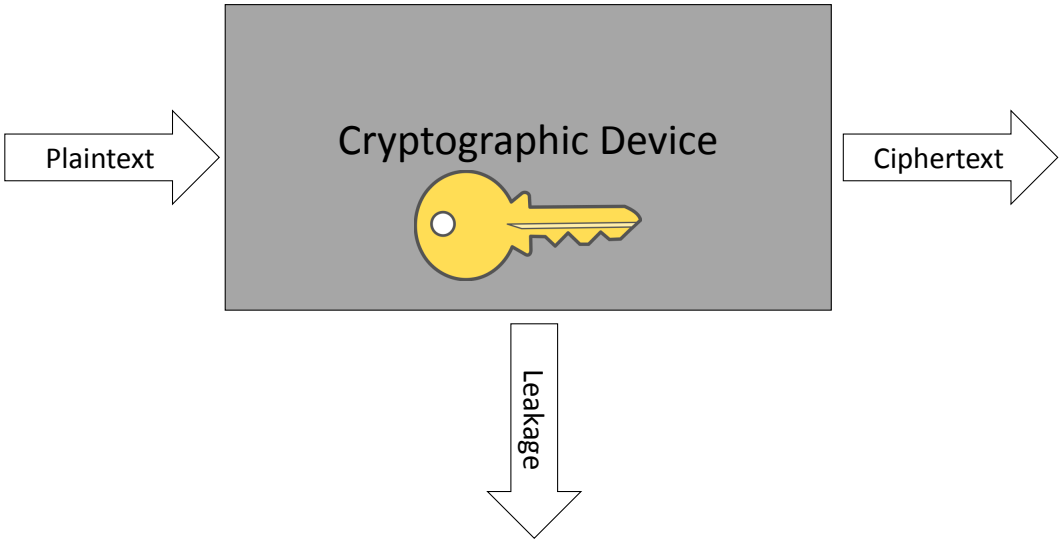

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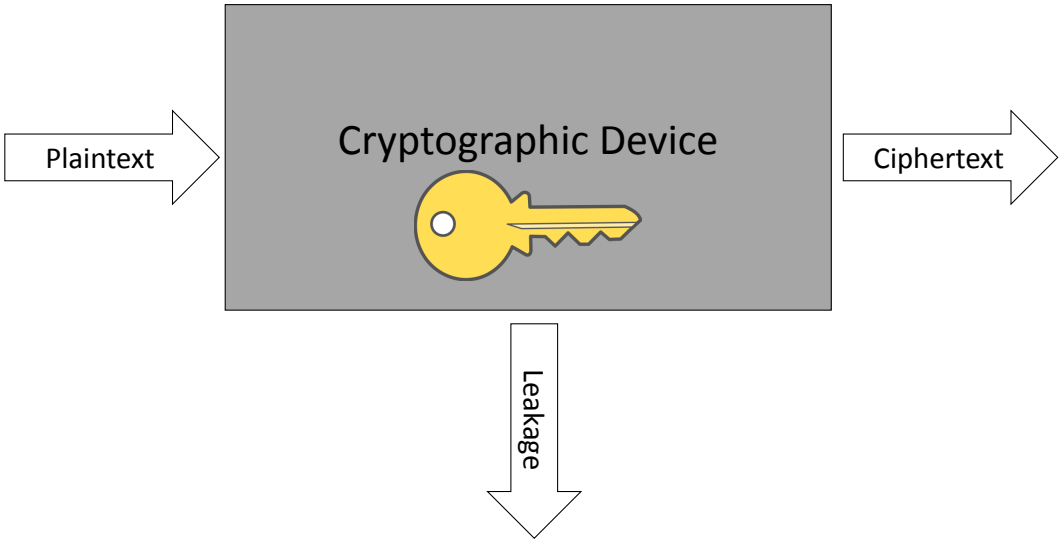


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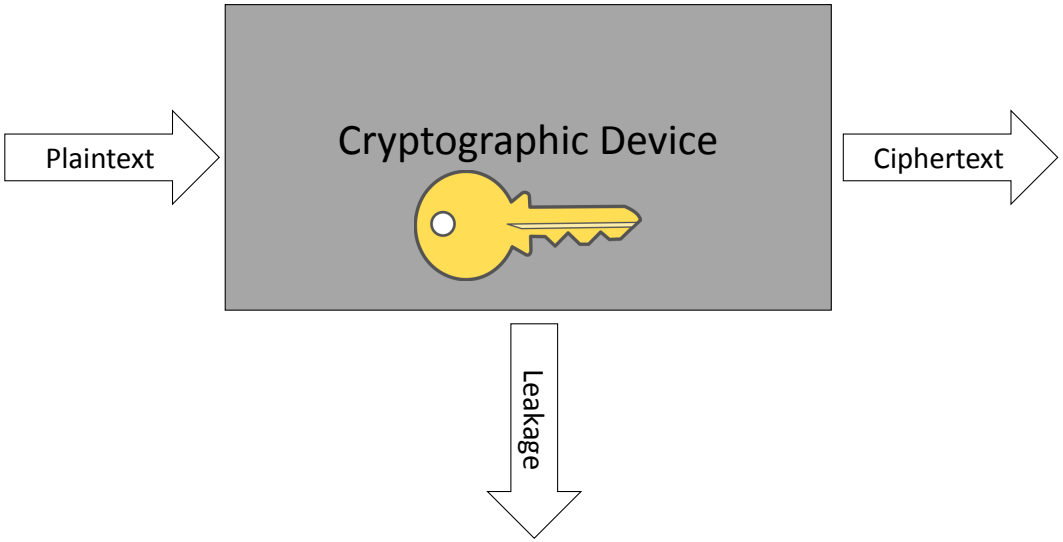


- Assuming limited access to the internal computations through this side channel window → greybox scenario
- Security in the blackbox scenario does not imply security under the greybox scenario

# Timing side-channel

# Timing side-channel: PIN verification

- Software for PIN code verification

```
Input: 4-digit PIN code
Output: PIN verified or rejected
Process CheckPIN (pin[4])
int pin_ok=0;
if (pin[0]==5)
   if (pin[1]==9)
      if (pin[2]==0)
         if (pin[3]==2)
            pin_ok=1;
         end
      end
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return pin_ok;
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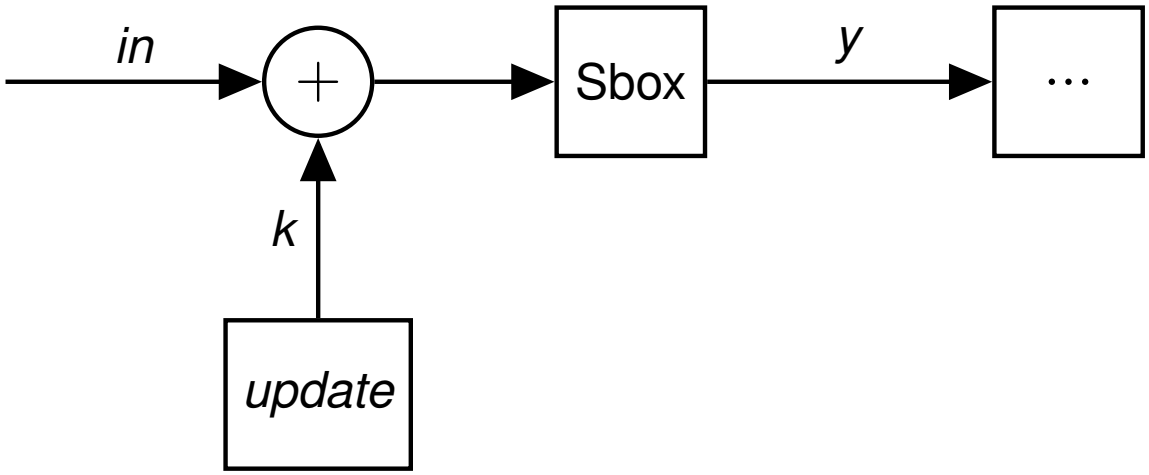
- What are the execution times of the process for PIN inputs `[0,1,2,3]`, `[5,3,0,2]`, `[5,9,0,0]`
- The execution time increases as we get closer to `[5,9,0,2]`

# Timing side-channel: Cache attacks



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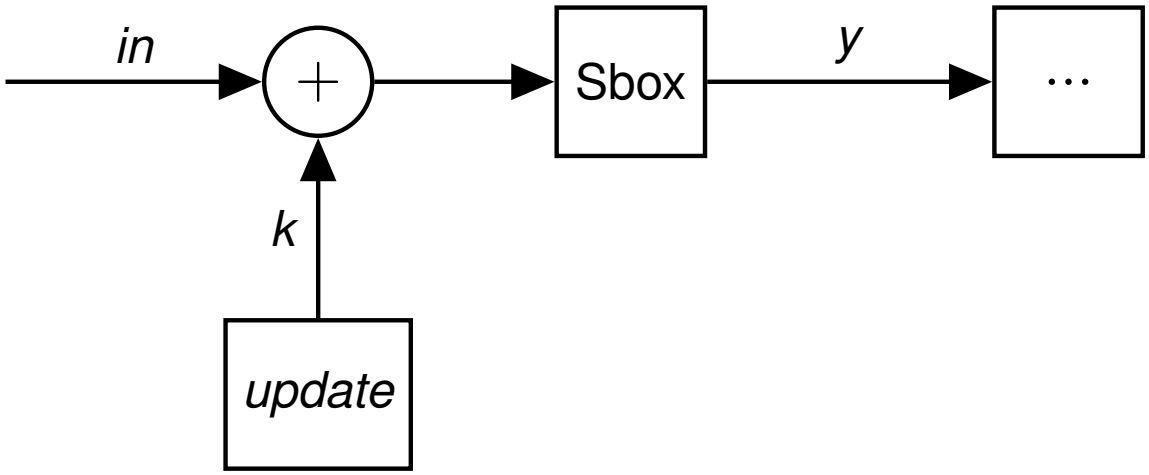


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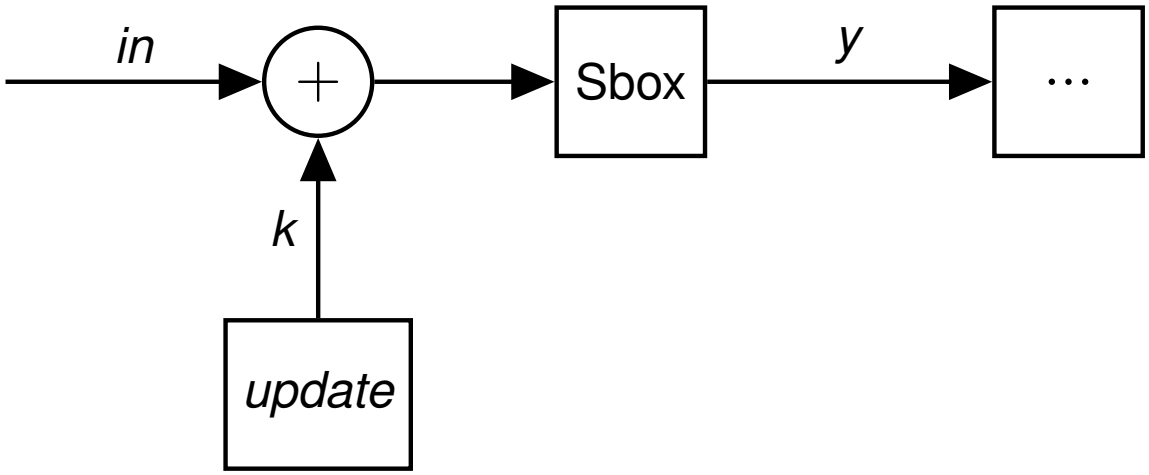


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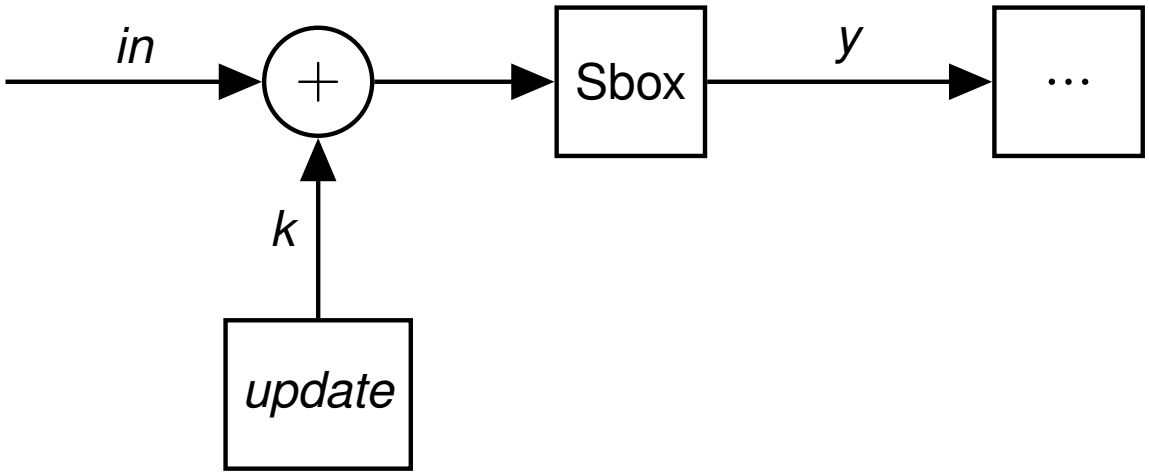


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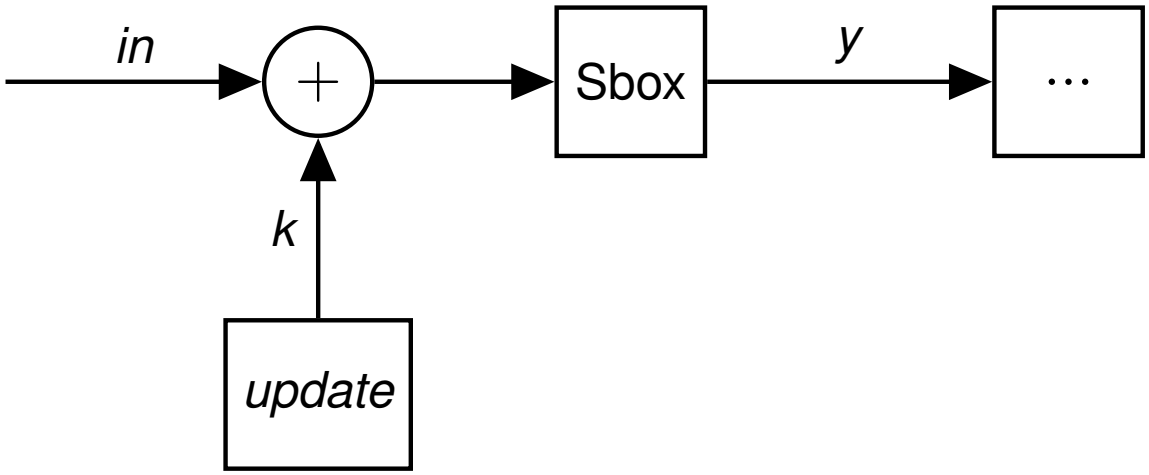


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- The underlying cause is cache behavior of modern processors

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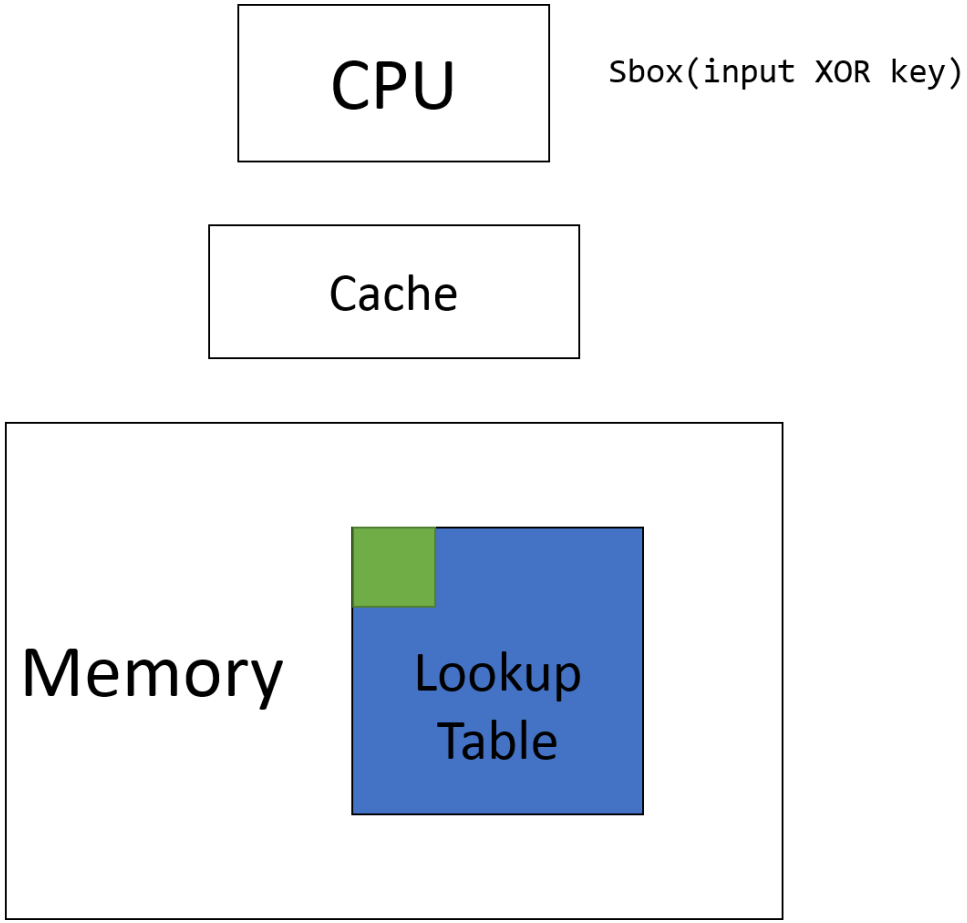

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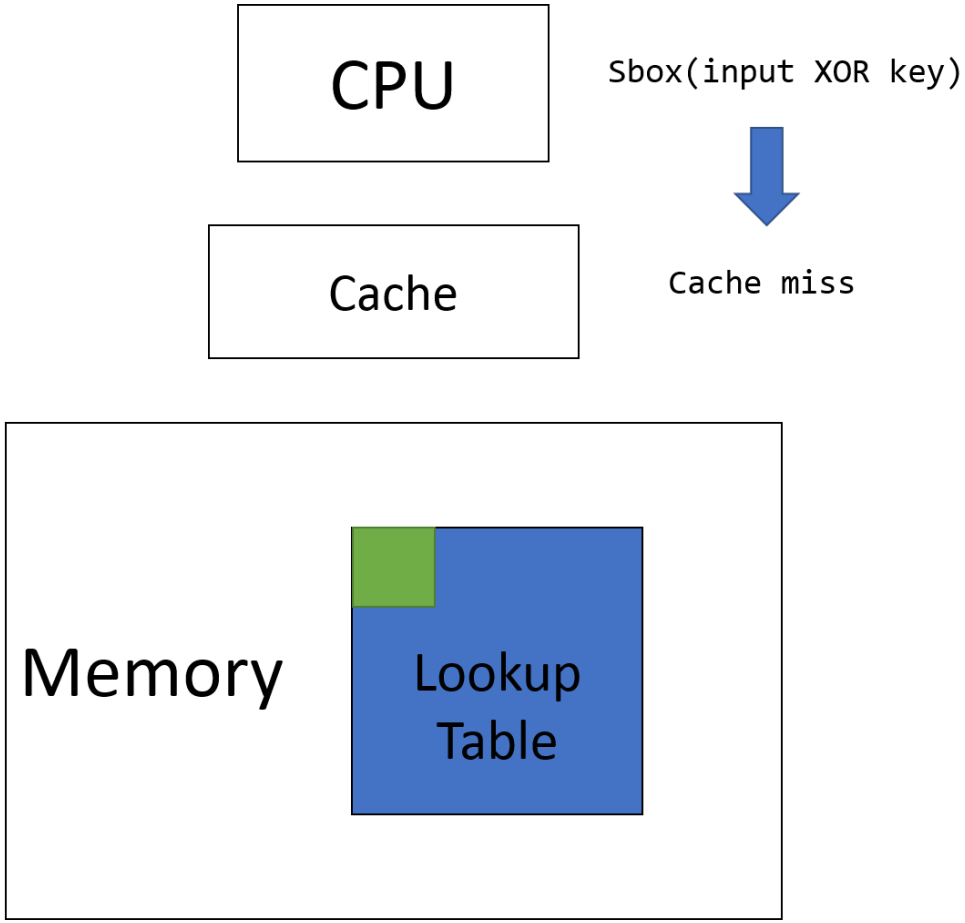

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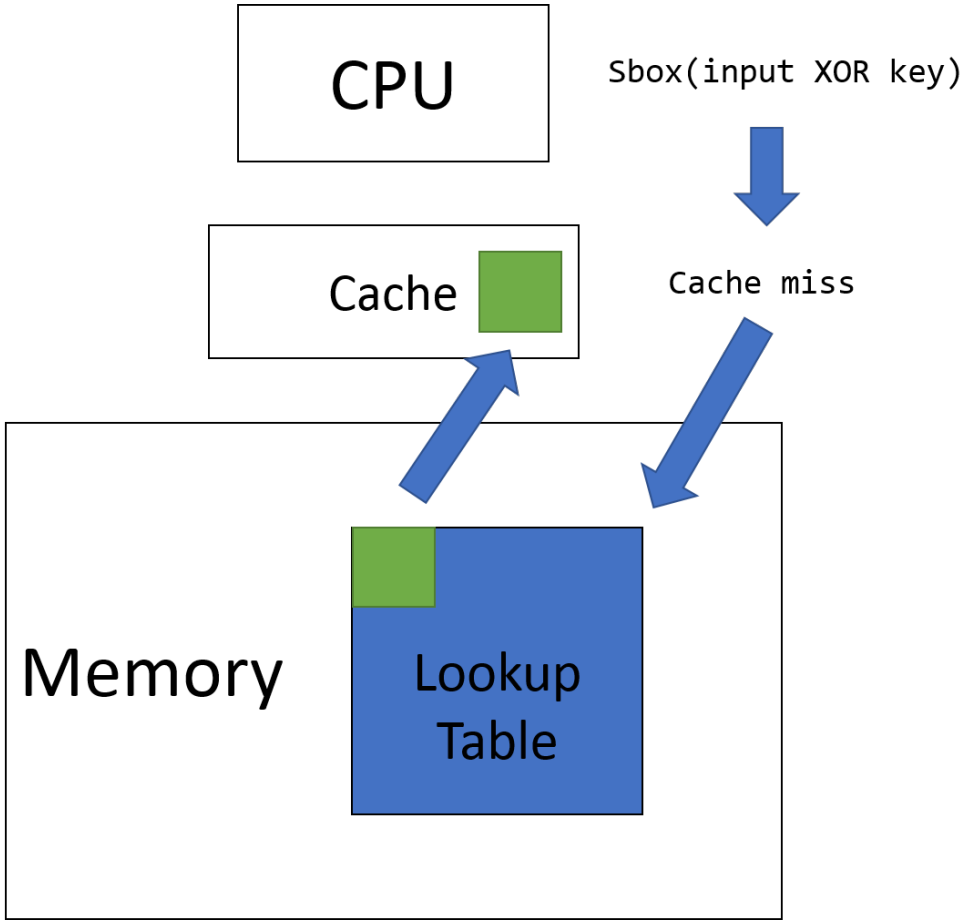

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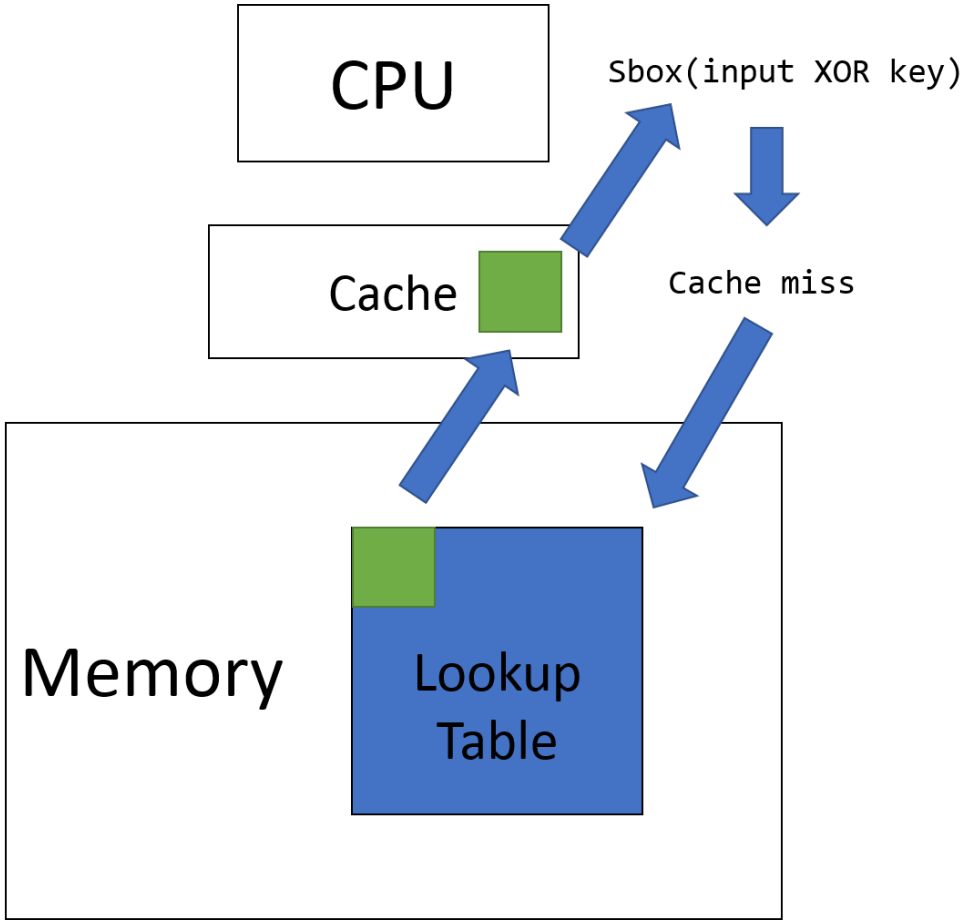

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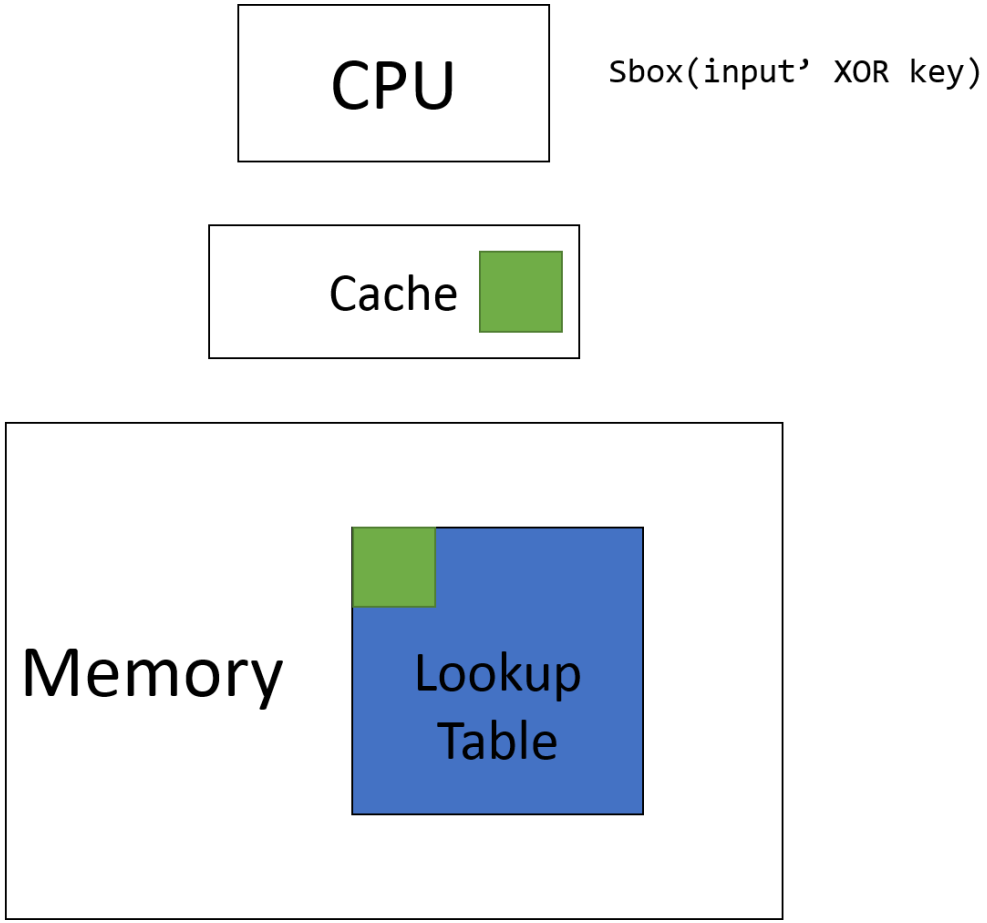

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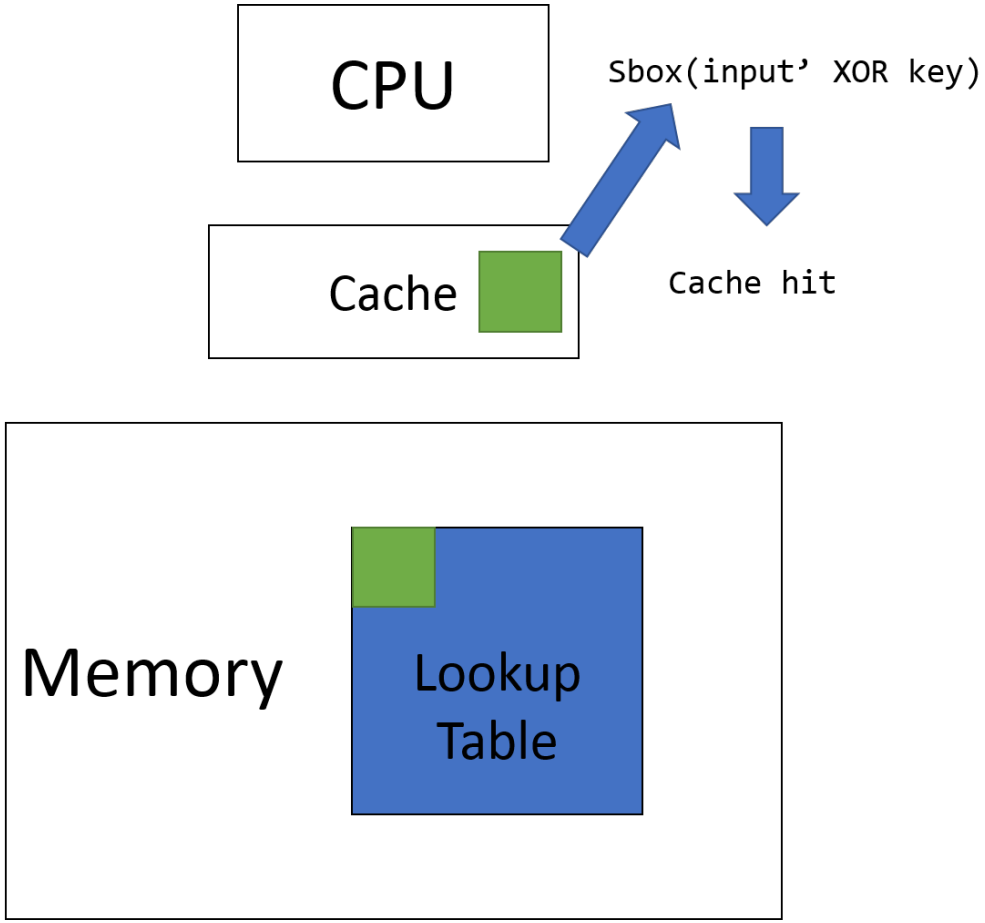

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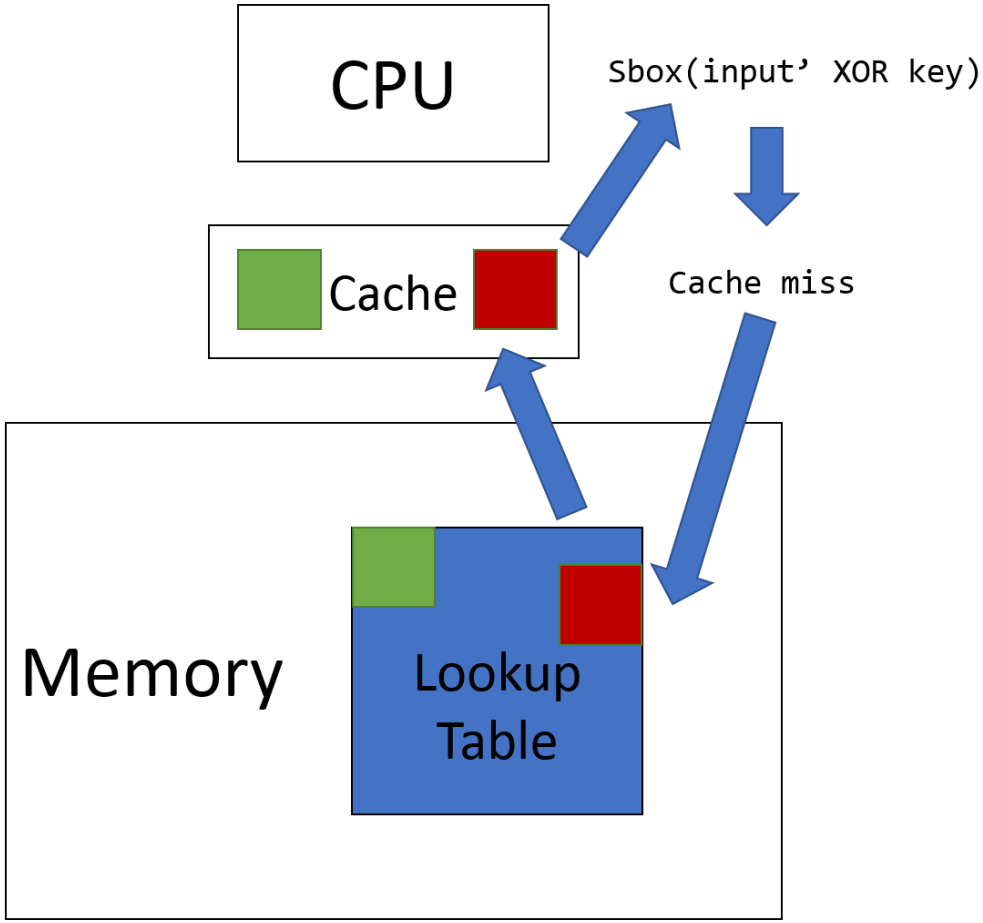

# Timing attacks notes and literature

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- Can also be exploited remotely
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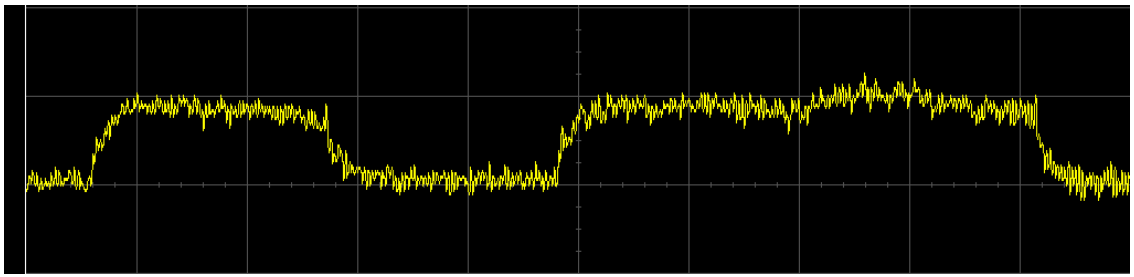
- P. Kocher. “Timing Attacks on Implementations of Diffie-Hellman, RSA, DSS, and Other Systems”, CRYPTO 1996
- Daniel Page. “Theoretical use of cache memory as a cryptanalytic side-channel”, technical report CSTR-02-003, 2002.
  `https://eprint.iacr.org/2002/169.pdf`
- Daniel J. Bernstein. “Cache-timing attacks on AES.”
  `https://cr.yp.to/antiforgery/cachetiming-20050414.pdf`

# Power side-channel



# Power side channel: CMOS leakage

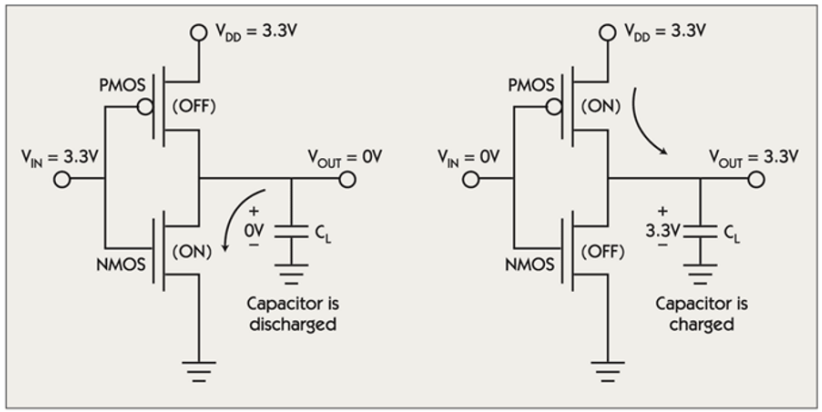



**Fig. 1** Dynamic power in a CMOS inverter.

- CMOS is the most popular technology and the CMOS circuits exhibit several types of leakage

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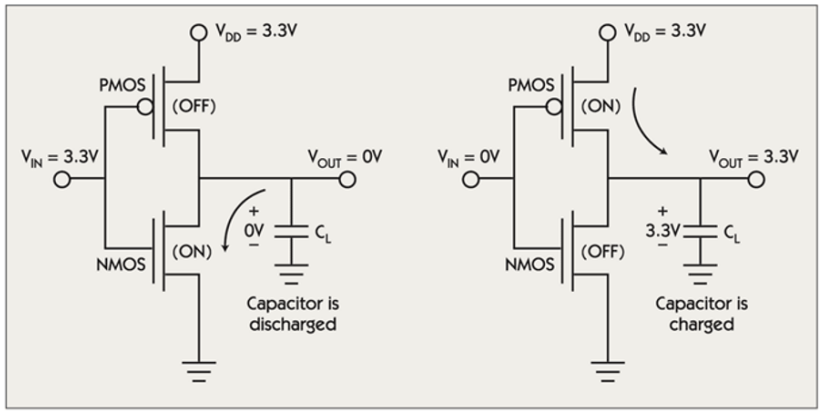


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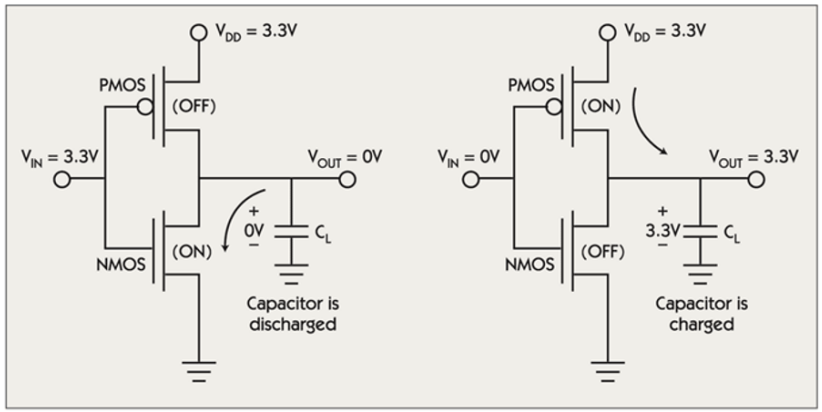


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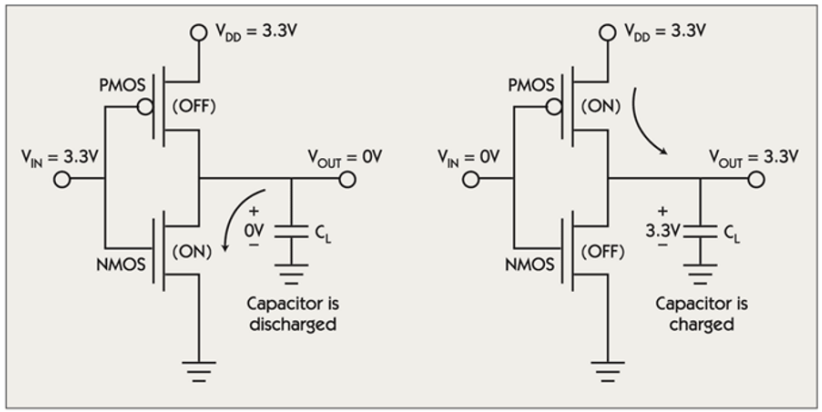


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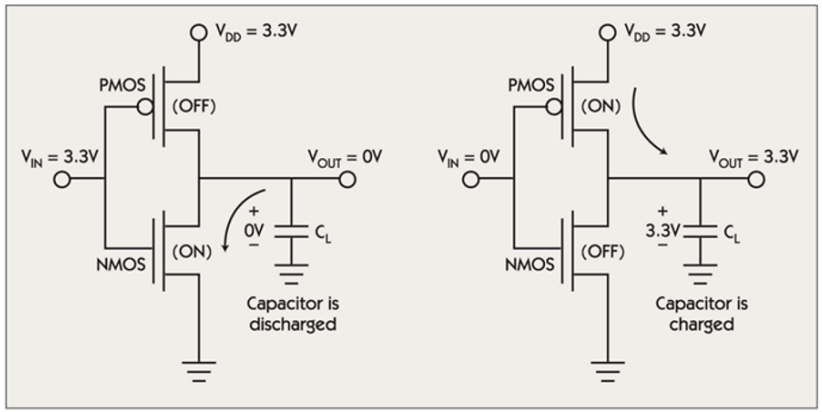


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- $P_{dyn} = CV_{DD}^2 P_{0\to1} f$,
  where $C$ the transistor capacitance, $V_{DD}$ the power supply voltage, $f$ the frequency and $P_{0\to1}$ the probability of a $0 \to 1$ transition

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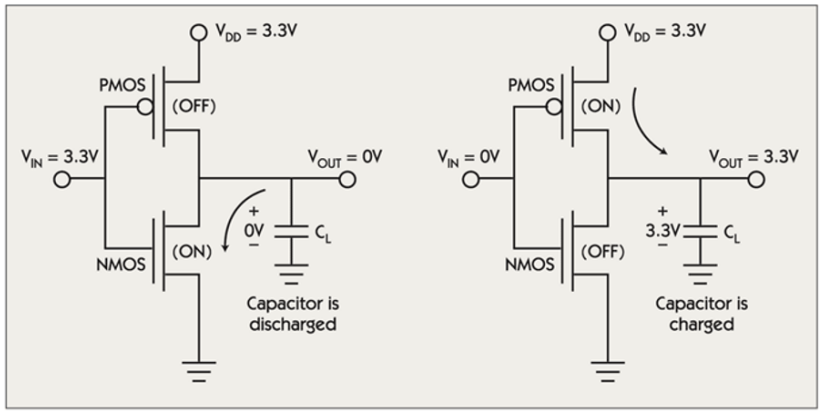


**Fig. 1** Dynamic power in a CMOS inverter.

- CMOS is the most popular technology and the CMOS circuits exhibit several types of leakage
- The most relevant for side-channel attacks is the charge and discharge of the CMOS load capacitance a.k.a dynamic power consumption
- Power analysis attack exploits the fact that the dynamic power consumption depends on the data and instructions being processed
- Dynamic power consumption ($P_{dyn}$) is produced by CMOS transitions from state 0 to 1 and from state 1 to 0
- $P_{dyn} = CV_{DD}^2 P_{0\to1} f$,
  where $C$ the transistor capacitance, $V_{DD}$ the power supply voltage, $f$ the frequency and $P_{0\to1}$ the probability of a $0 \to 1$ transition

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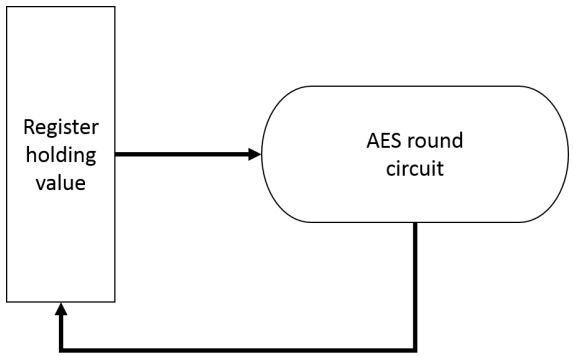

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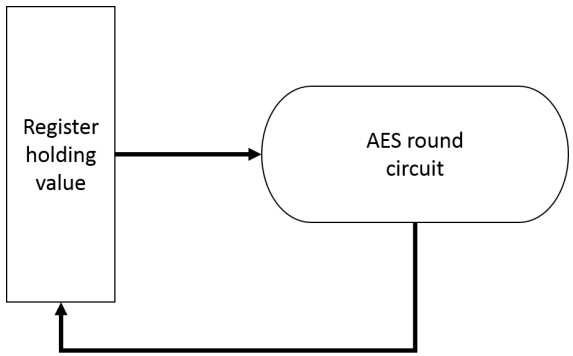


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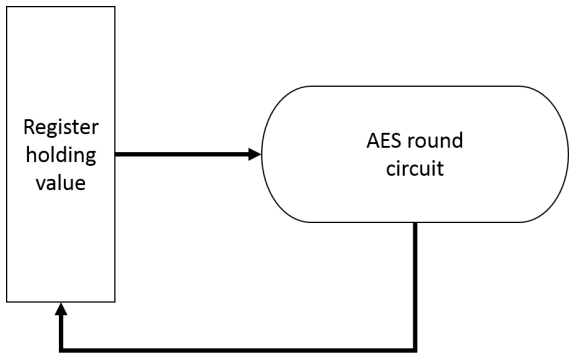


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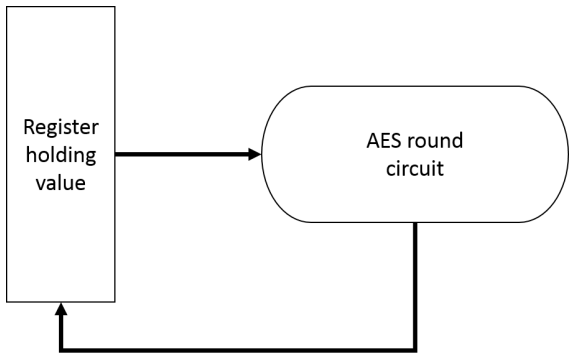


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- Common leakage model for hardware implementations (FPGA, ASIC)

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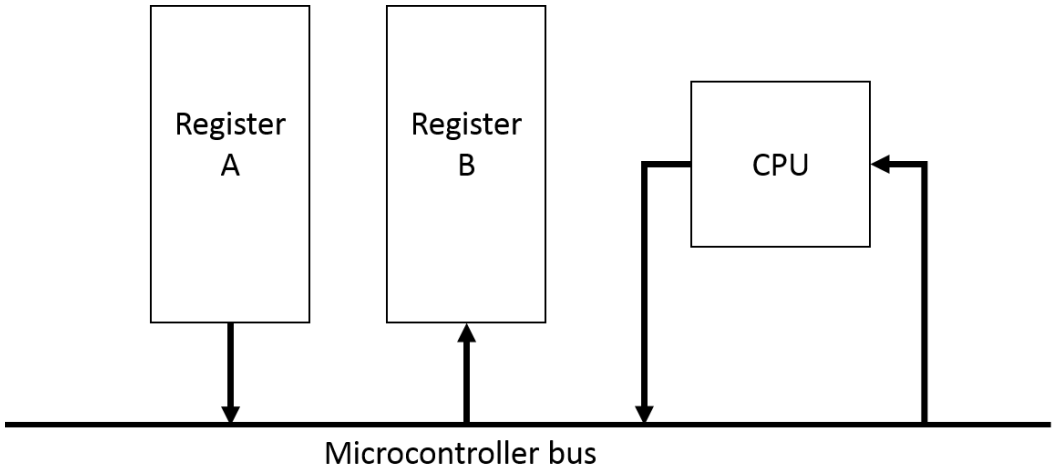

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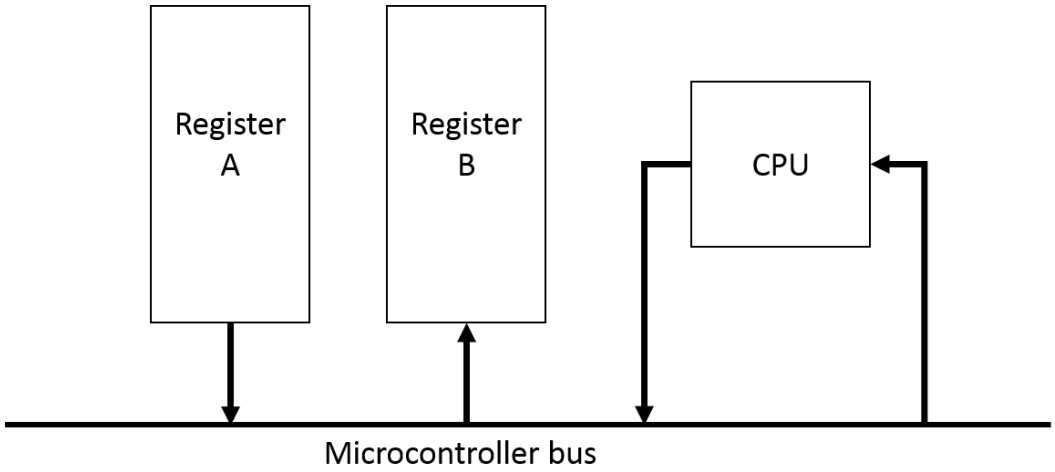


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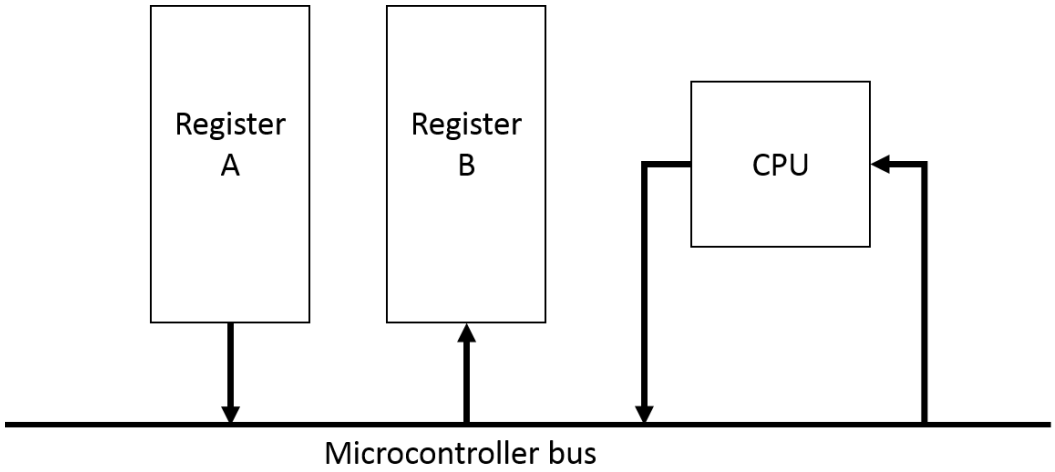


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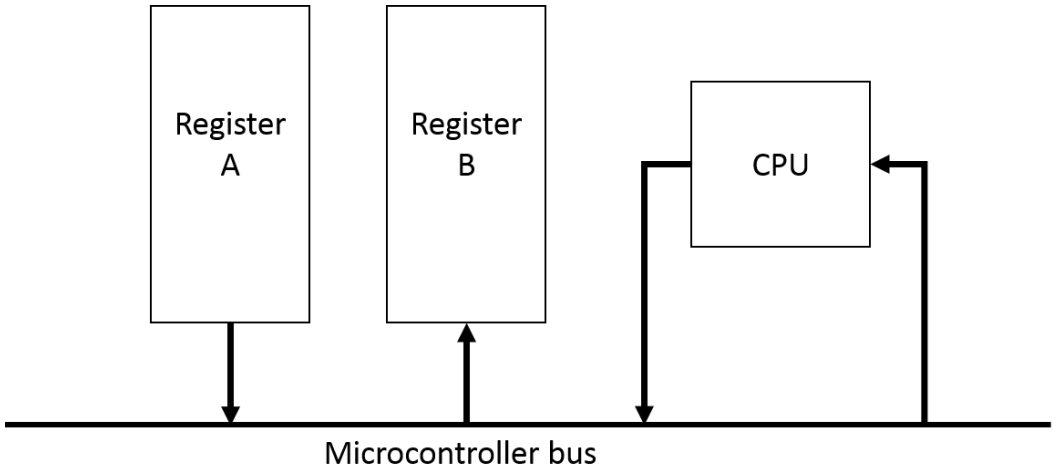


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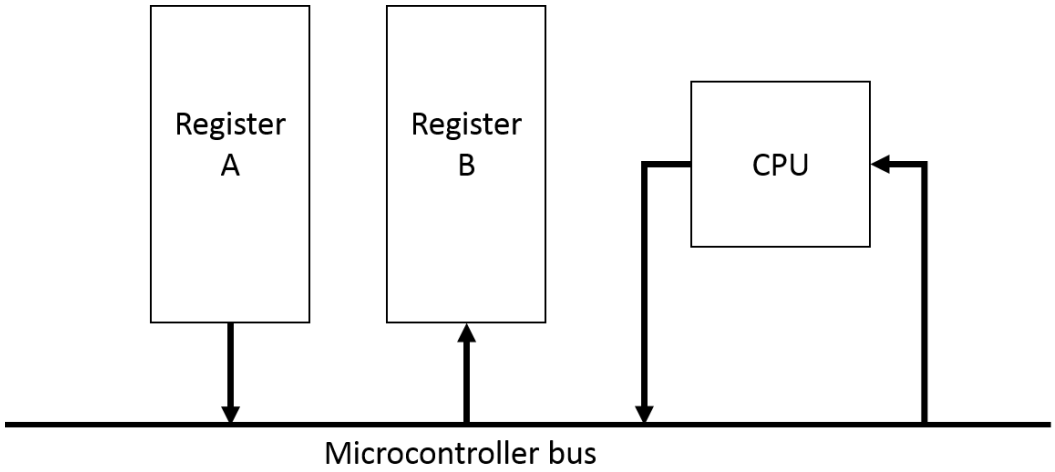


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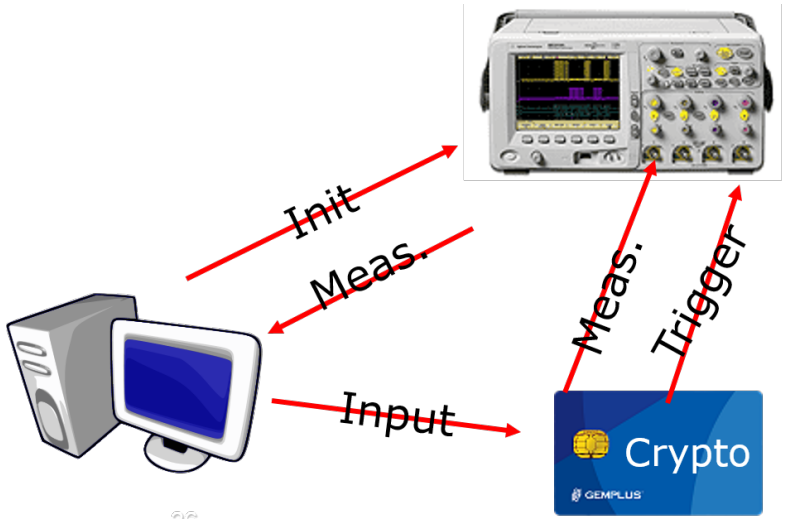
- Common leakage model for software implementations (AVR/ARM)

# Measurement setup schematics

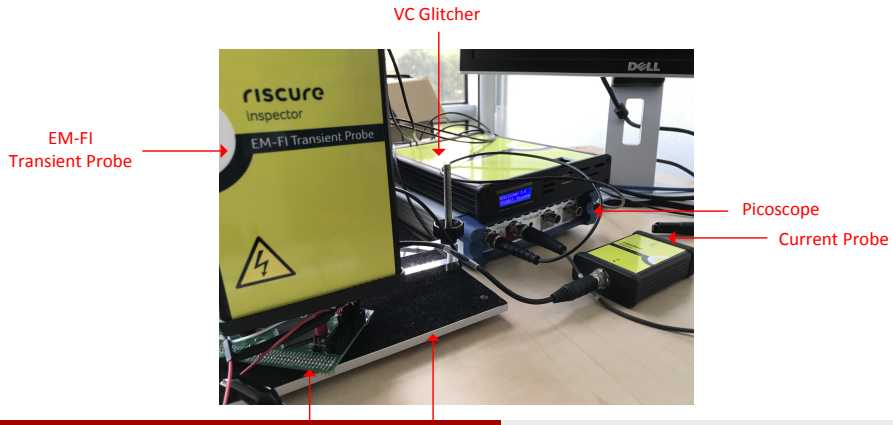



26

- Usually power measurements requires physical proximity to the device and customized measurement equipment (resistor, oscilloscope)

# Actual setups

## FA setup



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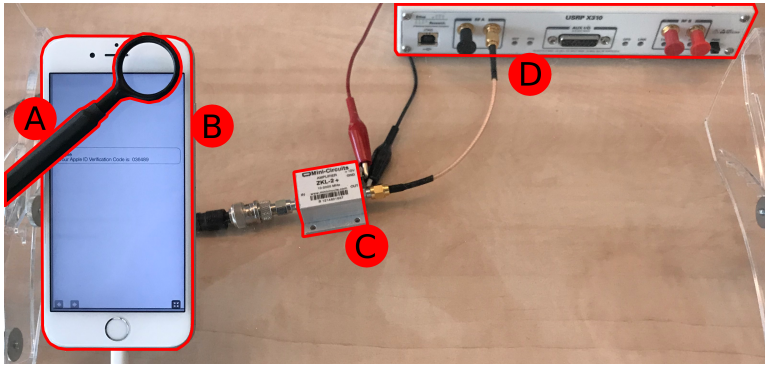
## Tempest

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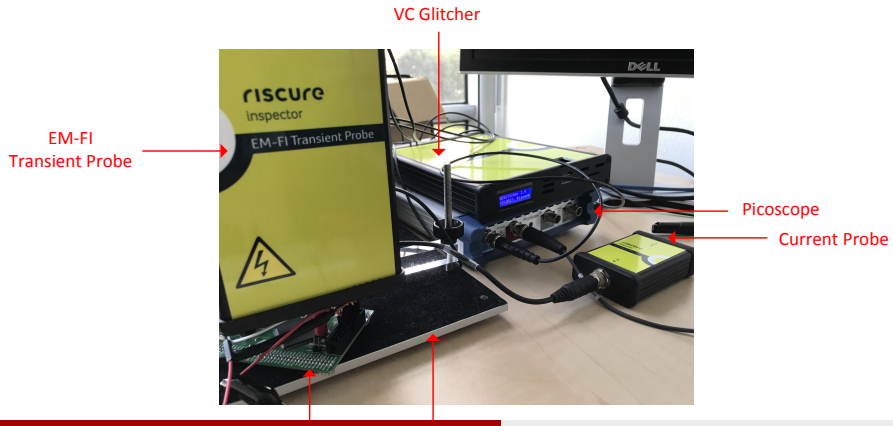
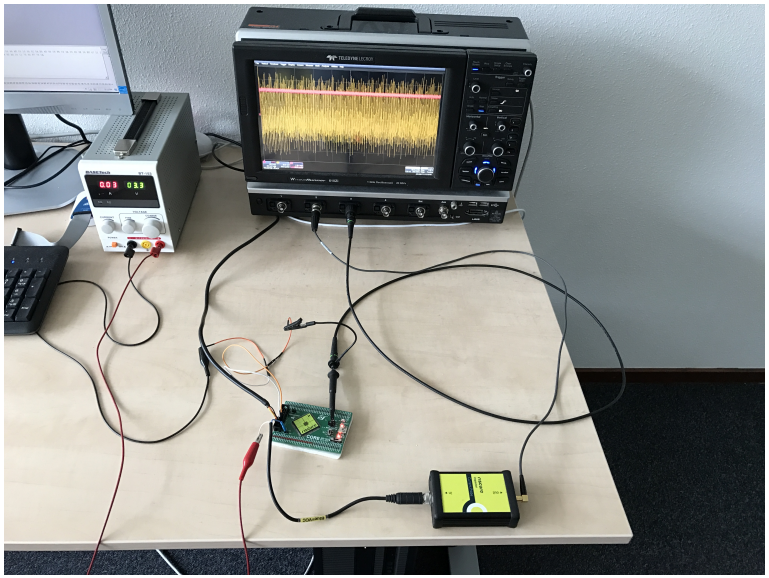


# Actual setups

## DPA setup with ARM CortexM4



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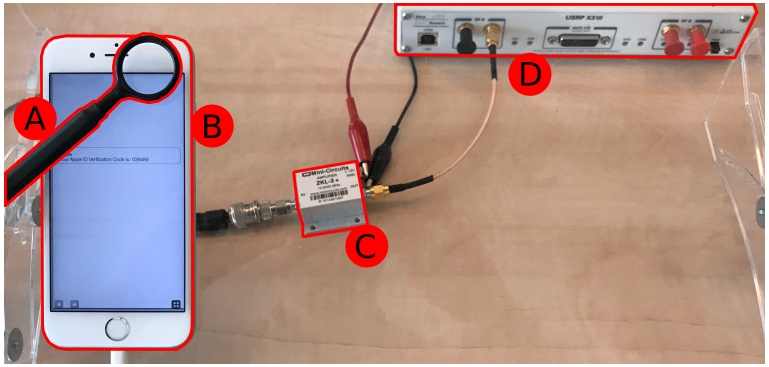


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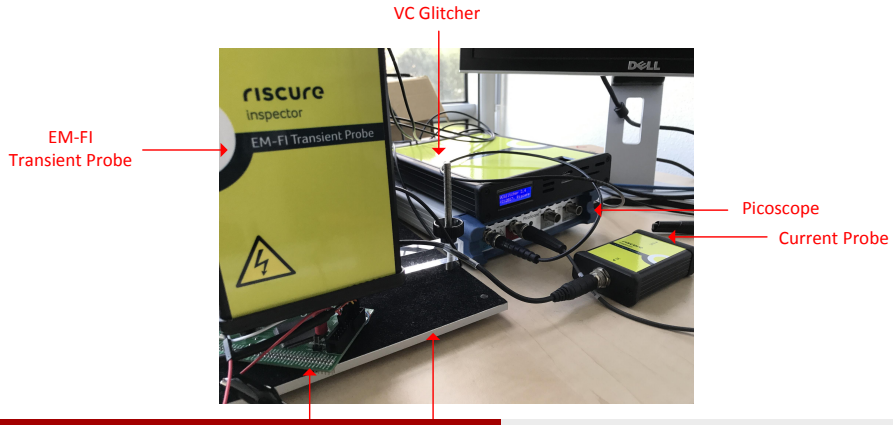

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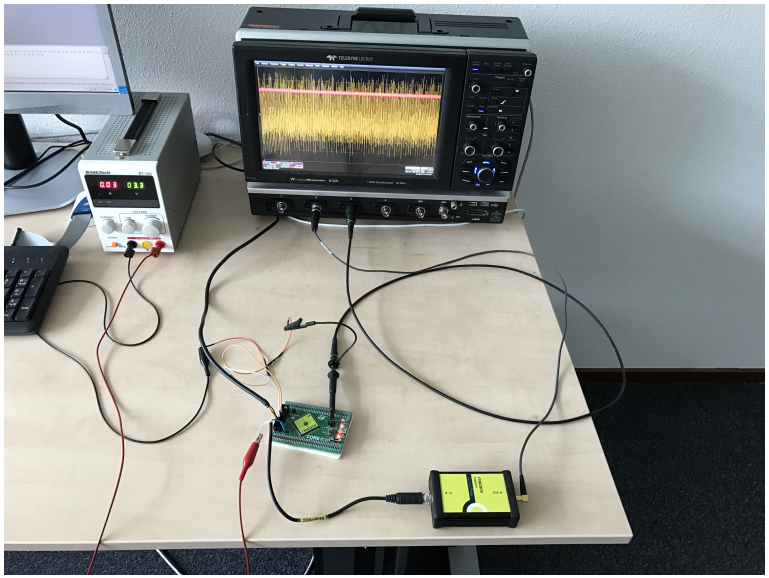

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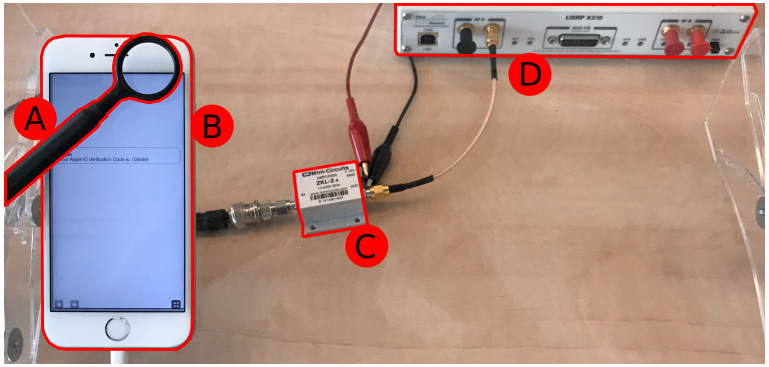
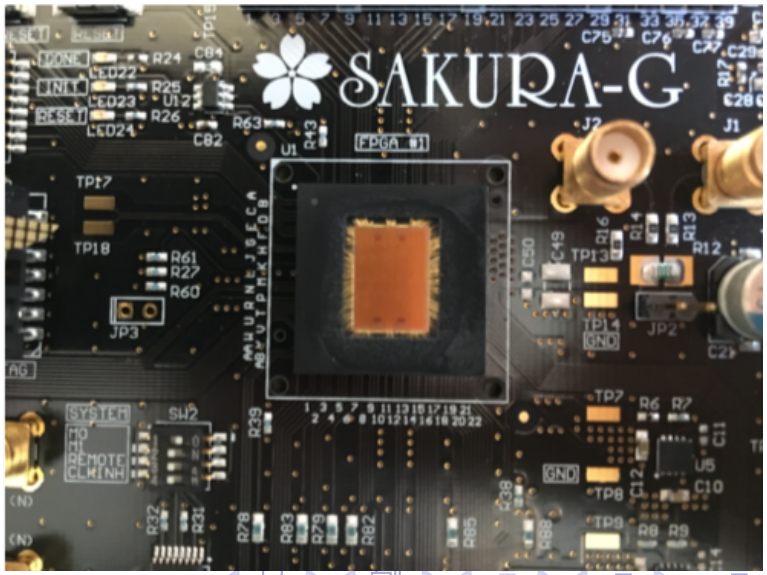
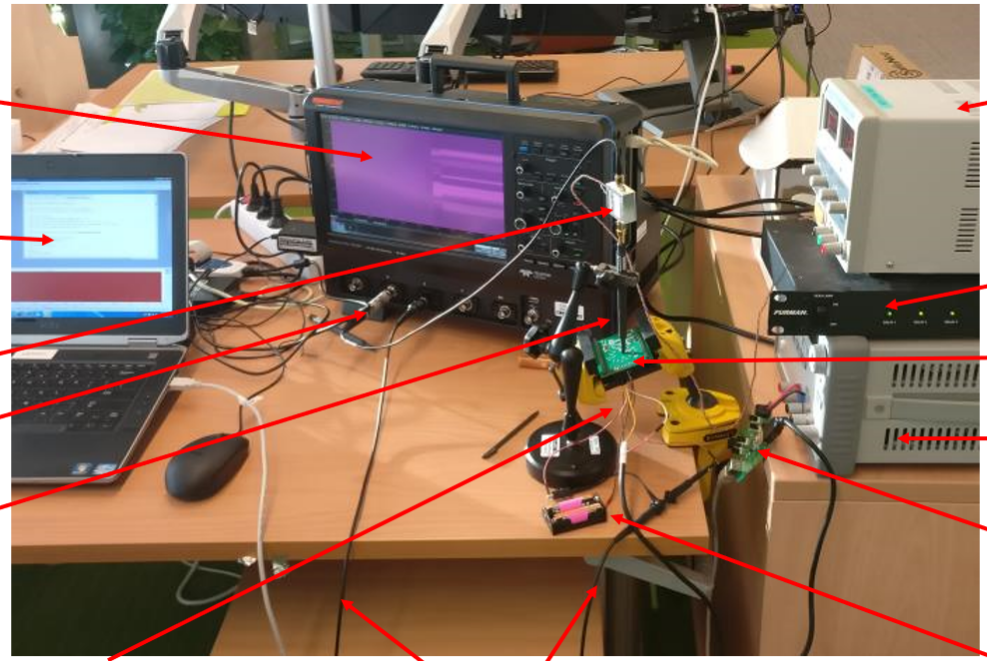



## FA setup


## FPGA board for SCA



# Actual (overcomplicated?) setup



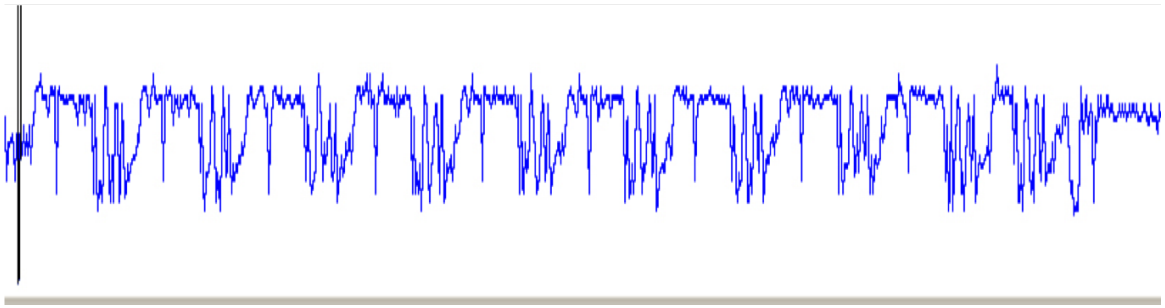
# Analysis capabilities

- Simple Power Analysis (SPA): one or a few measurements - visual inspection or some simple signal processing
- Differential attacks (DPA): multiple measurements - use of statistics, signal processing, etc.
- Higher order attacks: Univariate vs multivariate
- Profiled attacks: more in the lecture on Template attacks
- Combining two or more side-channels
- Combining side-channel attack with theoretical cryptanalysis

# Simple Power Analysis (SPA)

- Based on one or a few measurements
- Mostly discovery of data-(in)dependent but instruction-dependent properties e.g.
  - Symmetric:
    - Number of rounds (resp. key length)
    - Memory accesses (usually higher power consumption)
  - Asymmetric:
    - The key (if badly implemented, e.g. RSA / ECC)
    - Key length
    - Implementation details: for example RSA w/wo CRT

# SPA example 1



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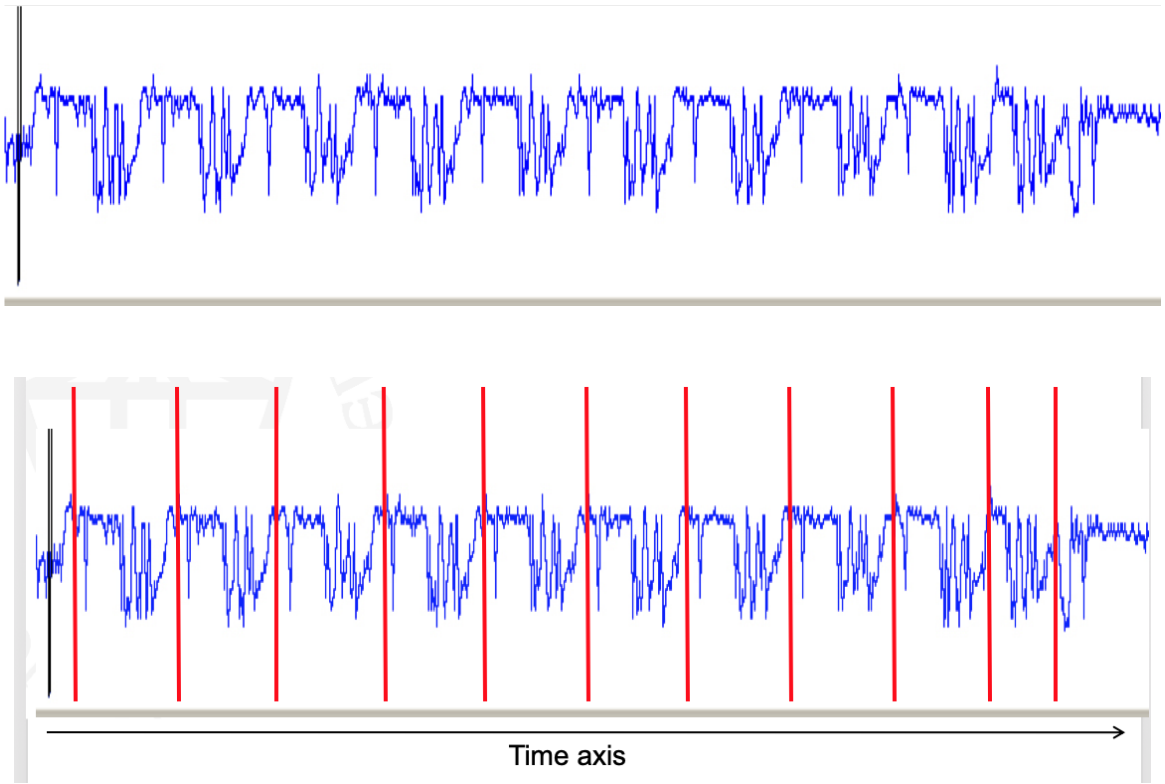

# SPA on RSA (Square-and-Multiply)

- RSA modular exponentiation

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Input: integers x, e, n, length l of e
Output: x^e mod n

Process ModularExponentiation(x, e, n, l)

r=1;
for j=l-1 down to 0
   r=r^2 mod n //square
   if (bit j of e) == 1
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return r;
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- Do you see another side-channel attack?

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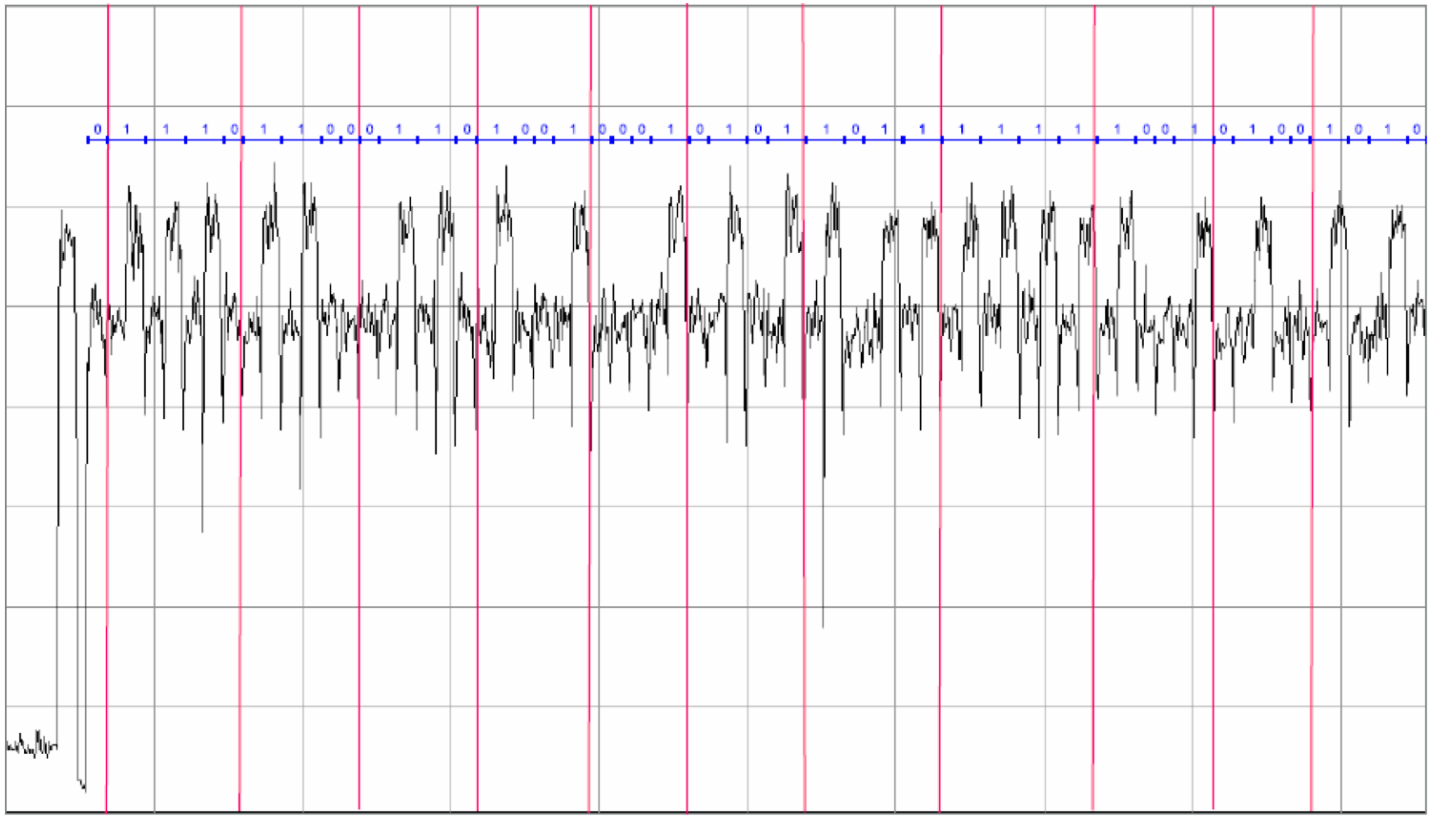

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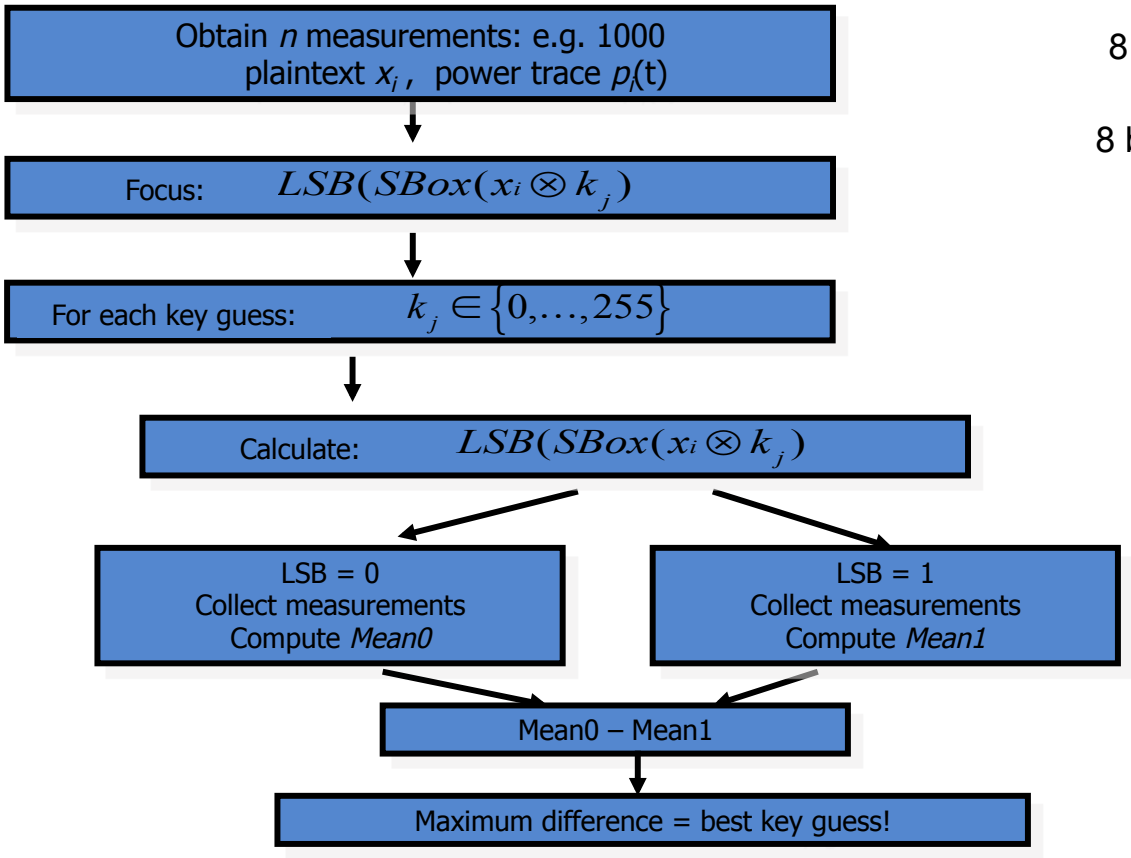
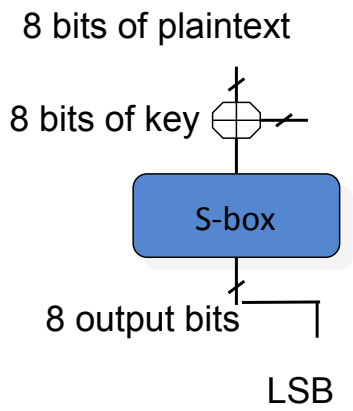
5. Recover the key by statistical means, using partition or comparison method as the side-channel distinguisher

# DPA with Distance of Means (DoM) as distinguisher

## Classical 1-bit DPA on AES using DoM




**AES impl.**




1000 measurements *
time window $t$ *
256 key guesses

[Kocher et al.]

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- T. Eisenbarth et al. “On the Power of Power Analysis in the Real World: A Complete Break of the KeeLoqCode Hopping Scheme”, CRYPTO 2008.
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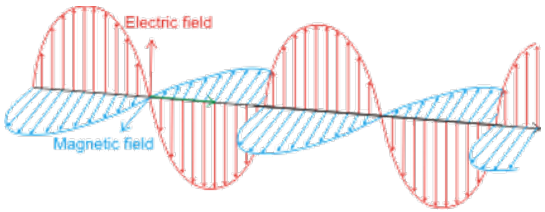
- T. Kasper et al. “All You Can Eat or Breaking a Real-World Contactless Payment System”, Financial Cryptography 2010.
- J. Balasch et al. “Power Analysis of Atmel CryptoMemory - Recovering Keys from Secure EEPROMs”, CT-RSA 2012.
- N. Samwel et al. “Breaking Ed25519 in WolfSSL.”, CT-RSA 2018.

# Electromagnetic side channel



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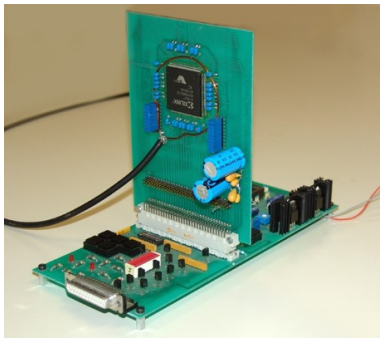

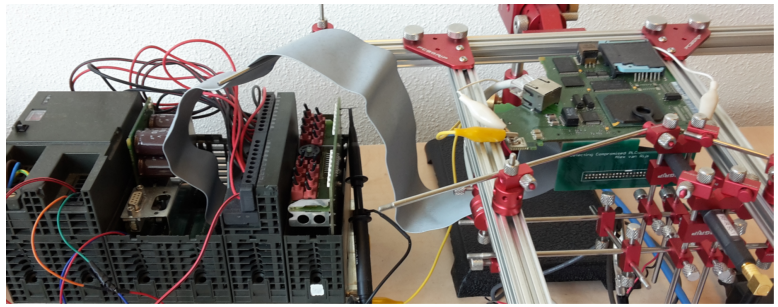

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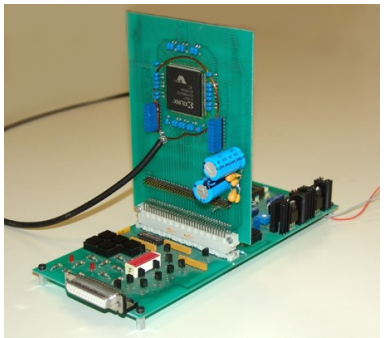
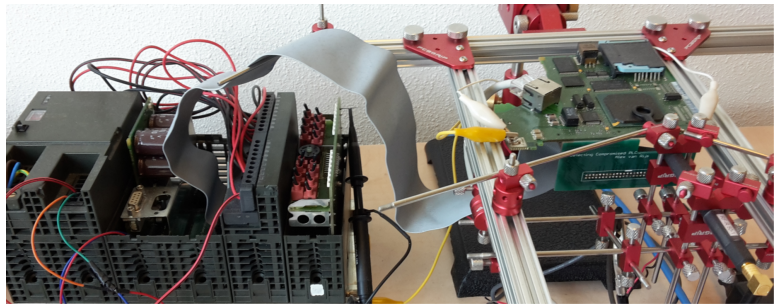
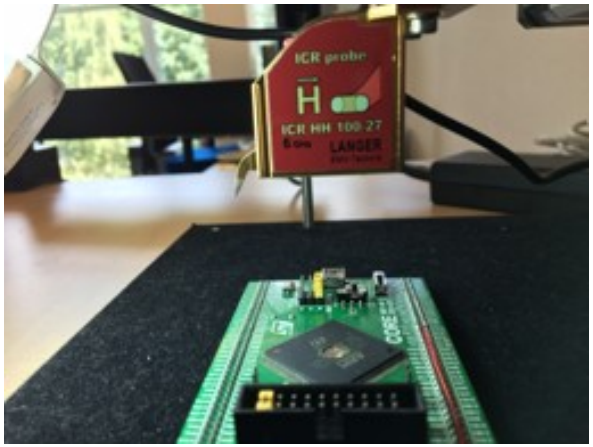




- A probe is used to access the power consumption with less board modifications
- Smaller probes can focus on interesting locations and ignore interference from unrelated el. components

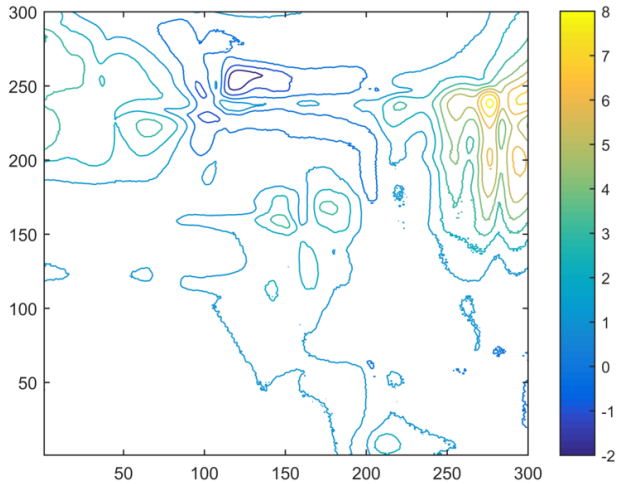
# EM side channel: Decapsulation and Microprobing

- To improve spatial resolution of analysis use a micrometer-sized antenna
- To exploit more leakage decapsulate the chip using chemicals




# EM side channel: Decapsulation and Microprobing

- Left: close inspection of decapsulated ARM processor using a microscope
- Right: EM emission heat-map of the same chip



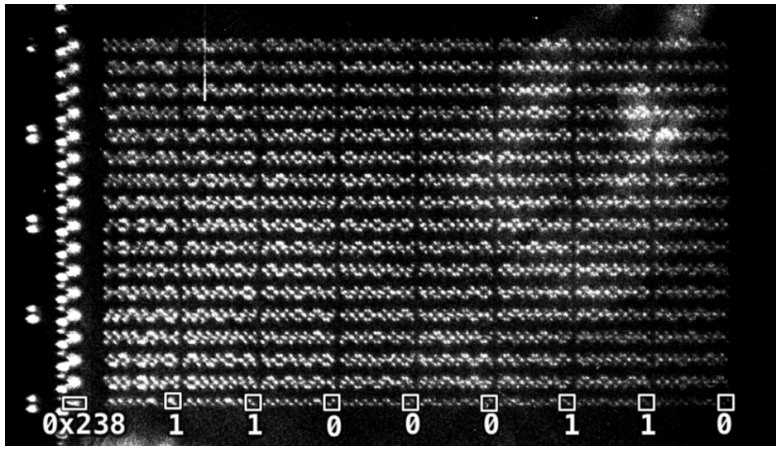
# EM side channel: notes and literature

- EM enables side-channel attacks both in high proximity scenarios and distance scenarios
- Main side channel for SoCs, FPGAs, contactless cards due to their complexity and communication methods
- TEMPEST-like attacks are also targeting private data and authentication methods such as code etc.
- Gandolfi et al.: Electromagnetic Analysis: Concrete Results, CHES 1999.
- Andrikos et al.: Location, location, location: Revisiting modeling and exploitation for location-based side channel leakages, ASIACRYPT2019

# Exotic side channels

## Exotic side channels

# Optical Emission

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- Visual inspection can reveal the memory location accessed

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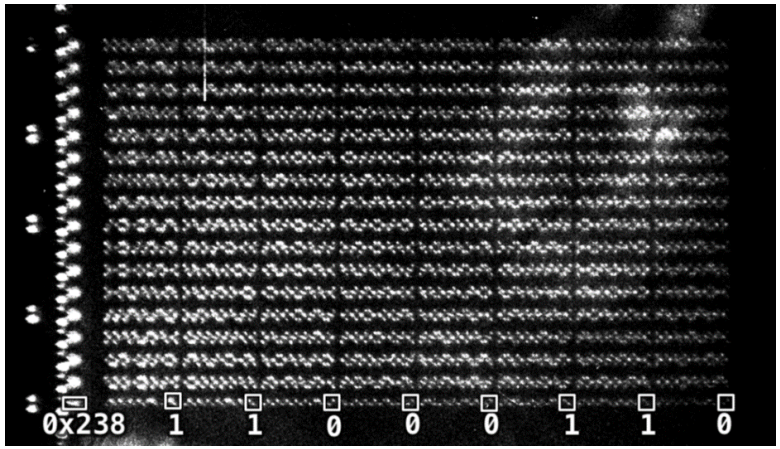
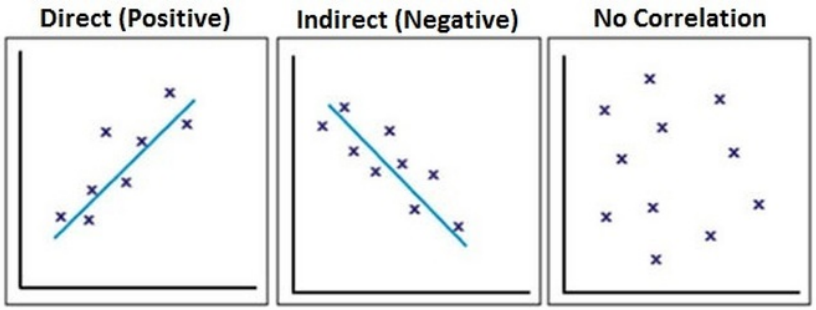



- Accessing the chip SRAM cells emits photons that can be detected by a high-resolution camera
- Visual inspection can reveal the memory location accessed
- The memory location maps to a specific value (e.g. in the AES LUT), i.e. it maps directly to $Sbox(in \oplus key)$
- Since the input *in* is known, knowledge of the memory location reveals the key
- Schlösser et al.: Simple Photonic Emission Analysis of AES, CHES 2012.

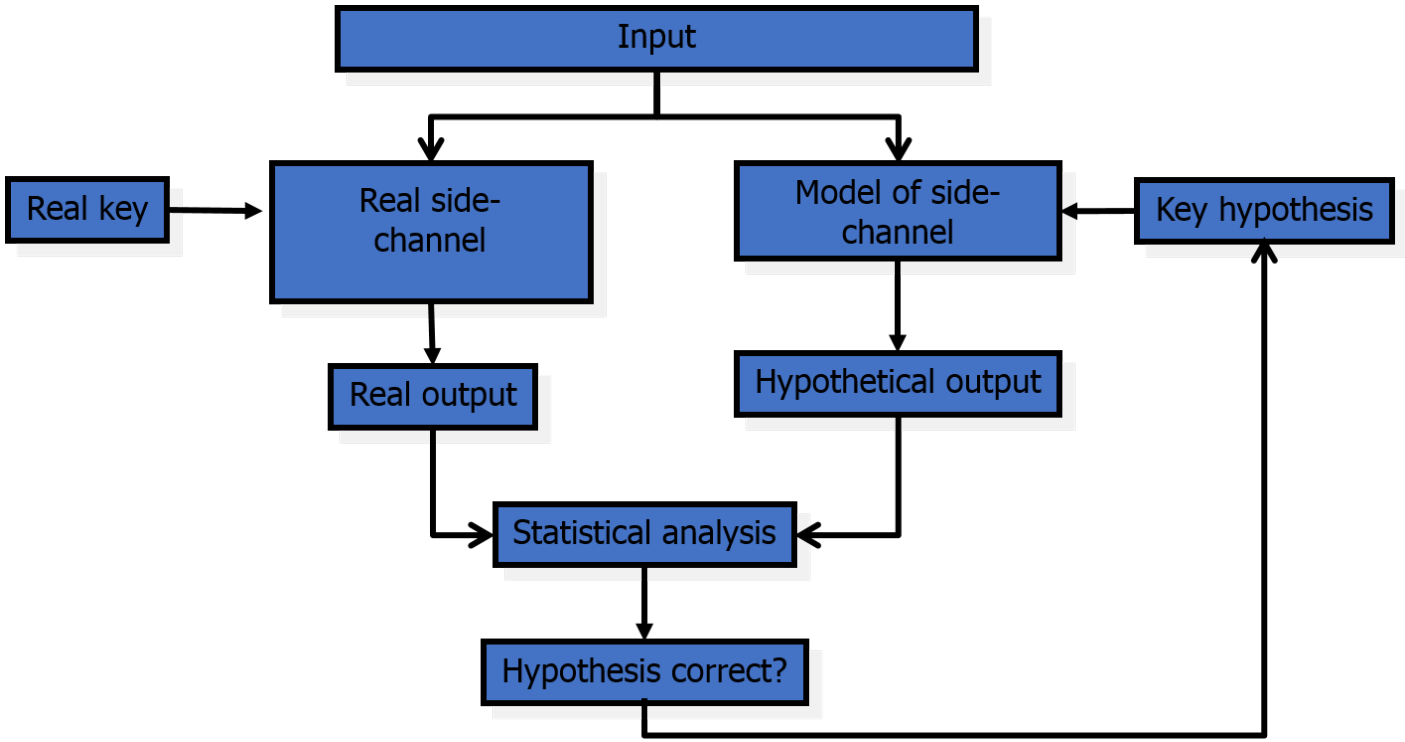
# Out-of-order and speculative execution


- Meltdown and Spectre Attacks
- Kernel addresses were access unintentionally due to out-of-order execution
- Taking all possible branches may also cause issues
- Foreshadow as a variant of Meltdown on SGX
- Recent ones: RIDL, ZombieLoad, ...

# Correlation Power Analysis (CPA)

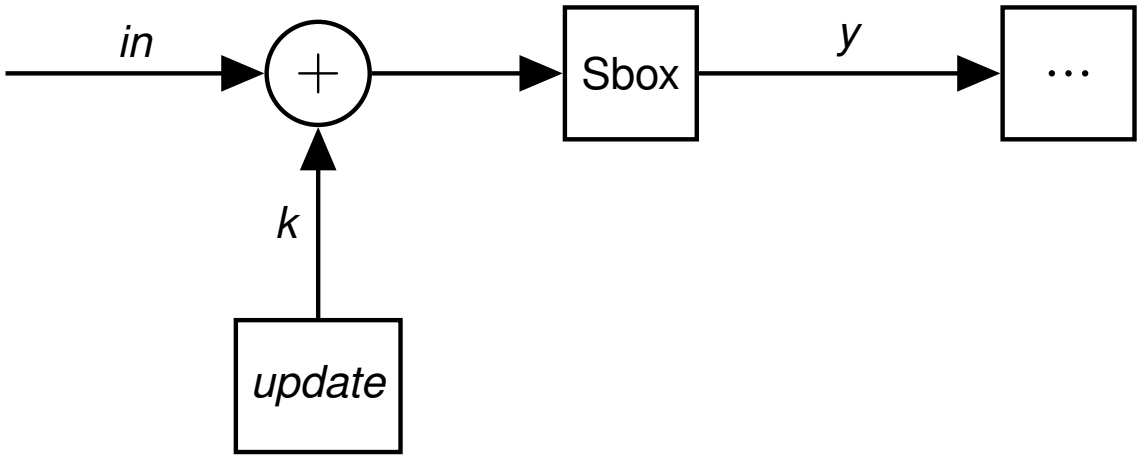


# CPA: the main principle




- Brier et al.: Correlation Power Analysis with a Leakage Model, CHES 2004

# CPA Step 1: Choose intermediate value and decide on the leakage model

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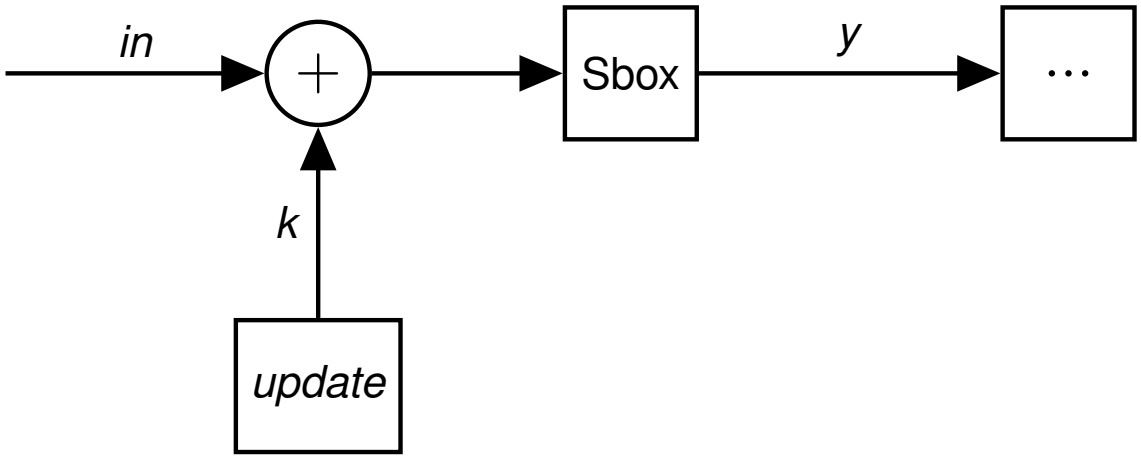


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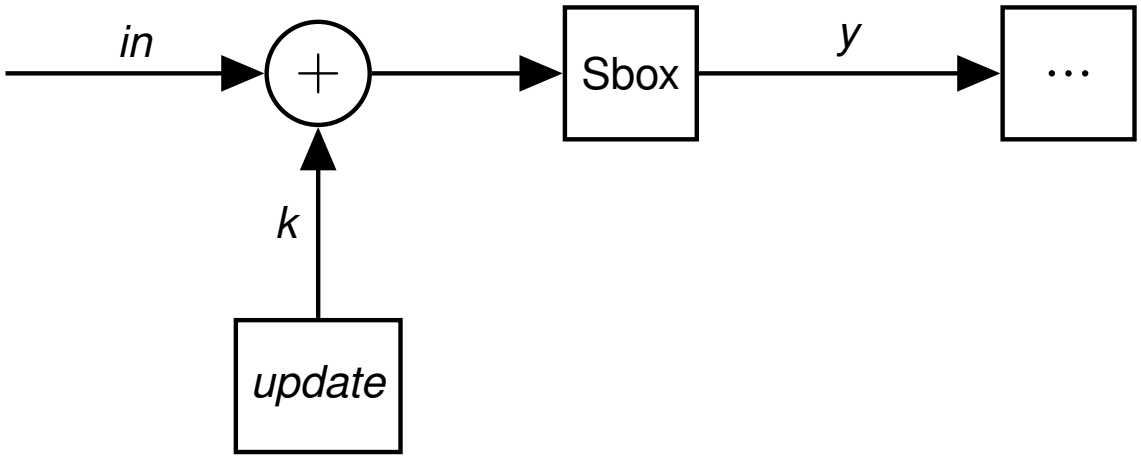


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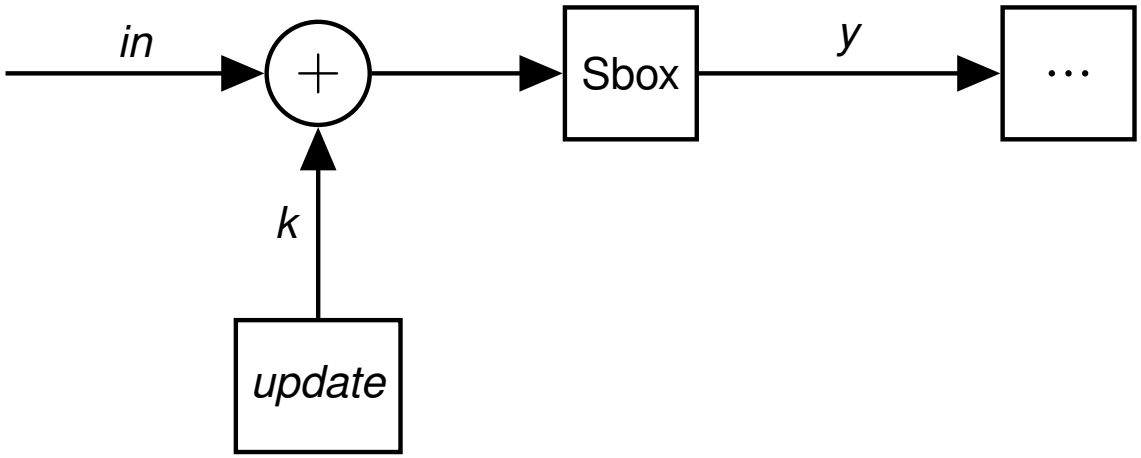


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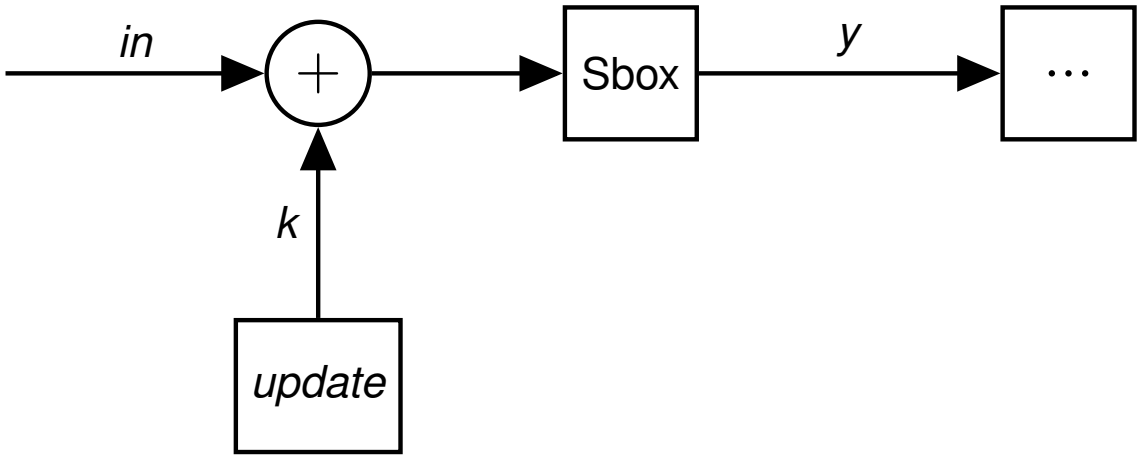


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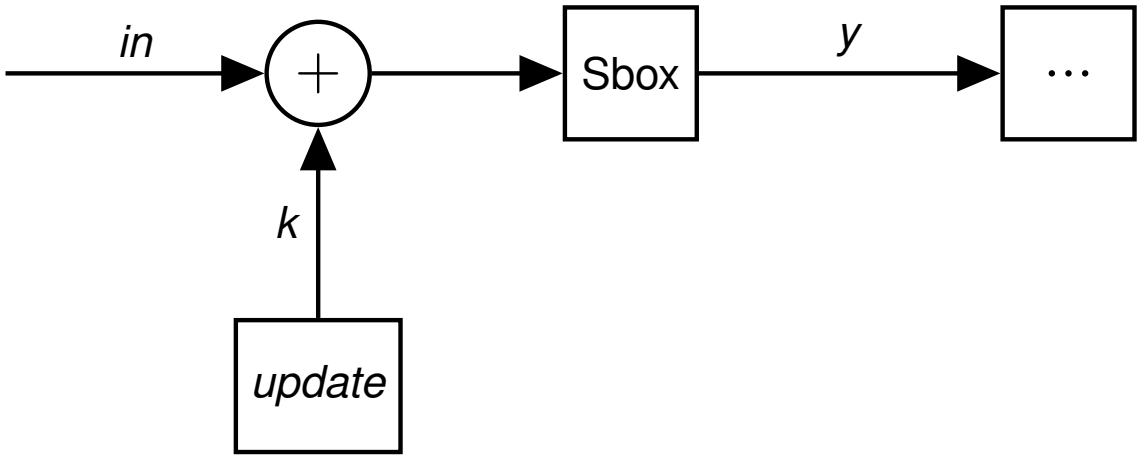


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- Throughout the attack the input $in$ is random

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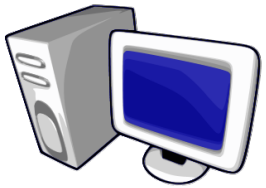
| 5 |
|---|
| 220 |
| 56 |
| 121 |
| 12 |
| 42 |

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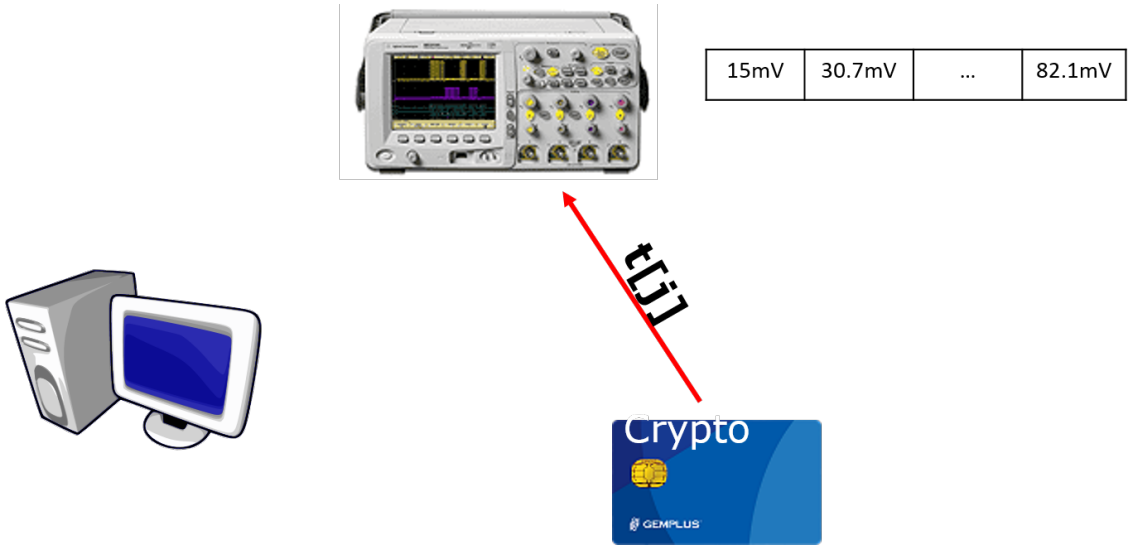
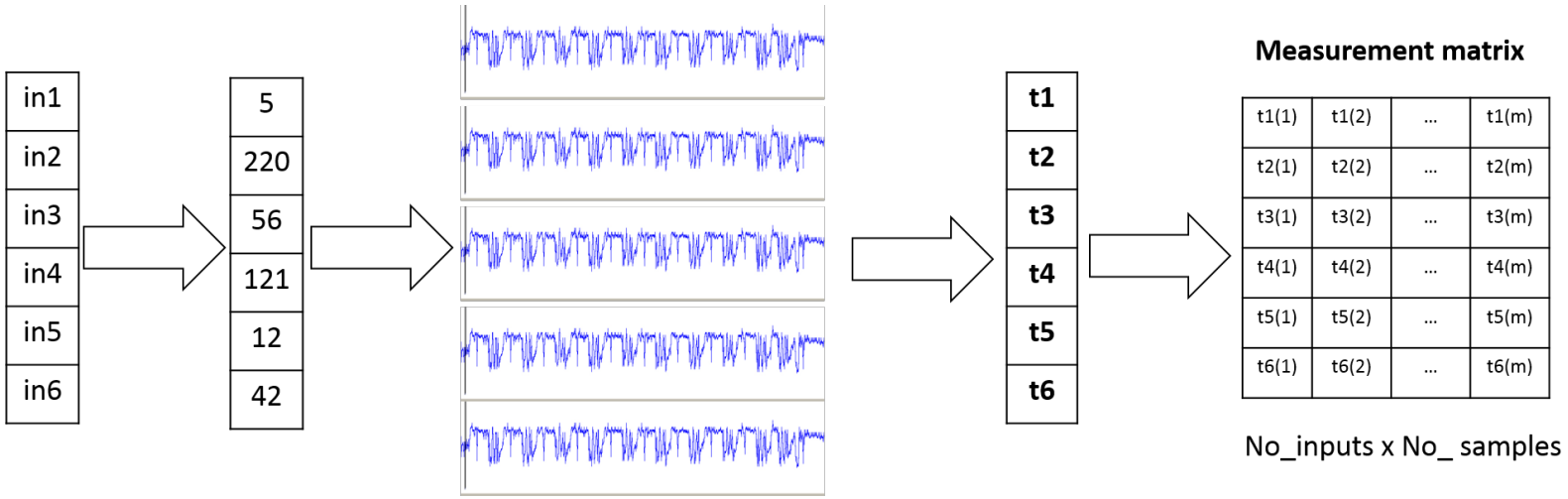


# CPA Step 2: Measure the power consumption

- Capturing 6 power traces with *m* time points (samples) results in the following measurement matrix



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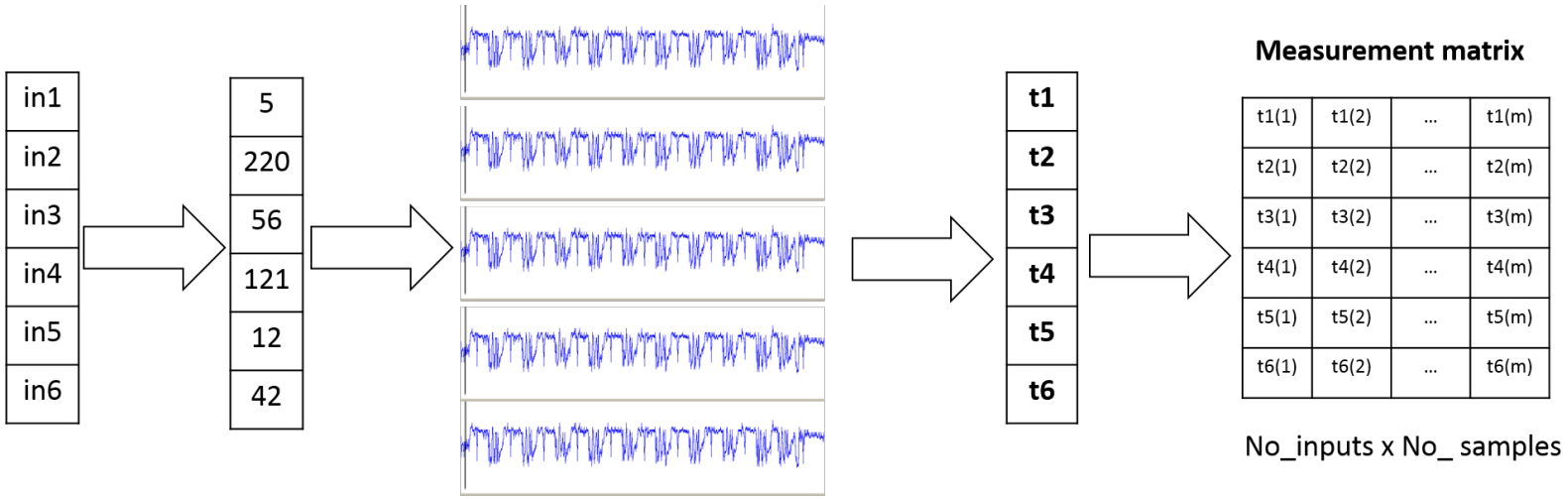


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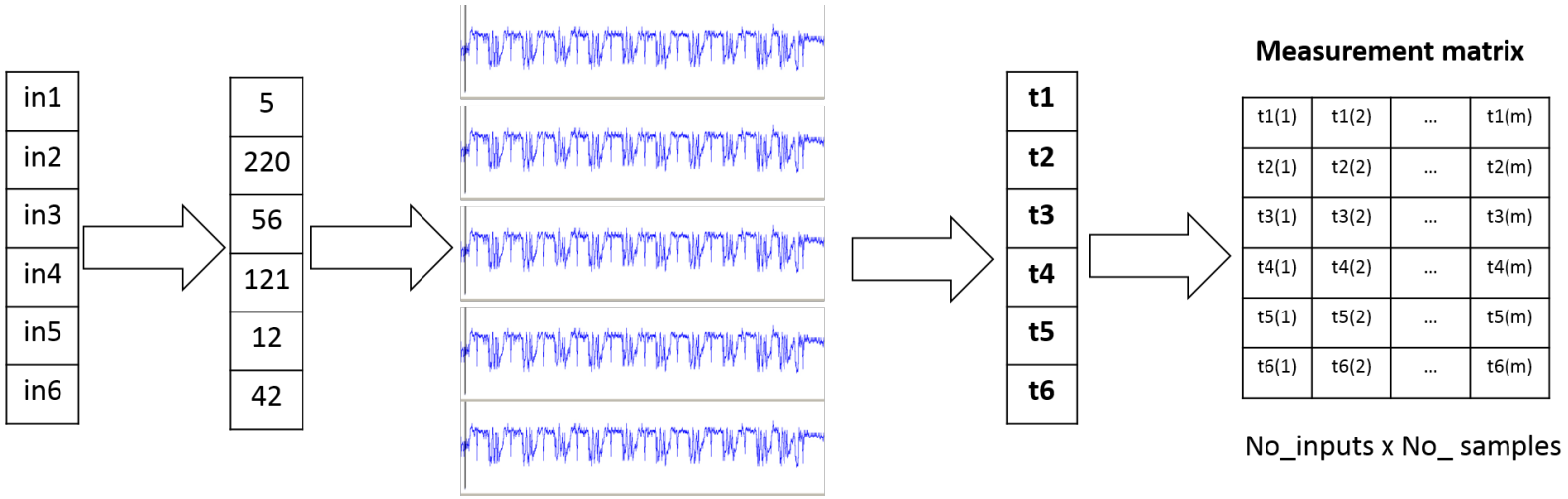


- Note that the power traces originate from the device, i.e. they are related to the secret key stored inside the device
- We will refer to the unknown key that is stored in the device as $k_{dev}$

# CPA Step 3: Predict (hypothetical) intermediate values

- In our device $y = Sbox(in \oplus k_{dev})$, but $k_{dev}$ is unknown!
- For a given input $in$ we can compute the value $y$ for all possible keys $k \in \{0, 1, \ldots, 255\}$

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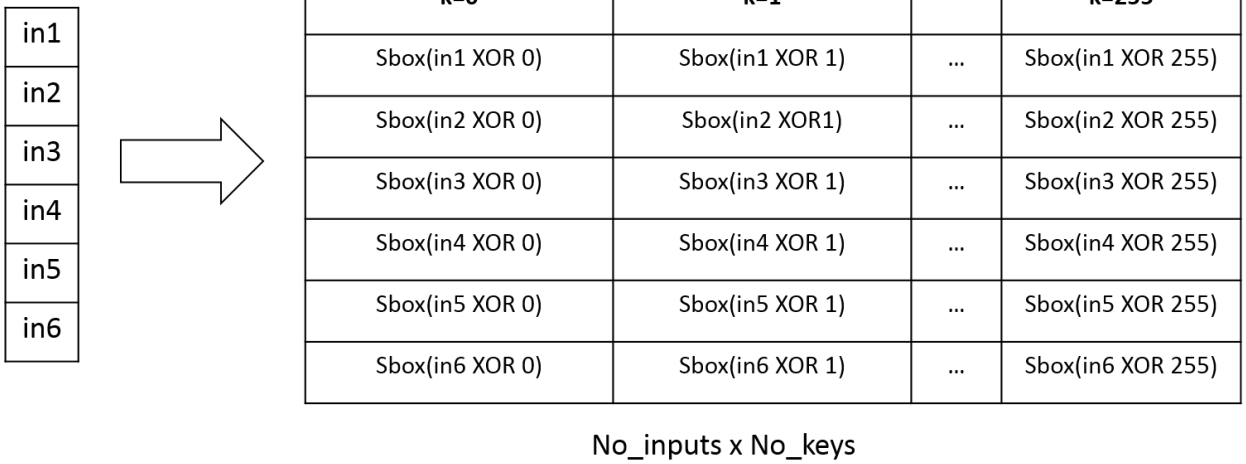


- One of the columns of this value-prediction matrix is the correct one!
- Divide and Conquer strategy

# CPA Step 4: Leakage model

- We map the hypothetical intermediate values to hypothetical power consumption values, producing the power-prediction matrix

**Power-prediction matrix**

| k=0 | k=1 | | k=255 |
|---|---|---|---|
| HW(Sbox(in1 XOR 0)) | HW(Sbox(in1 XOR 1)) | ... | HW(Sbox(in1 XOR 255)) |
| HW(Sbox(in2 XOR 0)) | HW(Sbox(in2 XOR1)) | ... | HW(Sbox(in2 XOR 255)) |
| HW(Sbox(in3 XOR 0)) | HW(Sbox(in3 XOR 1)) | ... | HW(Sbox(in3 XOR 255) |
| HW(Sbox(in4 XOR 0)) | HW(Sbox(in4 XOR 1)) | ... | HW(Sbox(in4 XOR 255)) |
| HW(Sbox(in5 XOR 0)) | HW(Sbox(in5 XOR 1)) | ... | HW(Sbox(in5 XOR 255)) |
| HW(Sbox(in6 XOR 0)) | HW(Sbox(in6 XOR 1)) | ... | HW(Sbox(in6 XOR 255)) |

No_inputs x No_keys

- A common choice is Hamming weight but keep in mind that other models may be applicable

# CPA Step 5: Comparison

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Pearson correlation coefficient $\rho_k(L, HW(V_g))$ for leakage $L$, Hamming weight of the intermediate value computed $HW(V)$ and key guess $K_g$ :

$$\rho_k(L, HW(V_g)) = \frac{cov[L, HW(V_g)]}{\sqrt{Var[L] \cdot Var[HW(V_g)]}} \tag{1}$$

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