CPE 233 – Winter 2011

Experiment ~~2~~ 2 - Revised

Universal Shift Register

Objectives:

- ✓ To understand the design and operation of a Universal Shift Register.
- ✓ To reinforce your understanding of the VHDL concatenation operation (&) and how it is utilized to piece a vector together out of various parts of a vector or individual bits.

Note on this Revision to Experiment #3: This experiment has been reduced in scope to suite the goals of CPE 233 one-day experiments. The initial experiment required that various shift functions such as Arithmetic Shift Left be implemented. This functionality is NOT part of this experiment and it will be included in the experiment in which the ALU will be constructed. Please see below for revised instructions.

General Notes: A universal shift register is typically a rising-edge triggered device, is n-bits long (or wide) and is generally capable of one four operations upon each activating clock edge, e.g. rising edge. These universal shift register operations are: Hold, Parallel Load, Shift Left, and Shift Right. Please see notes in Lecture #7 of CPE 229 Lecture Notes for more information regarding the implementation of a universal shift register.

Experiment Overview:

1. Implement the universal shift register from Lecture #7 in the CPE 229 notes in VHDL and synthesize. You will not run this in hardware but rather only test it with a simulator.
2. Use a VHDL self-checking test bench to verify Hold (Sel = 00), Load (Sel = 01), Shift Right (Sel = 10), and Shift Left (Sel = 11) modes of the universal shift register.

Required Test Cases:

1. Load "10110000", hold 2 clocks, and then shift right 8 bits with DR_IN = 1 and DL_IN = 0.
2. Load "11001010" and shift left 8 bits with DR_IN = 1 and DL_IN = 0.

Specific Required Deliverables for Lab Report:

1. Commented VHDL code 8-bit universal shift register.
2. Commented VHDL test bench.
3. Screen shot of test bench graphical waveform output in ModelSim.
4. Screen shot of ModelSim console output showing all test cases working properly and a screenshot of the same console output with a bit changed to cause a failure at some point during the simulation and hence an error on the console output.

Questions:

1. What determines the maximum clock speed of a universal shift register? Please give your answer in the form of detailed equation which incorporates all required parameters.
2. What application could a universal shift register be used for?