Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
ONLINE
SEMESTER II
SESSION 2020/2021

COURSE NAME	:	EMBEDDED SYSTEMS DESIGN
COURSE CODE	:	BEC41703
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JULY 2021
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS OPEN BOOK EXAMINATION

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) For embedded system designs of consumer electronic applications such as entertainment devices and kitchen appliances, list **FOUR (4)** critical design metrics.

(4 marks)

(b) FPGA can be used to develop embedded systems such as high performance computing systems and health monitoring systems because of hardware-customized systems as well as higher energy efficiency.

(i) Analyse the challenges of designing using FPGA for such applications.
(4 marks)

(ii) Between SRAM, FLASH and anti-fuse FPGA technology, select the most suitable technology for wearable devices in terms of high logic density, configurability and non-volatile requirements. Justify your answer.

(4 marks)

Q2 **Figure Q2** provides the specifications for quality control vision system in a food manufacturing factory. Answer the following questions:

- **TWO** (2) cameras capture images of packaged products placed on a conveyor at high speed
- If the captured images match certain defective criteria in a database, trigger motorised arms to remove products from the conveyor
- Priority setting for specific functions: 1 (highest priority) – interrupt from emergency buttons, 2 – cameras taking photos of products, 3 (lowest priority) – motorised robotic arms to remove products

Figure Q2

(i) Decide whether hard real time or soft real time is most suitable for the application.

(2 marks)

(ii) Give **TWO (2)** reasons for your answer in **Q2(i)**.

(4 marks)

(iii) Elaborate the concept of preemptive scheduling in RTOS based on the priority setting described in **Figure Q2**.

(4 marks)

(iv) Explain **TWO** (2) drawbacks of using RTOS in the embedded systems design.
(4 marks)

Q3 (a) A new embedded system application to be developed consists of hardware and software development. The application requires RTOS to process real time execution. In the hardware software co-design flow, analyse how RTOS is considered in partitioning, scheduling and allocation to develop the application.

(6 marks)

(b) List **FOUR** (4) design metrics in embedded systems design that can be optimized using hardware software co-design flow.

(4 marks)

Q4 (a) The Arduino Mega and Raspberry Pi 4 memory specifications are shown in **Figure Q4(a)(i)** and **Figure Q4(a)(ii)**. Compare the platforms in terms of the ability to support RTOS, complex embedded applications and low power requirements based on the given specifications.

Arduino Mega
• 256 KB Flash Memory (8 KB used by bootloader) • 8 KB SRAM • 4 KB EEPROM

Figure Q4(a)(i)

Raspberry Pi 4
• 1GB, 2GB, 4GB or 8GB LPDDR4 with on-die ECC (error correction code) • Micro SD card

Figure Q4(a)(ii)

(6 marks)

(b) Summarize the relation between speed to the bandwidth and power consumption for LPDDR memory architecture.

(4 marks)

Q5 (a) For each application type and its characteristics shown in **Table Q5**, determine the suitability of Zynq-7000 FPGA. Justify your answers.

Table Q5(a)

No.	Application type and characteristics	Suitability of Zynq-7000 FPGA
1	Automatic watering and fertilizing system for nursery plant – to control amount and timing to water and fertilizer	(1)
2	Vertical farming automation system – to control light, water, air flow, humidity, temperature and nutrient continuously	(2)
3	Real time wearable health monitoring devices – continuous monitoring of patient's vital signs for immediate emergency response	(3)
4	New medical imaging equipment for cancer diagnostic – intensive computational requirement in short time	(4)
5	Body camera for police force using machine learning application to identify wanted criminal in real time – high accuracy, fast detection, enable progressive system optimization	(5)

(20 marks)

(b) You are developing an embedded system application using Zynq-7000 FPGA. The application requires high performance operation through parallel processing using multicore architecture. Suggest **ONE** (1) design method related to programmable logic (PL) section in the Zynq-7000 FPGA to incorporate parallel processing for the application.

(2 marks)

Q6 Based on the following specifications, select a suitable communication interface between UART, I2C, SPI and CAN protocol to be connected to the main processor or microcontroller in an embedded system. Justify your answers.

(i) low data transfer rate but up to 10 devices connected.

(4 marks)

(ii) high accuracy data transfer with multi master

(4 marks)

Q7 (a) List **FOUR** (4) types for software testing.

(4 marks)

(b) Analyse the relation between the number of testing to be conducted and the testing time to the testing costs for complex embedded systems design.

(4 marks)

(c) Examine the challenges of testing embedded systems with RTOS.

(4 marks)

Q8 Given the C++ code shown in **Figure Q8** that convert a 6-digit-max hexadecimal string (allowable digits are 0-9, a-f, A-F) to its equivalent integer value, answer the following questions:

(i) Suggest **THREE** (**3**) possible methods to conduct black box testing based on the given code.

(6 marks)

(ii) Suggest **THREE** (**3**) possible methods to conduct white box testing based on the given code.

(6 marks)

```
1   int htoi(const char s[])
2   {
3       int i = 0;
4       int ans = 0;
5       int valid = 1;
6       int hexit;
7
8       if(s[i] == '0')
9       {
10          ++i;
11          if(s[i] == 'x' || s[i] == 'X'){ ++i; }
12      }
13
14      while(valid && s[i] != '\0')
15      {
16          ans = ans * 16;
17          if(s[i] >= '0' && s[i] <= '9')
18          {
19              ans = ans + (s[i] - '0');
20          }
21          else
22          {
23              hexit = hex2int(s[i]);
24              if(hexit == 0){ valid = 0; } else { ans = ans + hexit; }
25          }
26          ++i;
27      }
28
29      if(!valid) { ans = 0; }
30
31      return ans;
32  }
```

Figure Q8

– END OF QUESTIONS –