

**Faculty of Electrical and Electronic Engineering**

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**BEJ42203**

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**Report Title: Pollution based Traffic Control**

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# 1. Project Introduction

The European Environment Agency reports that “[c]ars, vans, trucks and buses produce more than 70 % of the overall greenhouse gas emissions from transport”[1]. Especially in cities, where many vehicles drive, health limits for fine particle matter get exceeded. Governments and cities are now curious to find fast solutions. The most recent is Abu Dhabi, they are starting a project where “AI-techniques will […] provide recommendations to improve traffic light efficiency, thus also reducing congestion and carbon emissions” [2]. Its goal is to reduce stop time at intersections, especially at those having high pollution levels.

This is also the goal of this project. To reach the environment protecting goal faster, a simpler system shall be established. This system will be able to measure the fine dust level at a conjunction and act. A suiting hardware needs to be designed. Additional to the light signal and magnetic loop a standard traffic light has, it needs sensors for air quality and a display to show the current pollution level. As the ZYNQ 7000 is a good architecture to read all this information, do complex processing and give output to the traffic light and display, it will be used.

The junction of this project has one main road, with one side road crossing it. This project will show how to establish such a traffic control system hardware. Therefor the report will discuss the project objectives, followed by an analysis of the hardware architecture. This is followed by a presentation of the results, a discussion and a conclusion.

# 2. Project Objectives

The project objective is to develop a traffic control system using the Zynq-7000 xxxxx. Further specified objectives can be found in the following list:

|  |  |
| --- | --- |
| No. | Description |
| 1. | Analyze which hardware components will be used. |
| 2. | Design the hardware architecture of the traffic control system using the Vivado software. Analyze performance. |
| 3. | Optimize the hardware and compare performance with the hardware state before optimizing. |

# Project Architecture

This chapter will explain the hardware and how it got developed. The project consists of five main components. The ZYNQ 7000, that takes the inputs, makes the calculations and create outputs. There are two input sensors. The first is a fine dust sensor. The fine dust value will determine the pollution of the junction. The higher the fine dust level is, the higher is the pollution. The second sensor type is an inductive sensor. There will be two, each in the side road parts of the junction. As output there are the signals for the display and the traffic lights.

## DIGILENT 410 248 Zedboard Zynq 7000 Arm FPGA/Soc Development Board ...3.1 Top level block diagram

**2**

**4**

**1**

Input Board Output

|  |  |  |  |
| --- | --- | --- | --- |
| No. | Name | Description | Connection  **5** |
| 1 | Zynq 7000  **3** | Development board | - |
| 2 | HM3301 | Fine dust sensor | IIC |
| 3 | BES R03KC-PSF30B-EP02 | Inductive sensor | Digital input (Normally open) |
| 4 | SBC - OLED01 | OLED Display | IIC |
| 5 | BB-LED-TL-CC | LED traffic light | GPIO for 12 LED |

Figure 3.1: Block Diagram with list

Figure 3.1 shows the components of the system, and how they are be connected. The list below gives their name, describe their function and how they are connected to the ZYNQ. The fine dust sensor and the OLED Display are both using the IIC protocol. The inductive sensor provides a digital value, that state if an object has been recognized. As each of the four sides of the junction has a traffic light, the GPIO has 12 exit pins to reach each of the lights.

## 3.2 Hardware blocks

Figure 3.2 Hardware block diagram

The architecture of the hardware design is displayed in Figure 3.2. The used blocks are the ZYNQ7 Processing System, a Processor System Reset block, a open source block that manages the traffic lights and a manager of onboard communication in form of the AXI-Interconnect block. This has three blocks connected, two AXI-IIC for the IIC communication and one GPIO block for all the traffic lights….

To use the open-source hardware, a new IP Package needs to be created. The package is created as AXI4 peripheral. The logic is used from [5]. The Variables are as listed in the table below:

|  |  |  |
| --- | --- | --- |
| Name | Input/Output | Bit(s) |
| enable | In | 1 |
| clk | In | 1 |
| reset | In | 1 |
| car2 | In | 1 |
| car4 | In | 1 |
| state | In | 2 |
| nextstate | Out | 2 |
| l13 | Out | 2 |
| l24 | Out | 2 |
| d1 | In | 4 |
| d2 | In | 4 |
| d3 | In | 4 |
| d4 | In | 4 |
| setbit | Out | 4 |
| q | Out | 4 |
| delay | Out | 4 |

Table x: Ports of the traffic light controller

For creating the registers of the new IP Block, the above listed variables are sorted by being an output or input. They got further separated by their area of use, extern or intern. The four registers slv\_reg their variables can be seen in the table below:

|  |  |  |
| --- | --- | --- |
| Connection description | slv\_reg | Variables |
| Inter input | 0 | enable, state, d1, d2, d3, d4 |
| Extern input | 1 | car2, car4 |
| Inter output | 2 | state, nextstate, q, delay |
| Extern output | 3 | l13, l24 |

Table x: AXI-Peripheral register definition

## 3.3 Operation

## 3.4 Design Flow

## 3.5 Sustainability and reliability

# 4. Results

# 5. Discussion

# 6. Conclusion

# 7. References

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| [6] |  |