EE103 Intro to VLSI Design

Lab 3 Study of Characteristics of CMOS Inverters

Objective:

- Lab 3 is mainly about using HSPICE simulation tool to explore the inverter characteristics and buffer design.
- The **DUE DATE** for this Lab report is **POSTED ON CANVAS**.

Laboratory Tasks:

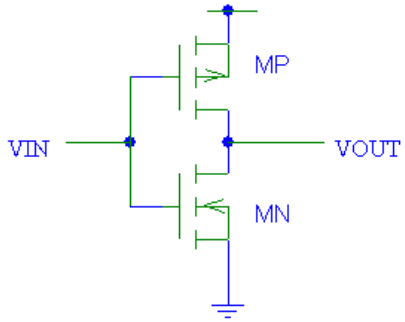
- Learn the characteristics of CMOS inverter design.

Assignment:

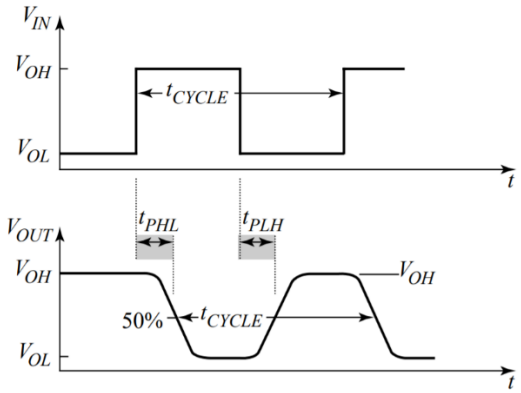
1. Construct a CMOS inverter. The first part includes the Vin and some basic parameters are given in the HSPICE code at the end of this file. For both nmos and pmos, w=300n, L=100n.

   M1 d g gnd! b n105 W=300n L=100n
   **syntax: Model_name Drain Gate Source Bulk Model (Width; Length; etc.)*

   Use '6p' for all the rise time and fall time of the input pulse.



2. Definitions of waveforms: (Example code is attached at the end of the assignment)



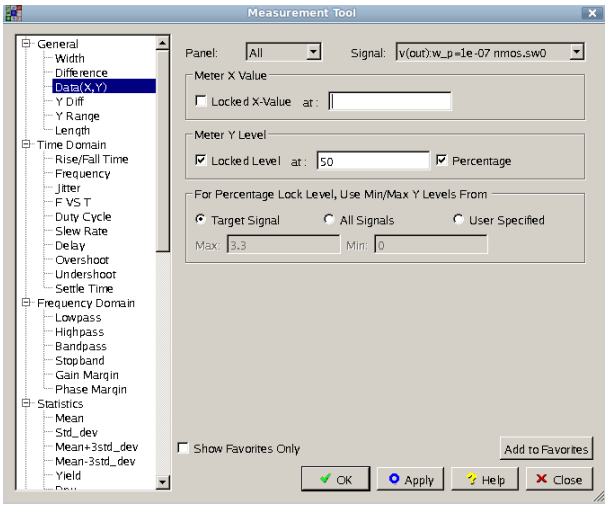
$\boldsymbol{t_{pHL}}$: $delay\ from\ input\ 50\%\ to\ outupt\ 50\%\ when\ output\ is\ \boldsymbol{falling}.$

$\boldsymbol{t_{pLH}}$: $delay\ from\ input\ 50\%\ to\ outupt\ 50\%\ when\ output\ is\ \boldsymbol{rising}$

First read the definitions of the waveform. Then measure the **rise time and fall time** of the **output** signal and **propagation delay (t_{pHL} & t_{pLH})**. Both of the information is measured via the **second** rising/falling edge of input voltage. Take a screenshot of the measurement result in the .lis file and attach it in the report.

3. Analyze the DC characteristic of the CMOS inverter (one graph):
    a. Set the **Length** of the NMOS and PMOS as a constant: 100n; **Width** of the NMOS as a constant: 300n.
    b. DC analysis the **VIN (x axis)** from 0 to 1.05v with a step of 0.01v
    c. Change the Beta ratio of the NMOS and PMOS by sweeping the **Width** of PMOS from 100n to 1000n with a step of 100n.
    d. View the **VOUT (y axis)** plot.

4. Use the measurement tool (shown below) and the graph in problem 3 to find the closest **Width** value of the PMOS that has the **Switching Threshold** closest to half of the Vdd (Vdd/2). <u>We will use this ***balanced inverter*** for the following tasks.</u>



5. Set the **Width** of the PMOS to be the value you found in part 4.In this part, you are required to discover one of the characteristics of the CMOS inverter: **delay(Tp)** as a function of **Vdd**. Now set the **Width** of the PMOS to be the value you found in part 4. Use the HSPICE *.alter* command to change the value of the parameter 'vdd' so that the supply voltage will change: 0.5:0.1:1.05

    .alter statements allows us to modify the circuit and run again.

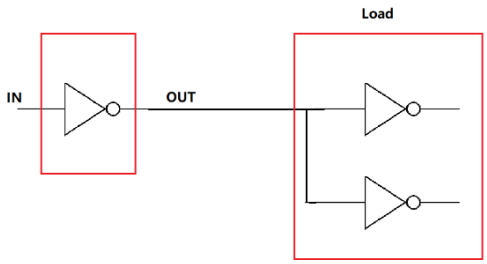
```
*vdd default value 1.05v
.param vdd = 1.05

*start to use .alter to run the hspice code multiple times
.alter
.param vdd = 0.5
.alter
.param vdd = 0.6
…
.alter
.param vdd = 1.05
```

This essentially will do 6 simulations for different vdd values. The results will only be included in one '.lis' file, but the waveforms will be stored in multiple .tr files as .tr0, .tr1….. You need to measure the **inverter delay (Tp)** corresponding to different supply voltage. Remember, you need to measure both $\mathbf{t_{pHL}}$ and $\mathbf{t_{pLH}}$ in order to get the delay **Tp**.
After you have found the inverter delay for each **Vdd**, you need to plot these data (**Vdd** being X axis, and **Tp** being Y axis) using any proper tool (e.g., excel, Matlab).
Hint: *.alter* command is to run the simulation multiple times under different parameters. Therefore, normally you will have many output graphical file (e.g. tr#, sw#). Since you only need to check the measurement in the '.lis' file, it is recommended to avoid generating these files. You can achieve this by commenting the *.option post* at the beginning of the HSPICE scripts.

6. In this part, you are required to plot the **device sizing** versus **delay Tp,** similar to the graph that is on the p.30 in the *VLSI-CMOS inverter.pdf*. Similar to part 5, where you need to measure Tp with different Vdd, here you need to measure **Tp** with different **size** of CMOS inverter:

   1:1:6 multiples of the width (both nmos and pmos) in the **balanced inverter** you obtained in part 3.

   Also, keep the length fixed and connect the output of the balanced inverter to a load (two balanced inverters which are exactly the same as you obtained in part 4) (see the schematic below). Also, similar to the part 5, you need to *.alter* command. Then, use appropriate tool to plot the data (**Width** being X axis, and **Tp** being Y axis).



Submission Requirements

- Parts 2-6: Take appropriate screenshots of the plots. Take part 4 as an example, you need to take a screenshot of the information that proves you have found the appropriate PMOS width for switching threshold equals Vdd/2

Reference HSPICE code for 1-6:

```
*this is an inverter spice file for the Lab5, part2

.lib '/usr/commercial_amd64/synopsys/libraries/SAED32_EDK/tech/hspice/saed32nm.lib' TT
.include
'/usr/commercial_amd64/synopsys/libraries/SAED32_EDK/lib/stdcell_rvt/hspice/saed32nm_rvt.spf'

*post the results
.option post
.global vdd gnd

*define model
.model n105 nmos level=54
.model p105 pmos level=54

*source declaration
vvdd vdd 0 vdd   *syntax:vname pos_node neg_node voltage_value
vgnd gnd 0 0v

M1 vo vi gnd gnd n105 W=300n L=l
M2 vo vi vdd vdd p105 W=300n L=l

*define parameters
.param vdd = 1.05
.param l = 100n
.param trf = 6p *initial rise/fall time of the transient source
.param del = 1u
.param pw = 1u
.param per = 2u

*define analysis voltage

vinput vi gnd pulse 0 vdd del trf trf pw per

.tran 1p 6u

.measure tran outrise
```

```
+trig v(vo) val='vdd*0.1' rise=2
+targ v(vo) val='vdd*0.9' rise=2

.measure tran outfall
+trig v(vo) val='vdd*0.9' fall=2
+targ v(vo) val='vdd*0.1' fall=2

.measure tran tphl
+trig v(vi) val='vdd*0.5' rise=2
+targ v(vo) val='vdd*0.5' fall=2

.measure tran tplh
+trig v(vi) val='vdd*0.5' fall=2
+targ v(vo) val='vdd*0.5' rise=2

.end
```