# Lab 1 VLSI

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## 1 Intro

The objectives of this lab are to investigate some major MOS transistor characteristics using the simulation tool HSPICE. In this experiment, we will simulate several behaviors of NMOS and PMOS transistors and plot visual data with WaveView. We are going to plot these behaviors in such a way that we try to determine the mathematical functions describing them, as introduced in the theoretical part of this course. The key simulations include plotting graphs for parameters: IDS vs VGS and IDS vs VDS, sub-threshold swing, body effect, and DIBL amongst others.

Note for all simulations but the one where we vary length the dimensions of the transistors are W/L = 300nm/100nm.

# 2 $I_{ds}$ versus $V_{gs}$ (for different $V_{ds}$)

## 2.1 Relevant Equations and Info)

For both NMOS and PMOS transistors, the drain current $I_{ds}$ depends on the gate-source voltage $V_{gs}$ and the drain-source voltage $V_{ds}$. The relationship between $I_{ds}$ and $V_{gs}$ varies for different values of $V_{ds}$, and can be summarized as follows:

In NMOS transistors:

- For small $V_{ds}$, the transistor operates in the linear region, where $I_{ds}$ increases linearly with $V_{gs}$ for a given $V_{ds}$.
- For larger $V_{ds}$, the transistor enters saturation, and $I_{ds}$ becomes independent of $V_{ds}$ and primarily depends on $V_{gs}$.
- As $V_{gs}$ increases beyond the threshold voltage $V_{th}$, $I_{ds}$ increases more significantly.

In PMOS transistors (operating with negative voltages):

- $I_{ds}$ increases with decreasing $V_{gs}$ (which is negative) for different values of $V_{ds}$.
- Similar to NMOS, PMOS transistors also have a linear region for small $V_{ds}$ and a saturation region for larger $V_{ds}$.
- As $V_{gs}$ becomes more negative (beyond the threshold voltage), the current $I_{ds}$ increases.

For both NMOS and PMOS, the $I_{ds}$ versus $V_{gs}$ characteristics show different behavior for different $V_{ds}$ values, with $I_{ds}$ increasing more significantly as $V_{gs}$ surpasses the threshold voltage.

The most relevant equation for this is the Unified MOS Model Regions:

$$I_d = 0 \quad \text{for} \quad V_{gt} \leq 0$$

$$I_d = k' \frac{W}{L} \left( V_{gt} V_{min} - \frac{(V_{min})^2}{2} \right) (1 + \lambda V_{ds}) \quad \text{for} \quad V_{gt} \geq 0$$

(Make sure to correctly apply the signs of the voltages and current depending on the type of MOSFET, whether NMOS or PMOS.)

## 2.2 Graph for NMOS

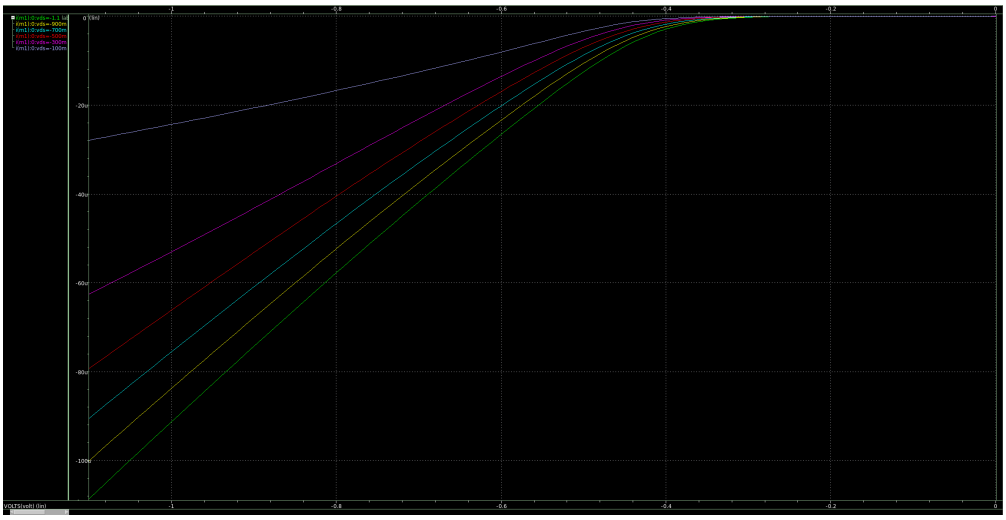

Figure 1: Plot of $I_{ds}$ versus $V_{gs}$ for a NMOS transistor, where the x-axis shows $V_{gs}$ ranging from 0 to 1.1 V. The y-axis shows $I_{ds}$ (drain current) with a range from 0 to around 175 $\mu$A, with different curves corresponding to $V_{ds}$ values ranging from 0 to 1.1 V, in 0.2 V increments.

## 2.3 Graph for PMOS

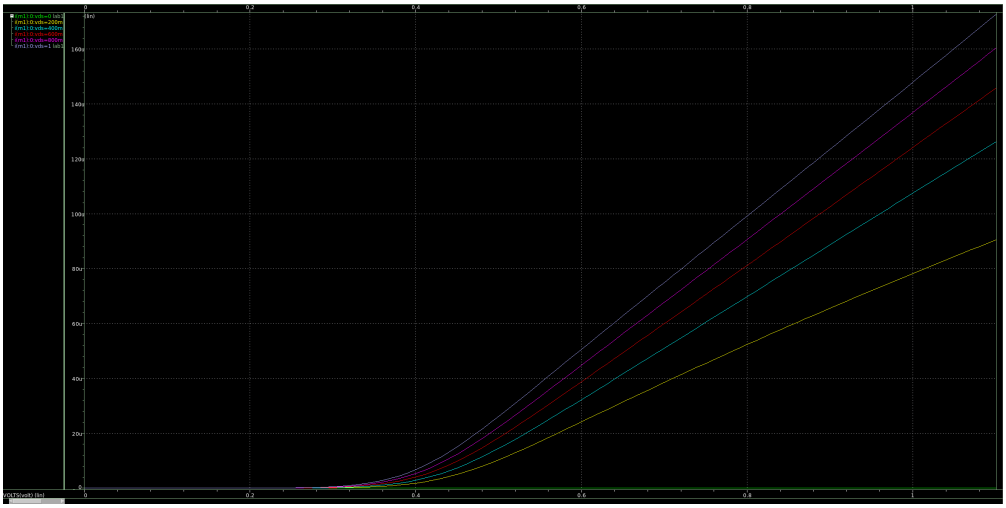

Figure 2: Plot of $I_{ds}$ versus $V_{gs}$ for an PMOS transistor, where the x-axis shows $V_{gs}$ ranging from -1.1 V to 0 V. The y-axis represents $I_{ds}$ (drain current), with a range from 0 to around -110 $\mu$A, with different curves corresponding to $V_{ds}$ values ranging from -1.1 V to 0 V, in 0.2 V increments.

# 3 $I_{ds}$ versus $V_{ds}$ (for different $V_{gs}$)

## 3.1 Relevant Equations and Info

As we have already seen, the Unified MOS Model can be utilized to describe the relationship between the drain current $I_{ds}$ versus the drain-source voltage $V_{ds}$ for various values of gate-source voltages $V_{gs}$. In the previous section, we briefly mentioned how the model controls the MOSFET behavior in the different regions of its operation.

For sufficiently small values of $V_{ds}$, the MOSFET is in the linear region (also called the triode region), where $I_{ds}$ rises roughly linearly with $V_{ds}$. The current $I_{ds}$ is also a function of the value of $V_{gs}$: the larger $V_{gs}$ is, the larger $I_{ds}$ will be. This behavior is in agreement with the expression derived from the Unified MOS Model, where the drain current is a function of both $V_{gs}$ and $V_{ds}$.

As $V_{ds}$ is increased further and the transistor enters the saturation region, $I_{ds}$ becomes less dependent on $V_{ds}$ and is primarily dependent on $V_{gs}$. Within this region, $I_{ds}$ remains virtually constant as $V_{ds}$ is increased further. The second part of the equation of the Unified MOS Model captures this: when in saturation, $I_{ds}$ is independent of $V_{ds}$. When $V_{gs}$ is less than the threshold voltage $V_{th}$, $I_{ds}$ is approximately zero due to the transistor being turned off, also captured by the Unified MOS Model.

## 3.2 Graph for NMOS

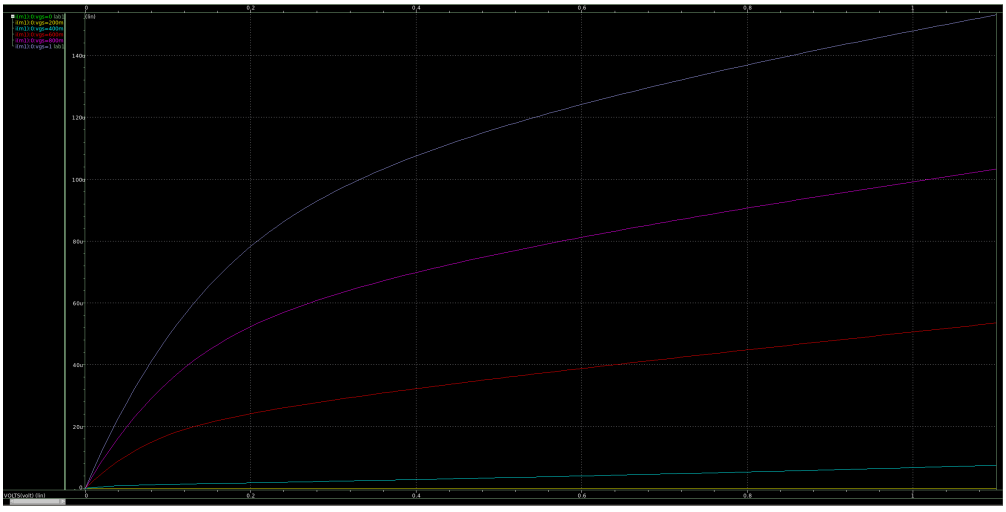

Figure 3: Plot of $I_{ds}$ versus $V_{gs}$ for an NMOS transistor, where the x-axis shows $V_{gs}$ ranging from 0 V to 1.1 V. The y-axis represents $I_{ds}$ (drain current), with a range from 0 to around 155 $\mu$A, with different curves corresponding to $V_{gs}$ values ranging from 0 V to 1.1 V, in 0.2 V increments.

## 3.3 Graph for PMOS

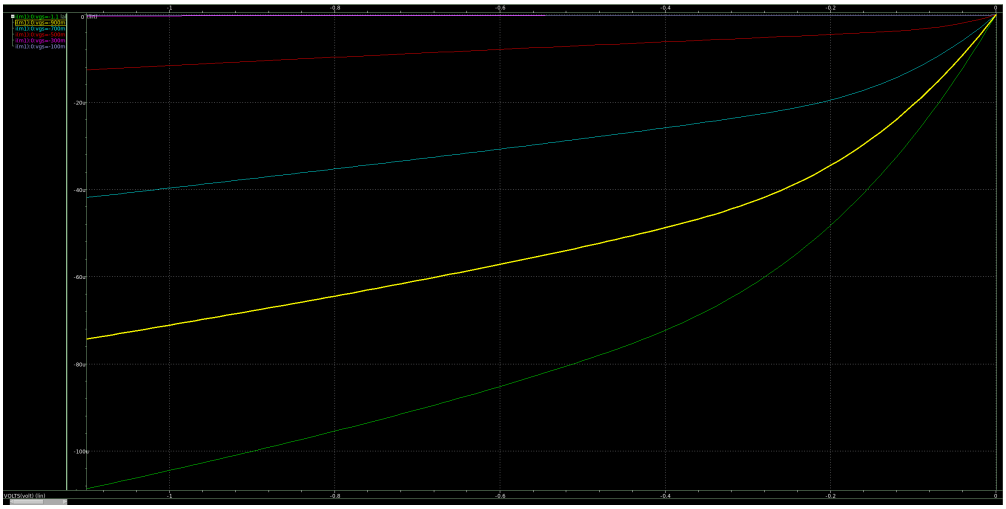

Figure 4: Plot of $I_{ds}$ versus $V_{gs}$ for a PMOS transistor, where the x-axis shows $V_{gs}$ ranging from -1.1 V to 0 V. The y-axis represents $I_{ds}$ (drain current), with a range from 0 to around -110 $\mu$A, with different curves corresponding to $V_{gs}$ values ranging from -1.1 V to 0 V, in 0.2 V increments.

# 4 Sub-threshold Swing

## 4.1 Relevant Equations and Info

**The Slope Factor**

The slope factor $n$ describes the subthreshold behavior of the MOSFET and plays a crucial role in determining how steeply the current increases as a function of gate voltage. The current in the subthreshold region can be expressed as:

$$I_D \sim I_0 e^{\frac{qV_{gs}}{nkT}}$$

where:

- $I_D$ is the drain current,
- $I_0$ is the pre-exponential constant,
- $V_{gs}$ is the gate-source voltage,
- $q$ is the electronic charge,
- $k$ is the Boltzmann constant,
- $T$ is the temperature in Kelvin,
- $n$ is the slope factor.

The slope factor $n$ is given by:

$$n = 1 + \frac{C_D}{C_{ox}}$$

where:

- $C_D$ is the depletion layer capacitance,
- $C_{ox}$ is the oxide capacitance.

**Subthreshold Swing (S)**

The subthreshold swing $S$ is defined as the change in gate-source voltage ($\Delta V_{GS}$) required to change the drain current by one decade (i.e., when $\frac{I_{D2}}{I_{D1}} = 10$). This can be expressed as:

$$S = n \left( \frac{kT}{q} \right) \ln(10)$$

Here, $S$ is typically expressed in millivolts per decade (mV/dec), and it determines how effectively the MOSFET can switch between off and on states. A smaller value of $S$ corresponds to a steeper subthreshold slope and better switching performance. The subthreshold swing depends on the slope factor $n$, and as the depletion layer capacitance $C_D$ increases relative to the oxide capacitance $C_{ox}$, the slope factor $n$ increases, leading to a larger subthreshold swing.

## 4.2 Graph for NMOS

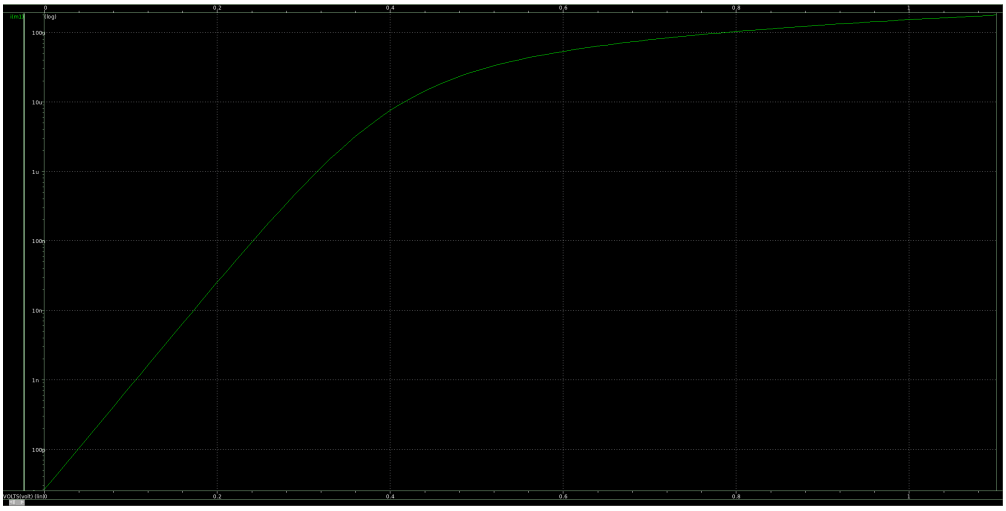

Figure 5: Plot of $I_{ds}$ versus $V_{gs}$ for an NMOS transistor. The x-axis shows $V_{gs}$ ranging from 0 V to 1.1 V, while the y-axis represents $I_{ds}$ on a logarithmic scale. The drain-source voltage ($V_{ds}$) is held constant at 1.1 V.

## 4.3 Graph for PMOS

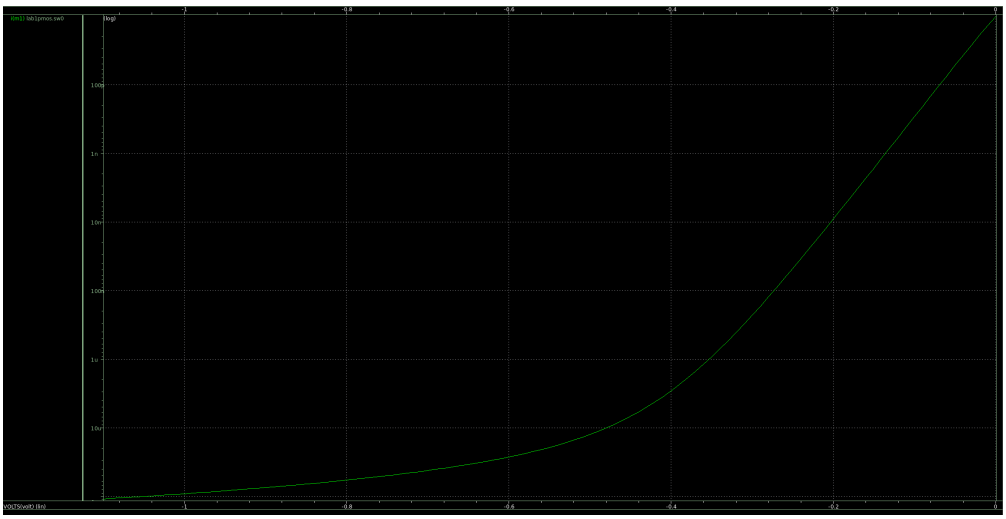

Figure 6: Plot of $I_{ds}$ versus $V_{gs}$ for a PMOS transistor. The x-axis shows $V_{gs}$ ranging from -1.1 V to 0 V, with the y-axis in logarithmic scale. The drain-source voltage ($V_{ds}$) is held constant at -1.1 V.

# 5 Body Effect

## 5.1 Relevant Equations and Info

The Body Effect describes how the threshold voltage $V_{th}$ changes with the source-bulk voltage $V_{sb}$, and can be expressed as:

$$V_{th} = V_{th0} + \gamma \left( \sqrt{V_{sb} + \phi_F} - \sqrt{\phi_F} \right)$$

where $V_{th0}$ is the threshold voltage when $V_{sb} = 0$, $\gamma$ is the body-effect coefficient, and $\phi_F$ is the surface potential.

For small source-to-body voltage $V_{sb}$, the body effect can be approximated linearly as:

$$V_t = V_{t0} + k_\gamma V_{sb}$$

where

$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si} N_A}{v_T \ln \frac{N_A}{n_i}}}}{2C_{ox}}$$

## 5.2 Graph for NMOS

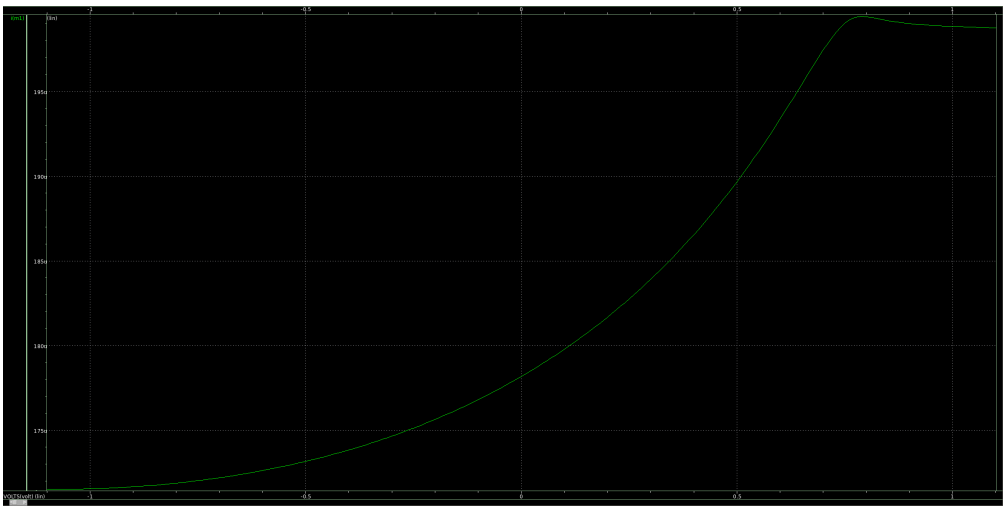

Figure 7: Plot of $I_{ds}$ versus $V_{bs}$ for an NMOS transistor, illustrating the body effect. The x-axis shows $V_{bs}$ ranging from -1.1 V to 1.1 V. The y-axis represents $I_{ds}$ (drain current), with a range from approximately 170 $\mu$A to 200 $\mu$A. Both $V_{gs}$ and $V_{ds}$ are held constant at 1.1 V. The graph demonstrates the impact of Gate-to-Source voltage, Drain-to-Source voltage, and Body-to-Source voltage on the transistor's behavior.

## 5.3 Graph for PMOS

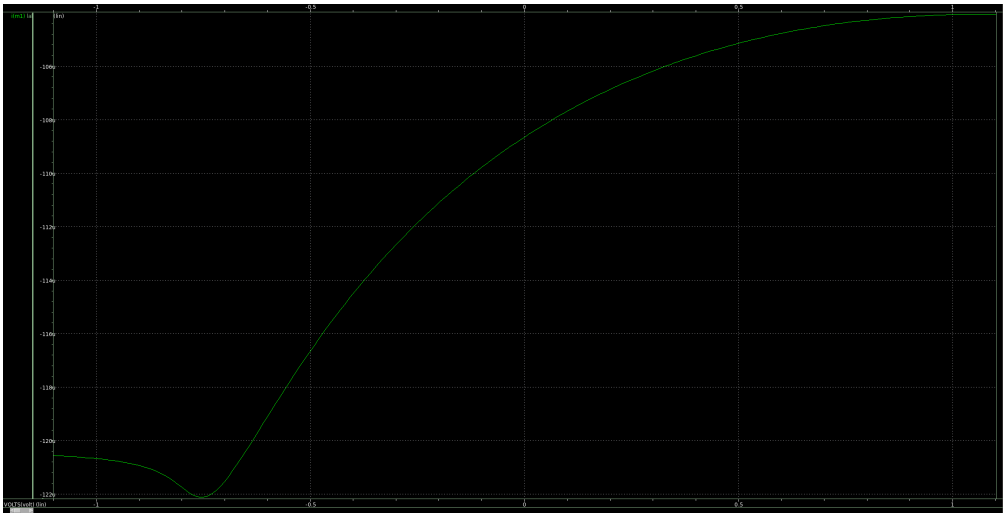

Figure 8: Plot of $I_{ds}$ versus $V_{bs}$ for a PMOS transistor, illustrating the body effect. The x-axis shows $V_{bs}$ ranging from -1.1 V to 1.1 V. The y-axis represents $I_{ds}$ (drain current), with a range from approximately -104 $\mu$A to -122 $\mu$A. Both $V_{gs}$ and $V_{ds}$ are held constant at -1.1 V. The graph highlights the impact of Gate-to-Source voltage, Drain-to-Source voltage, and Body-to-Source voltage on the transistor's behavior.

# 6 DIBL (Drain-induced barrier lowering) ($V_{ds}$ versus $V_{th}$)

## 6.1 Relevant Equations and Info

In a short-channel MOSFET, the source and drain regions each support a significant fraction of the total channel depletion charge $Q_{dep} \times W \times L$. As a result, the threshold voltage $V_{th}$ is lower than that of a long-channel MOSFET.

As the drain voltage $V_{ds}$ increases, the reverse bias on the body-drain PN junction increases, causing the drain depletion region to widen. This leads to a reduction in the threshold voltage:

$$V_{th} \text{ decreases with increasing drain bias.}$$

The reduction in the threshold voltage occurs because the barrier to carrier diffusion from the source into the channel is reduced. Consequently:

$$I_D \text{ increases with increasing drain bias.}$$

This phenomenon is known as **Drain-Induced Barrier Lowering (DIBL)**, where the increase in $V_{ds}$ lowers the potential barrier and effectively reduces $V_{th}$, leading to increased current.

$$V_{th} \propto \frac{1}{V_{ds}}$$

## 6.2 Graph for NMOS

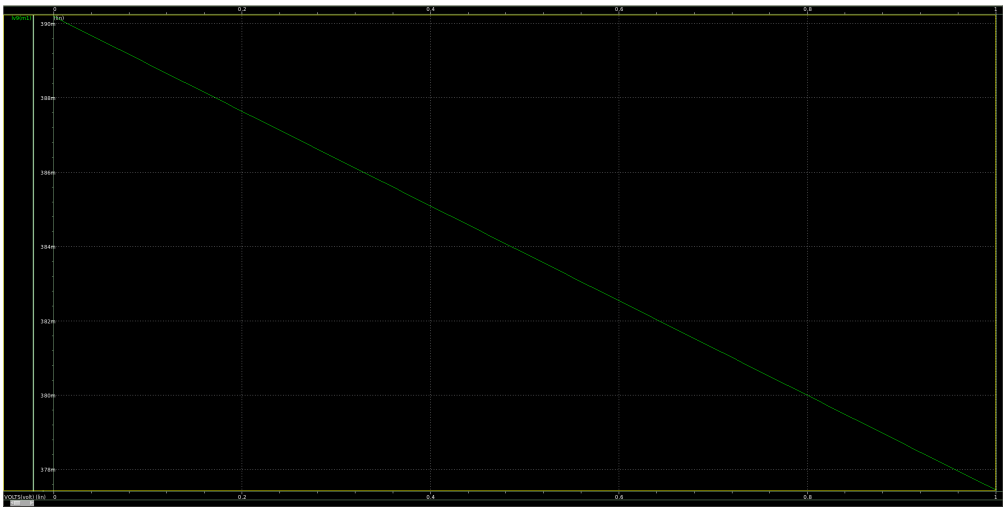

Figure 9: The plot shows the Drain-Induced Barrier Lowering (DIBL) effect, where $V_{ds}$ (drain-source voltage) is plotted against $V_{th}$ (threshold voltage) for an NMOS transistor. The x-axis represents $V_{ds}$ ranging from 0 V to 1.1 V, and the y-axis shows $V_{th}$ ranging from approximately 390 mV to 378 mV. The gate-source voltage ($V_{gs}$) is held constant at 1.1 V.

## 6.3 Graph for PMOS

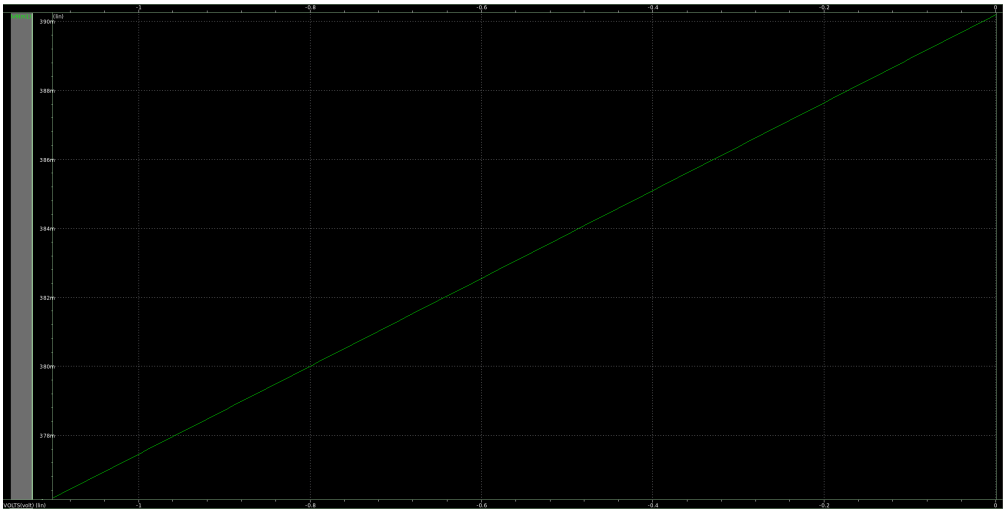

Figure 10: The plot shows the Drain-Induced Barrier Lowering (DIBL) effect, where $V_{ds}$ (drain-source voltage) is plotted against $V_{th}$ (threshold voltage) for a PMOS transistor. The x-axis represents $V_{ds}$ ranging from -1.1 V to 0 V, and the y-axis shows $V_{th}$ ranging from approximately 377 mV to 390 mV.

# 7 DIBL (Drain-Induced Barrier Lowering) (Length vs $V_{th}$)

## 7.1 Relevant Equations and Info

DIBL is one of the most important short-channel effects, which designates the threshold voltage $V_{th}$ reduction as a function of channel length $L$ reduction or drain-source voltage $V_{ds}$ increase. This can be understood as in the case of short-channel devices, the electric field coming from the drain gives an important contribution to the potential barrier between the source and the channel.

When the channel length $L$ is reduced, the depletion regions coming from the source and drain encroach into the channel. This reduces the effectiveness of the gate in controlling the channel potential, which in turn reduces the threshold voltage. Due to DIBL, the relation between $L$ and $V_{th}$ can be written as:

$$\Delta V_{th} \propto -\frac{1}{L}$$

That is, the reduction of $V_{th}$ will be more significant for smaller channel lengths. The reduction of $V_{th}$ is due to a lowering of the potential barrier by the electric field of the drain, which in turn makes it easier for carriers to be injected from the source into the channel. This, in turn, increases the subthreshold current and degrades the ability of the device to switch off completely (for both PMOS and NMOS).

The threshold voltage $V_{th}$ decreases with increasing $V_{ds}$ as a result of DIBL. This effect becomes more pronounced as the channel length $L$ is reduced. The dependency of the drain voltage on the threshold voltage is given by the relation:

$$\Delta V_{th} \approx -\text{DIBL} \cdot V_{ds}$$

Where:

- DIBL is the DIBL coefficient, or a measure of the sensitivity of $V_{th}$ versus changes in $V_{ds}$.
- $L$ is the channel length, and the smaller the length, the worse the effect.
- $V_{ds}$ is the drain-source voltage.

In general, DIBL results in a reduction of $V_{th}$ with a reduction of $L$, and the drain voltage $V_{ds}$ acts to further reduce it. This short-channel effect is highly important in the design of a MOSFET since this factor influences device performance in submicron and nanoscale technologies.

## 7.2 Graph for NMOS

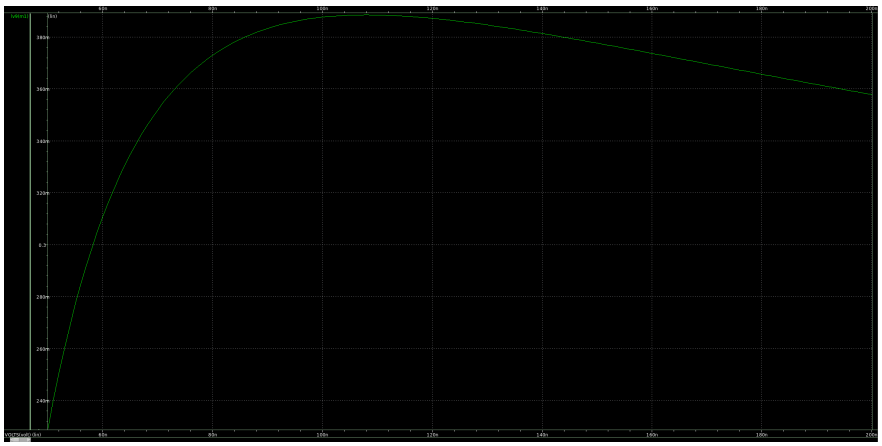

Figure 11: The plot shows the Drain-Induced Barrier Lowering (DIBL) effect, where the channel length is plotted against $V_{th}$ (threshold voltage) for an NMOS transistor. The x-axis represents the channel length ranging from 50 nm to 200 nm, and the y-axis shows $V_{th}$ (threshold voltage) ranging from approximately 230 mV to 390 mV. The drain-source voltage ($V_{ds}$) is set to 0.2 V. The graph demonstrates how the threshold voltage initially increases with the channel length, reaching a peak around 110 nm, and then decreases, which is characteristic of the DIBL effect in NMOS transistors.

## 7.3 Graph for PMOS

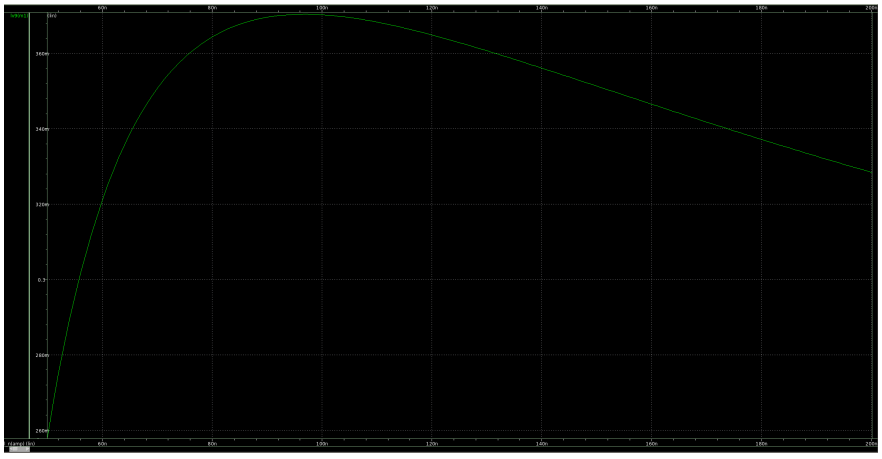

Figure 12: The plot shows the Drain-Induced Barrier Lowering (DIBL) effect, where the channel length is plotted against $V_{th}$ (threshold voltage) for a PMOS transistor. The x-axis represents the channel length ranging from 50 nm to 200 nm, and the y-axis shows $V_{th}$ (threshold voltage) ranging from approximately 260 mV to 370 mV. The drain-source voltage ($V_{ds}$) is set to 0.2 V. The graph demonstrates how the threshold voltage initially increases with the channel length, peaking around 95 nm, before decreasing, which is characteristic of the DIBL effect in PMOS transistors.

# 8 Temperature versus $V_{th}$

## 8.1 Relevant Equations and Info

According to the slides in class and readings the threshold voltage $V_{th}$ is **inversely proportional** to temperature. As the temperature increases, the threshold voltage decreases, which can be approximately expressed as:

$$V_{th} \propto \frac{1}{T}$$

This inverse relationship is due to the increase in intrinsic carrier concentration and the narrowing of the semiconductor band gap with increasing temperature. Thus, as temperature $T$ increases, the threshold voltage $V_{th}$ decreases. (for both PMOS and NMOS)

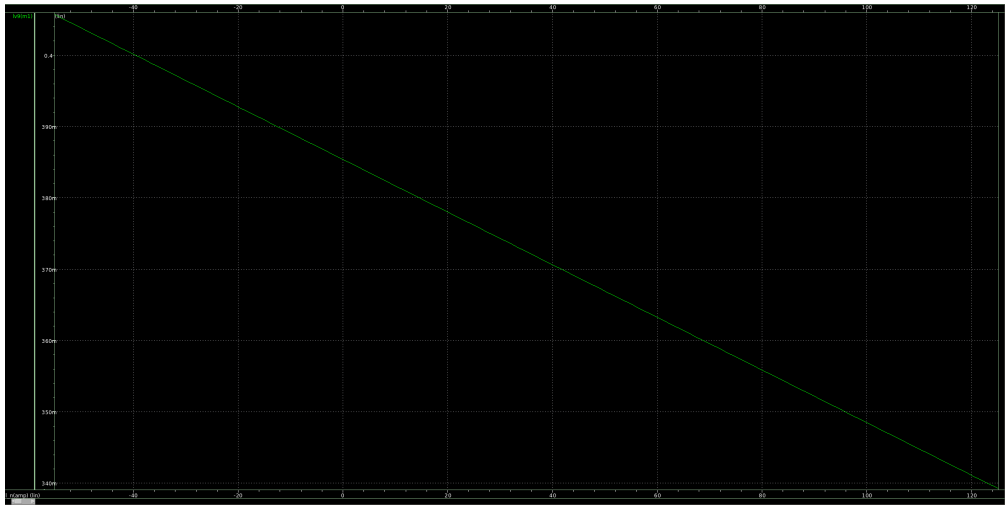


Figure 13: The plot shows the relationship between temperature and $V_{th}$ (threshold voltage) for an NMOS transistor. The x-axis represents temperature ranging from -55° to 125°C, while the y-axis shows $V_{th}$ (threshold voltage) ranging from approximately 400 mV to 340 mV.

## 8.2 Graph for PMOS

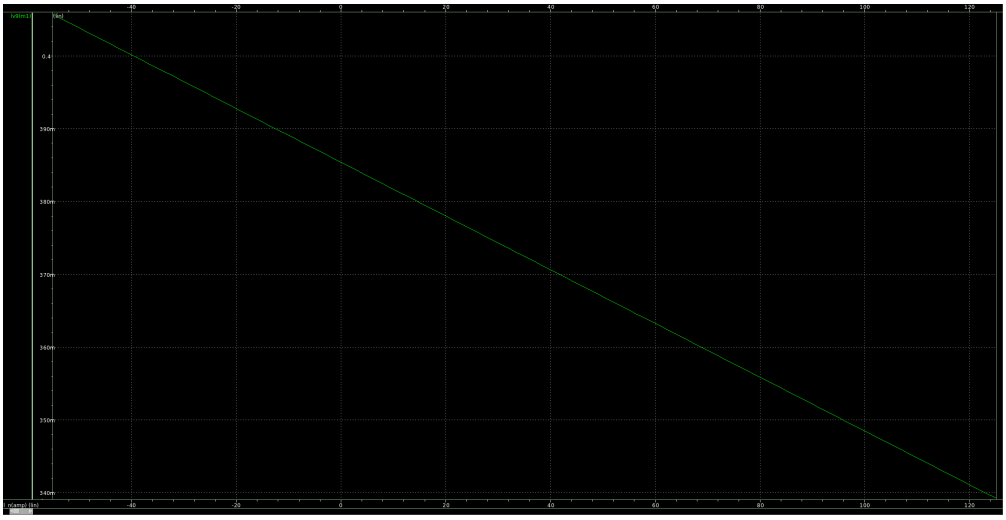

Figure 14: The plot shows the relationship between temperature and $V_{th}$ (threshold voltage) for an PMOS transistor. The x-axis represents temperature ranging from -55° to 125°C, while the y-axis shows $V_{th}$ (threshold voltage) ranging from approximately 400 mV to 340 mV. (Interesting how it is basiclly the same as the graph for NMOS)

# References

[1] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Addison-Wesley, 2011, ISBN: 0321547748.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed., Prentice-Hall, 2003, ISBN: 0130909963.

[3] *Intro to VLSI Design: Transistor*, Lecture Slides, EE-103 course, accessed 2024.

[4] *Intro to VLSI Design*, Lecture Slides, EE-103 course, accessed 2024.