EE103 Intro to VLSI Design

Lab 1: Study of Characteristics of a MOS Transistor

Objective:

- Lab 1 is mainly about using HSPICE simulation tool to explore the MOS transistor characteristics learnt from class. Lab 1 will be using HSPICE and WaveView to generate graphs to visualize these characteristics. You need to write one lab report which includes all parts of the Lab 1.
- The **DUE DATE** for this Lab 1 report is **POSTED ON CANVAS**.

Laboratory Tasks:

- Use what you have learned and the HSPICE code as a reference to plot the graphs required in the assignment session.
- Include the equations related to these plots.

Assignment: (W=300n, L=100n for all transistors by default)

- Use HSPICE and WaveView to generate a graph on **Ids versus Vgs (for different Vds)** for both NMOS and PMOS.
    - Vgs: [0, 1.1]; Vds: 0: 0.2: 1.1 (NMOS)(min:step:max)
    - Vgs: [-1.1, 0]; Vds: -1.1: 0.2: 0 (PMOS)
- Use HSPICE and WaveView to generate a graph on **Ids Versus Vds (for different Vgs)** for both NMOS and PMOS.
    - Vgs: 0:0.2:1.1; Vds: [0,1.1] (NMOS)
    - Vgs: -1.1:0.2:0; Vds: [-1.1,0] (PMOS)
- Use HSPICE and WaveView to generate a graph on **sub-threshold swing** for both NMOS and PMOS.
    - Vgs: [0,1.1]; Vds: 1.1 (NMOS)
    - Vgs: [-1.1:0]; Vds: -1.1(PMOS)
- Use HSPICE and WaveView to generate a graph on **Body Effect** for both NMOS and PMOS.
    - Vgs: 1.1; Vds: 1.1; Vbs: [-1.1,1.1] (NMOS)
    - Vgs: -1.1; Vds: -1.1; Vbs: [-1.1,1.1] (PMOS)
- Use HSPICE and WaveView to generate a graph on **DIBL (Drain-induced barrier lowering) (Vds versus Vth)** for both NMOS and PMOS.
    - Vds: [0, 1.1]; Vgs: 1.1 (NMOS)
    - Vds: [-1.1,0]; Vgs: -1.1(PMOS)
- Use HSPICE and WaveView to generate a graph on **DIBL (Drain-included barrier lowering) (Length versus Vth)** for both NMOS and PMOS.
    - Length: [50n,200n]
    - Vds: 0.2
- Use HSPICE and WaveView to generate a graph on **Temperature versus Vth** for both NMOS and PMOS. (There will be a guide for this part at the end of this file)
    - TEMP: [-55,125] (NMOS & PMOS)

- Hint: you can find most of the similar plots in the *VLSI-Transistor.pdf* uploaded to the course documents. Use it as a reference.
- Save all of the graphs generated, and write a short comment or include equations to help you explain each of these graphs. Besides, for each graph, you need to include a title (For Example: *DIBL (Length Versus Vth)*)and the simulation parameters (For example: *W/L=300nm/100nm Vgs=0.7 Vds=0.7 Vbs sweep: [-1.1,1.1]*), and in the multi-trace graphs you need to include the legend. (similar to the one below):

- Graphical Output

  A. .DC vds 0 1.05 0.1 sweep vgs 0 1.05 0.2 *Ids vs Vds

  Use WaveViewer to open the HSPICE output and double click on the i(M1) to view Ids vs Vds

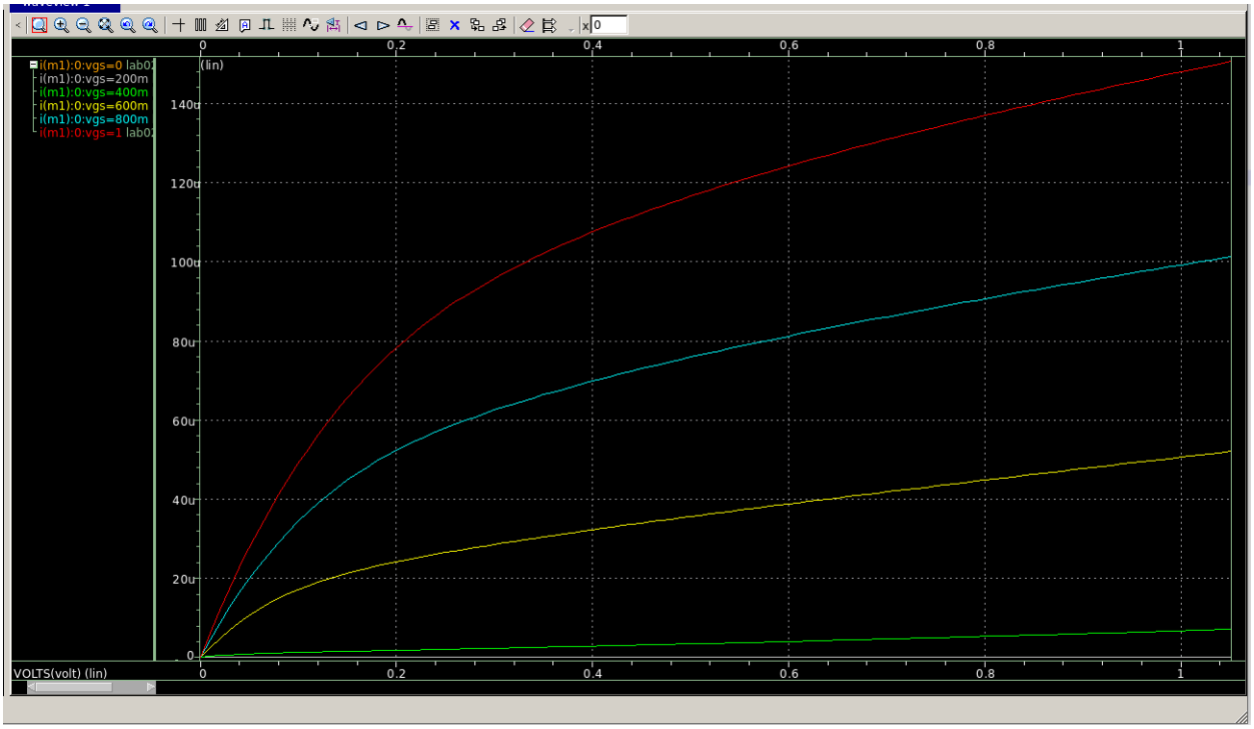
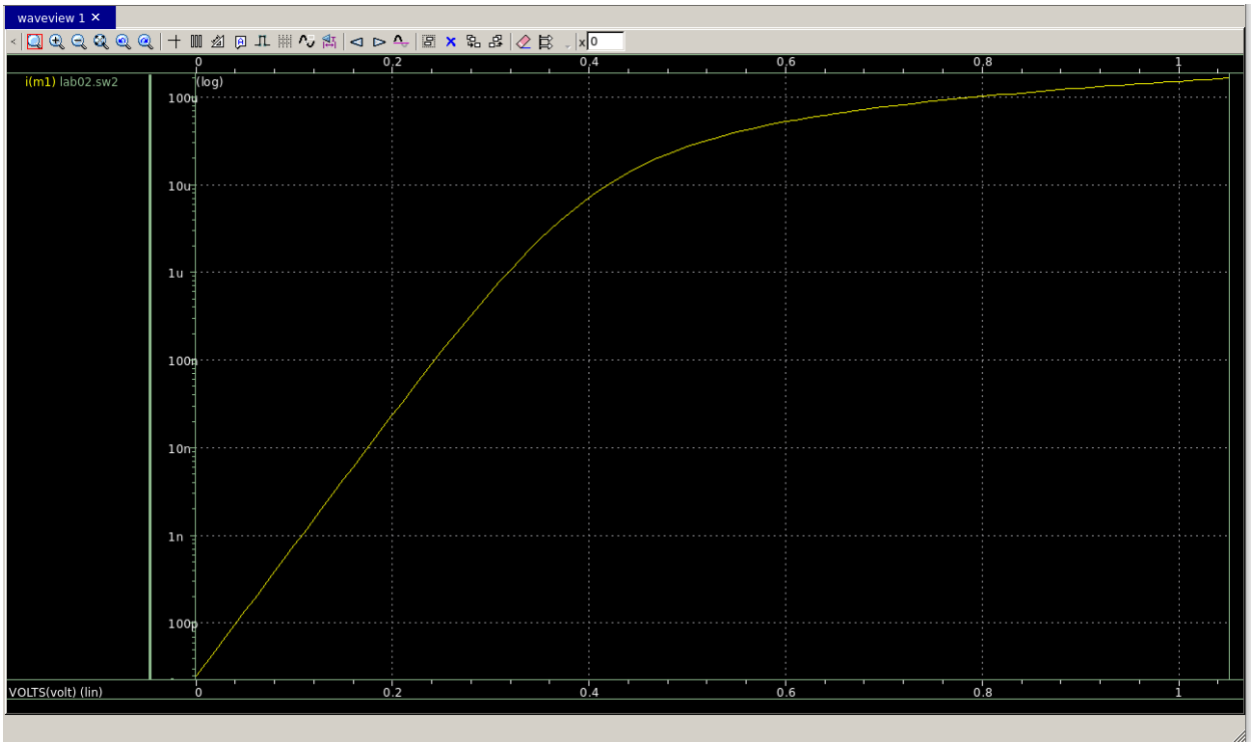


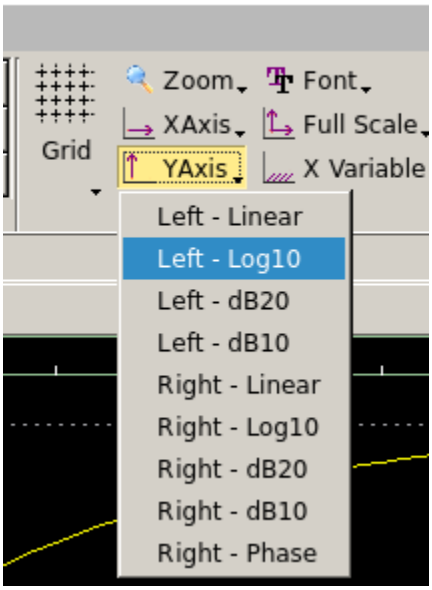
Figure 1

B. .DC vgs 0 1.05 0.01 *vgs vs ids sub threshhold

This is the graph of the sub-threshold swing for NMOS. X-axis is Vgs, while Y-axis is the decibel of transistor current.



Setting Y-axis to be decibel (log10)



HSPICE code and Tutorial:

```
*library file
.lib '/usr/cots/synopsys/UniversityLibrary/SAED32_EDK/tech/hspice/saed32nm.lib' TT
.include
'/usr/cots/synopsys/UniversityLibrary/SAED32_EDK/lib/stdcell_rvt/hspice/saed32nm_rvt.spf'

*post the results
.option post
.GLOBAL gnd vdd

vgs g gnd 1.05
vds d gnd 1.05
vbs b gnd 0

.model n105 nmos level=54

M1 d g gnd b n105 W=300n L=100n
*syntax: Model_name Drain Gate Source Bulk Model (Width; Length; etc.)


vvdd vdd 0 1.05v
vgnd gnd 0 0v

.dc vds 0 1.05 0.01 sweep vgs 0 1.05 0.2        *Ids vs Vds
.dc vgs 0 1.05 0.01                      *vgs vs ids  sub threshhold
.dc temp -55 125 5

*M1 d g gnd b n105 W=300n L=l_n
*.dc l_n 20n 150n 1n


*.PROBE DC i(M1)                    *probe transistor current (Ids)
*.PROBE DC i(M2)
*.PROBE lv9(M1)                     *probe threshold voltage  (Vt)
*.PRINT lv9(M1)                      *print and store all the swept threshold voltage value in .lis
file
.end
```