Tufts
UNIVERSITY

EE-103 VLSI Design
Lab 01 Study of Characteristics of a MOS Transistor

Kaiyuan Zhang

kzhang11@tufts.edu

Outline

- Get Hspice Ready
- First Hspice Script
- WaveView

Copy & Paste command after you download the slides file! Directly copy from canvas preview may have extra format issue.

Introduction to Hspice

What is Hspice

- Optimizing analog circuit simulator
- Used for steady-state, transient and frequency domains.

Hspice Input & Output files

- Input: Hspice script (netlist file)
  - Circuit description & analysis options
  - Typical file extension: ‘.sp’. E.g. inv.sp
- Output: files that contain circuit analysis results.
  - ‘.lis’ file: contains analysis error info if any
  - Different file extensions for different analysis results.

Introduction to Hspice (continue)

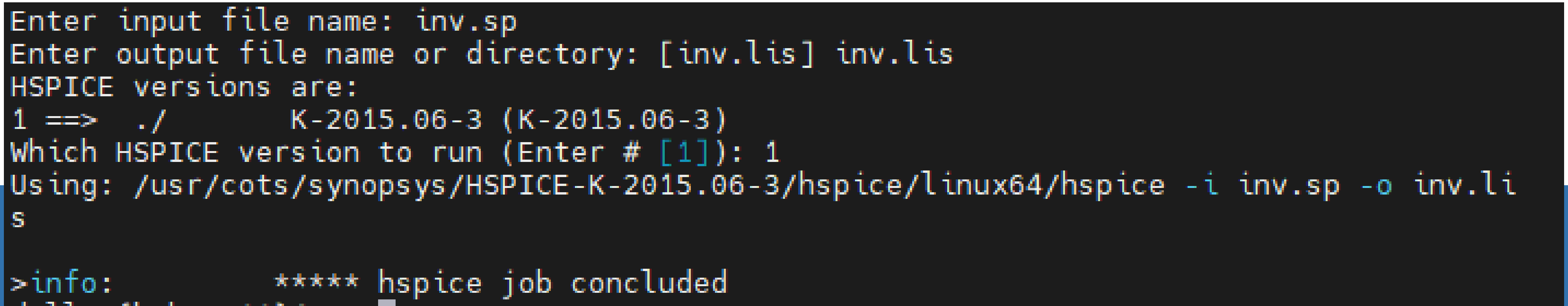
- Use command “hspice” to use Hspice and enter inv.sp
- Hit Enter for the rest commands and Hspice will generate the inv.lis and other files.
- Or you could define the input and output file name :

hspice -i inv.sp -o inv.lis

-i : specifies the input netlist file name

-o: specifies the output file name

- If succeeded:



```
Enter input file name: inv.sp
Enter output file name or directory: [inv.lis] inv.lis
HSPICE versions are:
1 ==>  ./       K-2015.06-3 (K-2015.06-3)
Which HSPICE version to run (Enter # [1]): 1
Using: /usr/cots/synopsys/HSPICE-K-2015.06-3/hspice/linux64/hspice -i inv.sp -o inv.li
s

>info:          ***** hspice job concluded
```

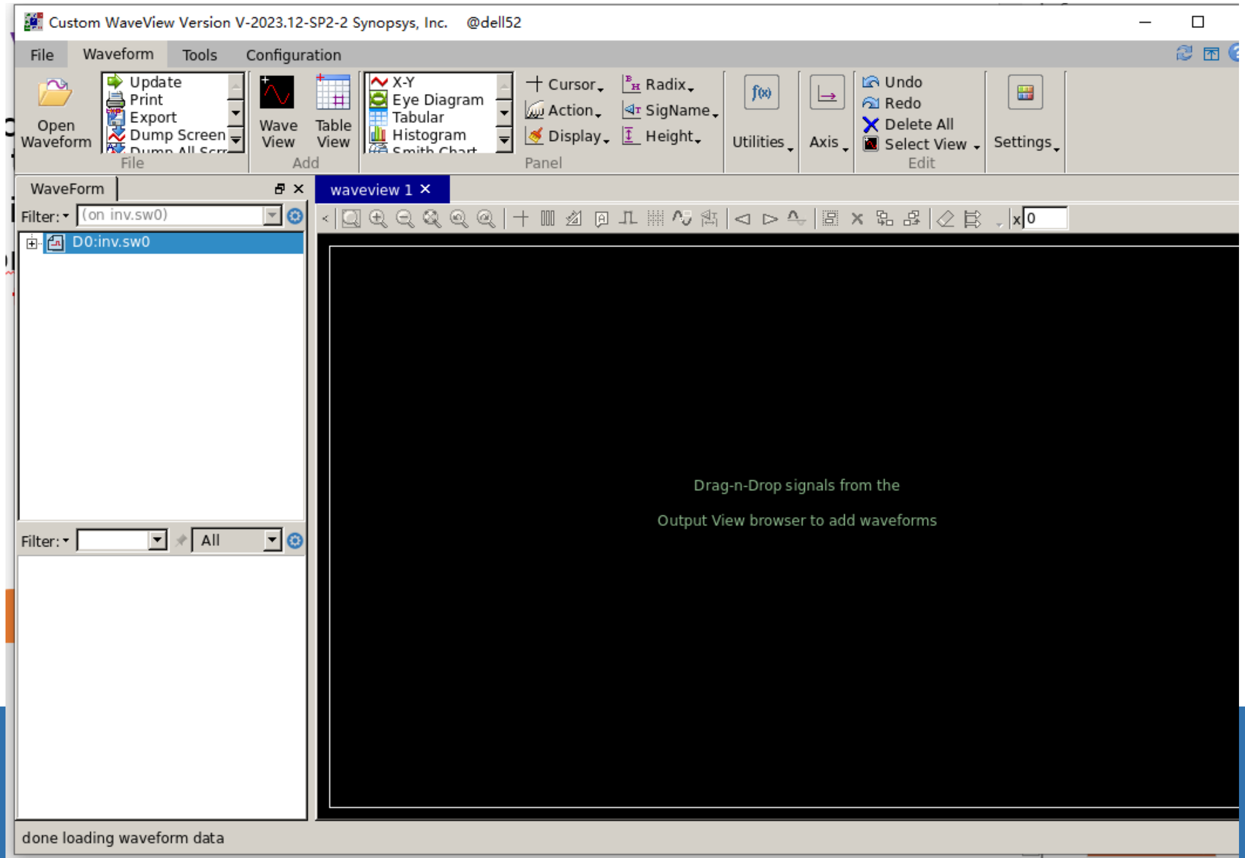
Output file Extensions

File Description	Suffix
DC analysis measurement results	.ms#
DC analysis results (from .POST statement)	.sw#
Output listing (where you can find error information)	lis, or user-specified
Output status	.st#
Transient analysis measurement results	.mt#
Transient analysis results (from .POST statement)	.tr#

WaveView

- WaveView:
  - Used for viewing graphical results of Hspice analysis
  - Embedded inside the Synopsys

WV



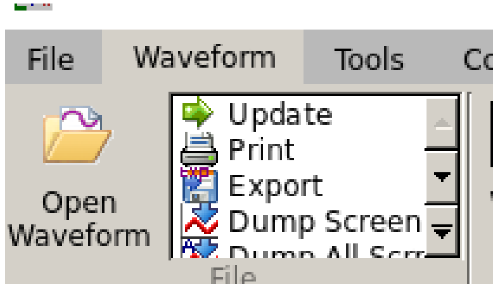
Custom WaveView Version V-2023.12-SP2-2 Synopsys, Inc. @dell52

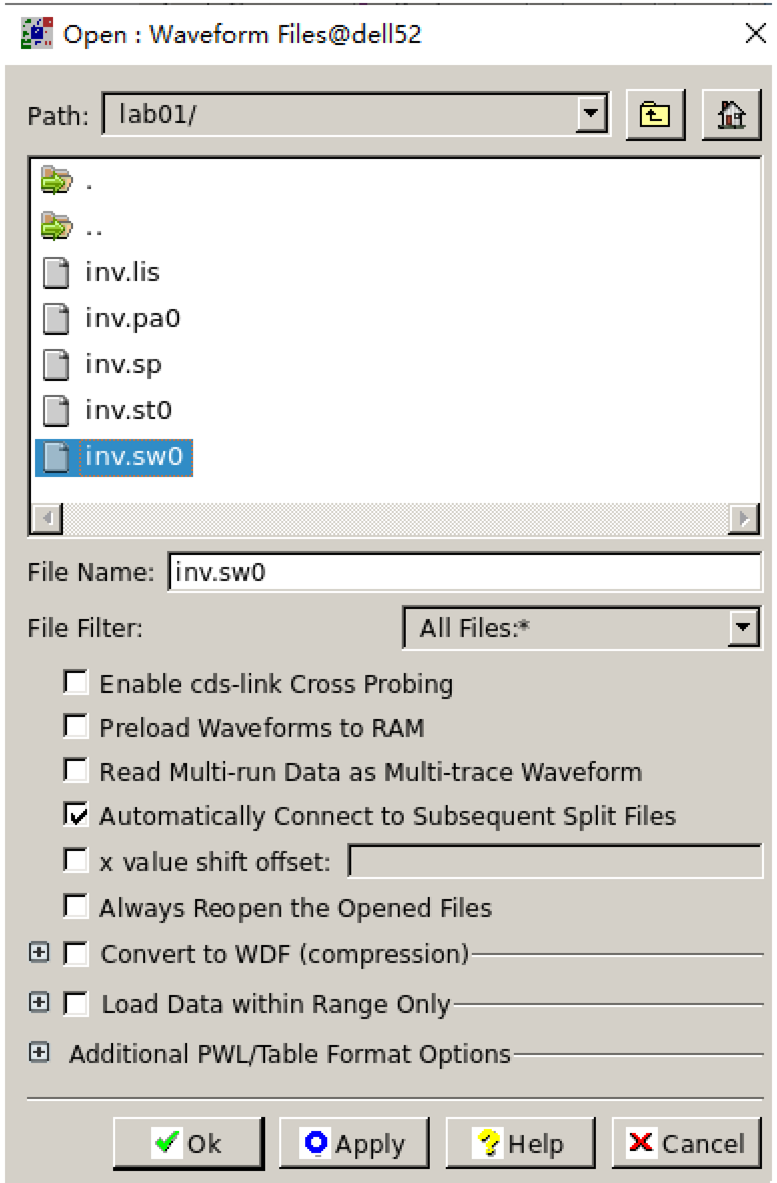
Drag-n-Drop signals from the Output View browser to add waveforms

done loading waveform data

WaveView (continue)

- Import desired graph file
- Here we open the inv.sw0




Open : Waveform Files@dell52

Path: lab01/

.
..
inv.lis
inv.pa0
inv.sp
inv.st0
inv.sw0

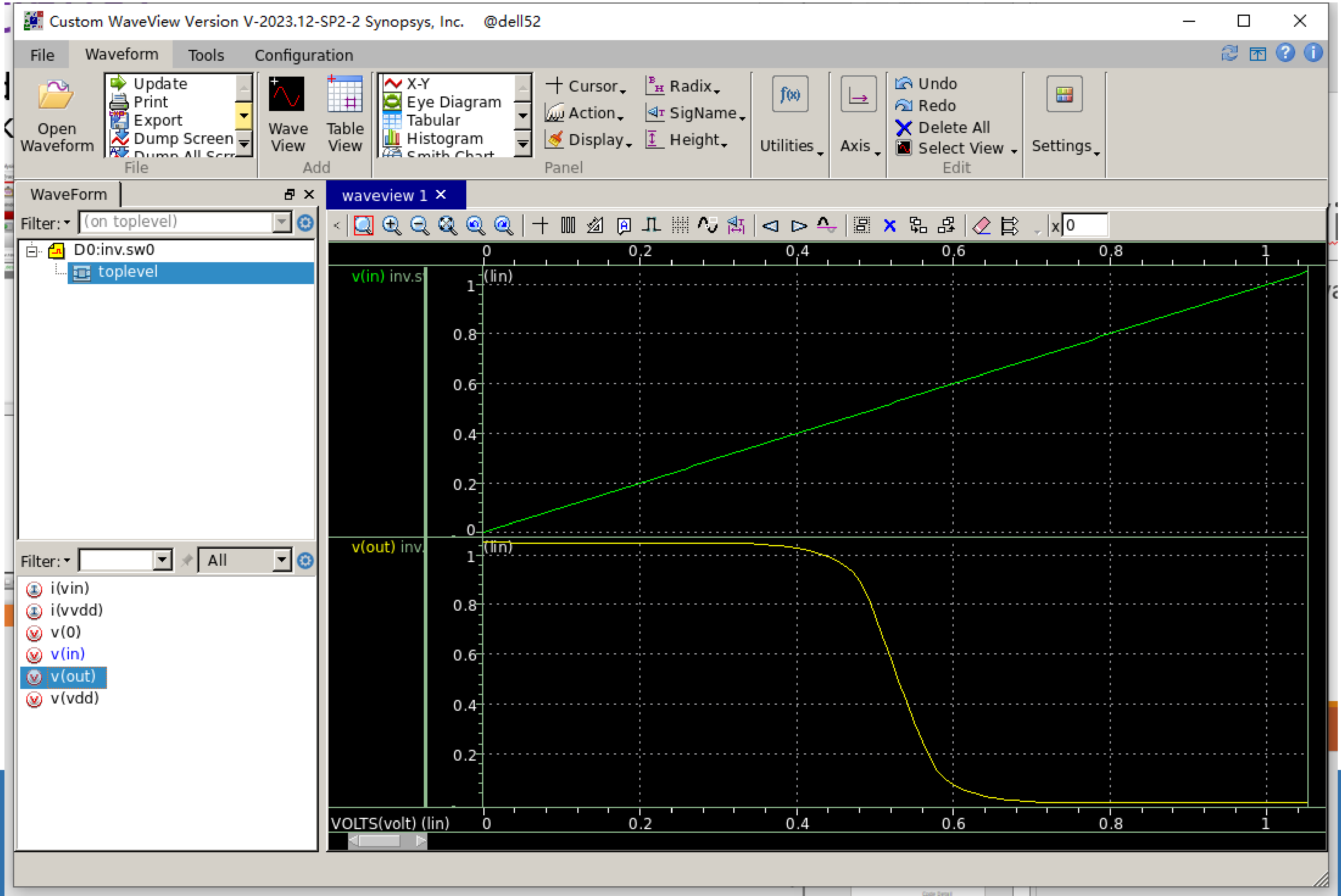
File Name: inv.sw0

File Filter: All Files:*

- □ Enable cds-link Cross Probing
- □ Preload Waveforms to RAM
- □ Read Multi-run Data as Multi-trace Waveform
- ☑ Automatically Connect to Subsequent Split Files
- □ x value shift offset:
- □ Always Reopen the Opened Files
- ⊞ □ Convert to WDF (compression)
- ⊞ □ Load Data within Range Only
- ⊞ Additional PWL/Table Format Options

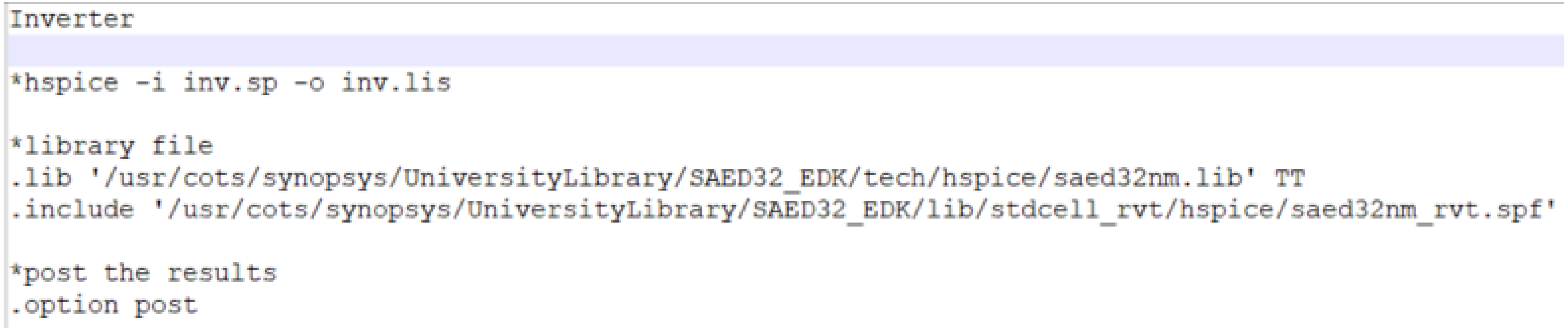
WaveView (continue)

- Display the waves by dragging the signals into the waveform box or just double click



Code Detail (inv.sp)

- NOT Case sensitive
- First line is automatically a comment, **DON’T put your code in the first line!**
- Lines starting with ‘*’ is a comment
- saed32nm.lib: Synopsys 32nm Educational library
- TT: Typical NMOS Typical PMOS(FF, SS, FS…)
- RVT: regular voltage threshold(HVT, LVT)



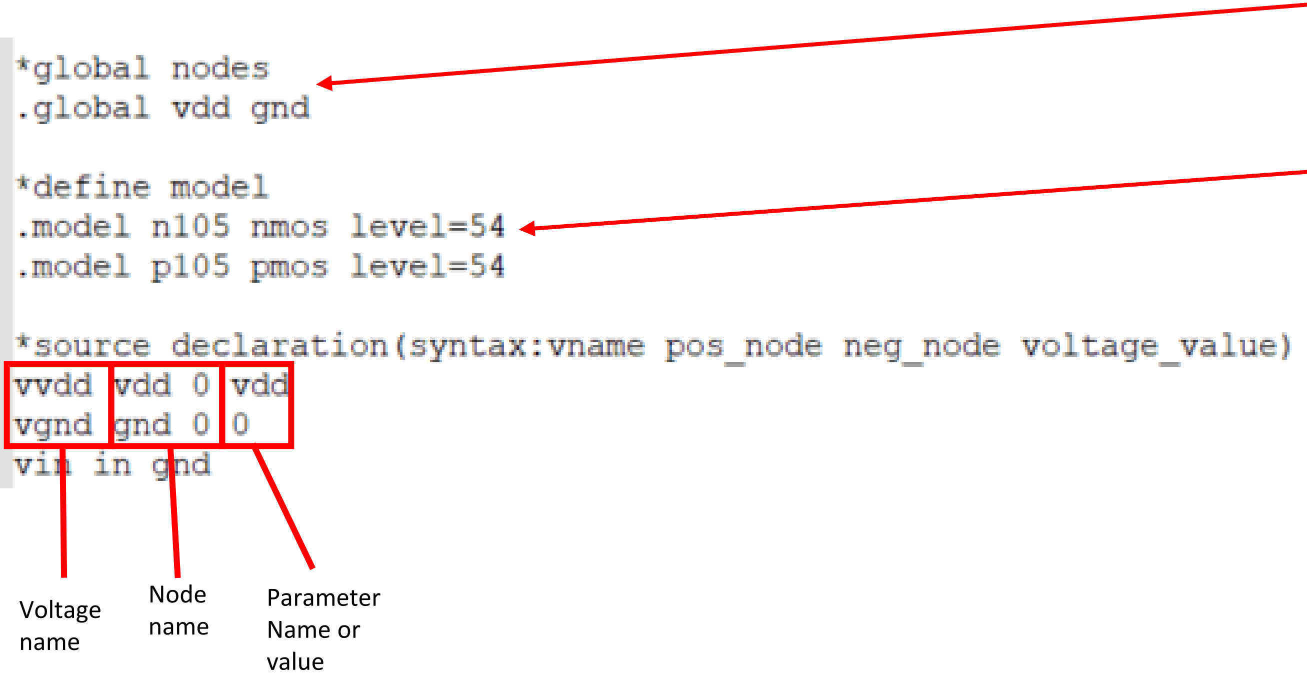
```
Inverter

*hspice -i inv.sp -o inv.lis

*library file
.lib '/usr/cots/synopsys/UniversityLibrary/SAED32_EDK/tech/hspice/saed32nm.lib' TT
.include '/usr/cots/synopsys/UniversityLibrary/SAED32_EDK/lib/stdcell_rvt/hspice/saed32nm_rvt.spf'

*post the results
.option post
```

Code Detail (inv.sp)



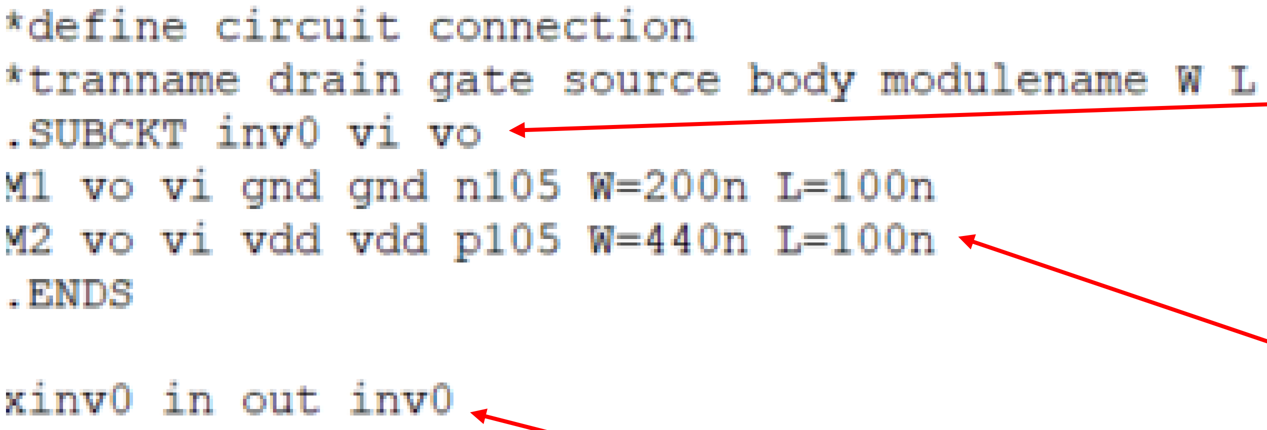
```
*global nodes
.global vdd gnd

*define model
.model n105 nmos level=54
.model p105 pmos level=54

*source declaration(syntax:vname pos_node neg_node voltage_value)
vvdd vdd 0 vdd
vgnd gnd 0 0
vin in gnd
```

- Global nodes that available for all sub-circuits
- Define the wanted model from the library
  .model name type level
  (level indicates the module complexity)
- Declare source:
  A voltage source called ‘**vvdd**’, connected between nodes ‘**vdd**’ and ‘0-voltage node’, with the value according to parameter ‘**vdd**’
  ’Vxxx’ for voltage source name, ’Ixxx’ for current source name

Code Detail (inv.sp)

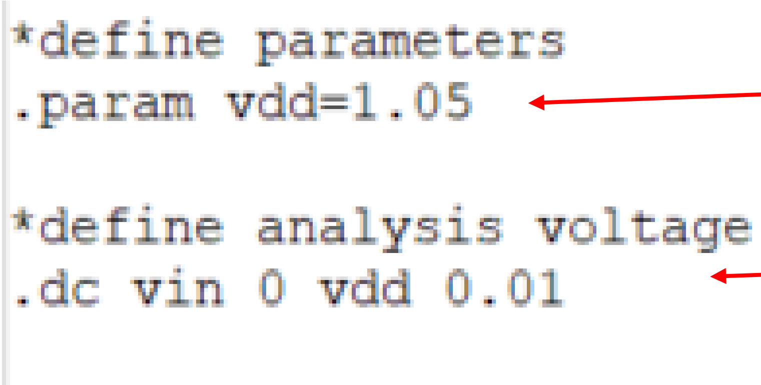


```
*define circuit connection
*tranname drain gate source body modulename W L
.SUBCKT inv0 vi vo
M1 vo vi gnd gnd n105 W=200n L=100n
M2 vo vi vdd vdd p105 W=440n L=100n
.ENDS

xinv0 in out inv0
```

- Start design a sub-circuit, which named ‘inv0’, it has two ports: ‘vi’ and ‘vo’
- Add transistors to the sub-circuit. Transistor name starts with ’M’.
- Instantiation of the sub-circuit, pay attention to the order of all ports.

Code Detail (inv.sp)



```
*define parameters
.param vdd=1.05

*define analysis voltage
.dc vin 0 vdd 0.01
```

- Define all the parameters
- Run a DC test on source ‘vin’, scan it from 0 to vdd with the step length of 0.01

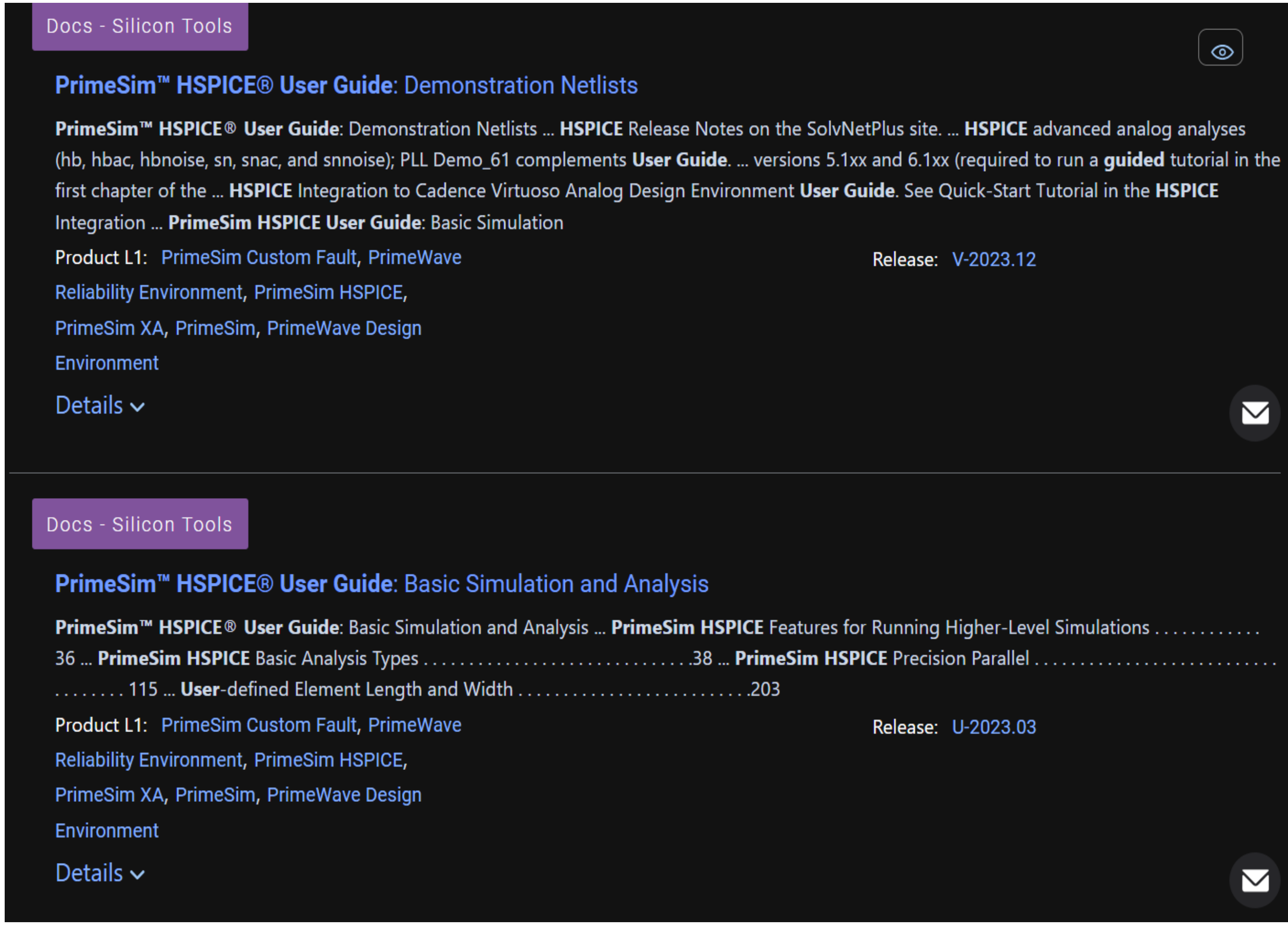
Resource Page Updates

Hspice user guides:

- **Create a SolvNetPlus account**

https://solvnetplus.synopsys.com/s/

- **Search “Hspice user guide”, you will get very detailed documents about Hspice.**



Docs - Silicon Tools

PrimeSim™ HSPICE® User Guide: Demonstration Netlists

PrimeSim™ HSPICE® User Guide: Demonstration Netlists ... **HSPICE** Release Notes on the SolvNetPlus site. ... **HSPICE** advanced analog analyses (hb, hbac, hbnoise, sn, snac, and snnoise); PLL Demo_61 complements **User Guide**. ... versions 5.1xx and 6.1xx (required to run a **guided** tutorial in the first chapter of the ... **HSPICE** Integration to Cadence Virtuoso Analog Design Environment **User Guide**. See Quick-Start Tutorial in the **HSPICE** Integration ... **PrimeSim HSPICE User Guide**: Basic Simulation

Product L1: PrimeSim Custom Fault, PrimeWave Reliability Environment, PrimeSim HSPICE, PrimeSim XA, PrimeSim, PrimeWave Design Environment

Release: V-2023.12

Details

Docs - Silicon Tools

PrimeSim™ HSPICE® User Guide: Basic Simulation and Analysis

PrimeSim™ HSPICE® User Guide: Basic Simulation and Analysis ... **PrimeSim HSPICE** Features for Running Higher-Level Simulations . . . . 36 ... **PrimeSim HSPICE** Basic Analysis Types . . . . .38 ... **PrimeSim HSPICE** Precision Parallel . . . . 115 ... **User**-defined Element Length and Width 203

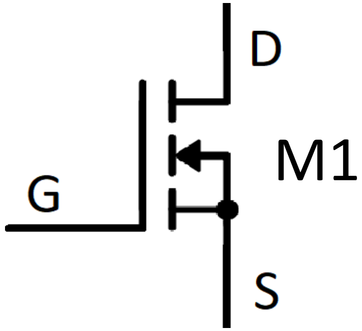
Product L1: PrimeSim Custom Fault, PrimeWave Reliability Environment, PrimeSim HSPICE, PrimeSim XA, PrimeSim, PrimeWave Design Environment

Release: U-2023.03

Details

Hspice Simulation (DC Analysis)

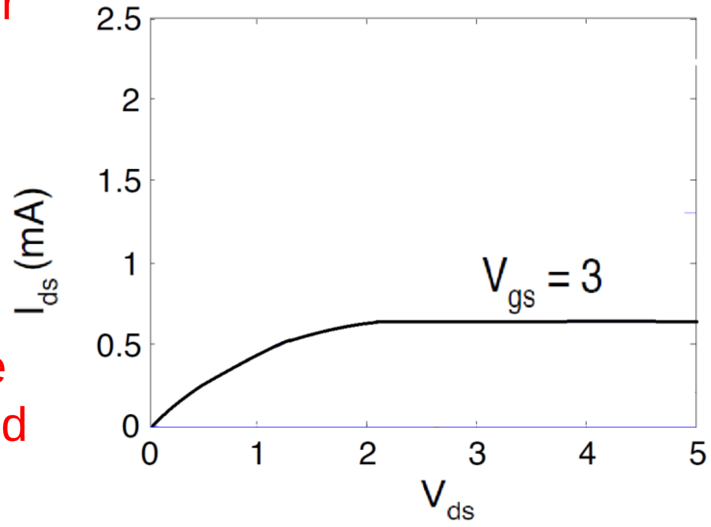
- DC Analysis (Figure out how circuits behave when some variable values change)
- Syntax 1: .DC var1 start1 stop1 step1
- Example: plot nMOS I-V curve



```
*define analysis voltages
vds d gnd 5
vgs g gnd 3
*start dc analysis(sweep vds)
.dc vds 0 5 0.05
*probe Ids (gate current)
.probe DC i(M1)
```

Always leave a default value for all sources!

Will overwrite the previously defined vds value

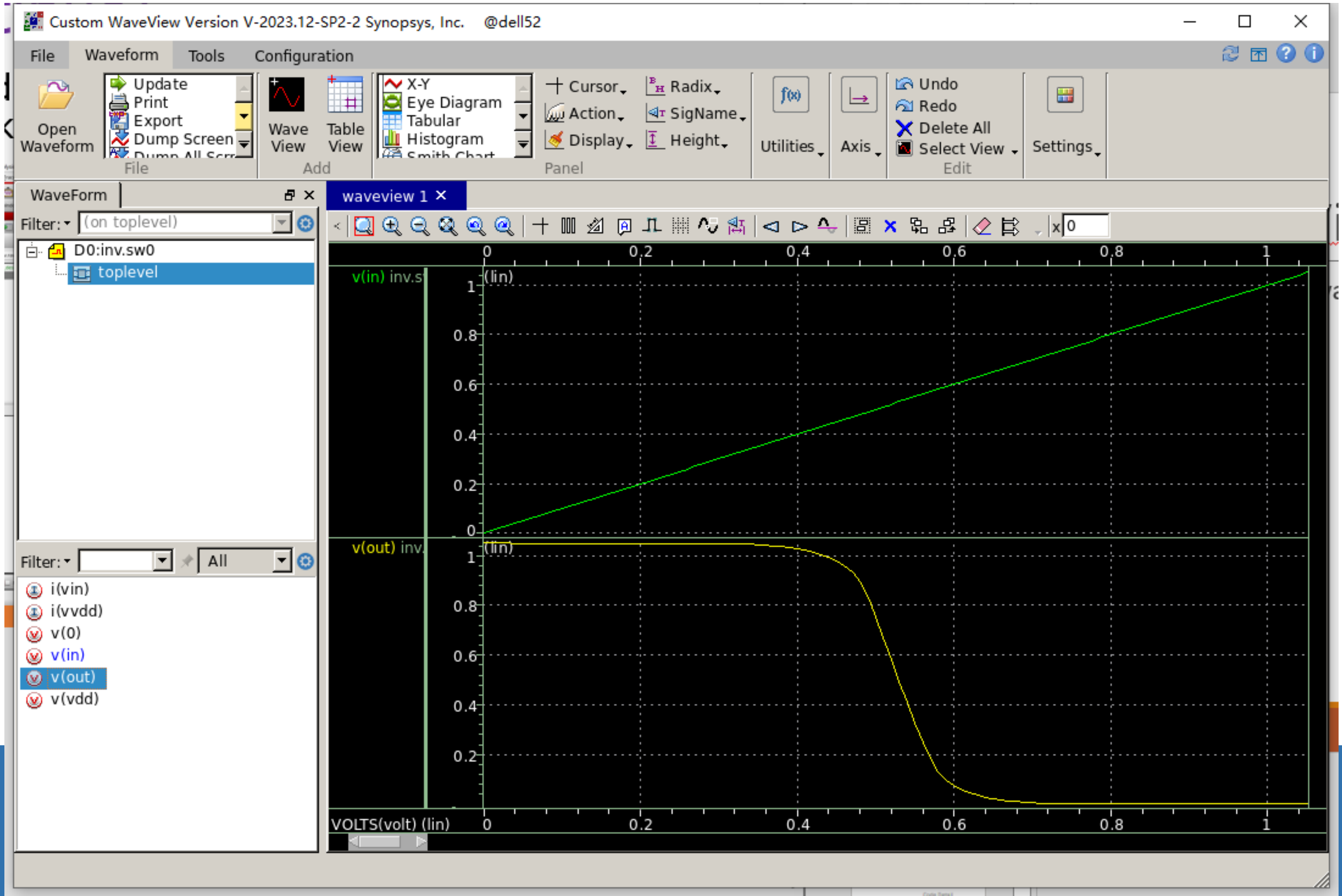


Hspice Simulation (DC Analysis)

- .dc indicate your X-axis

```
        .dc vin 0 1.05 0.01
```

In the .sw file generated with this .dc, all waveforms will share the same X-axis, which is vin from 0 to 1.05.



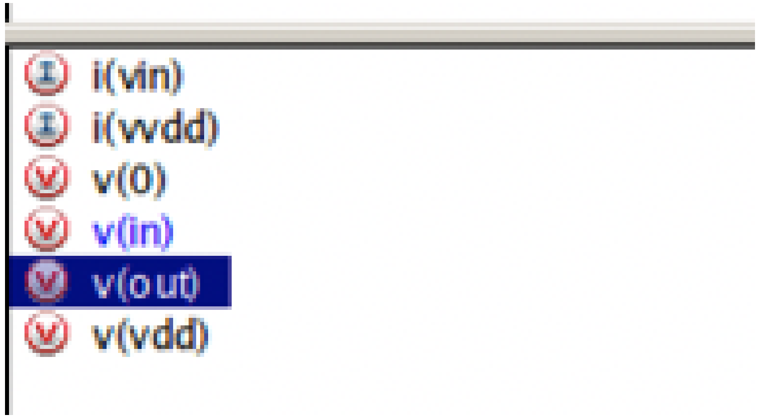
Hspice Simulation (DC Analysis)

Command	Explanation
.dc vds 0 1.05 0.01	Scan vds from 0 to 1.05, with step length of 0.01
.dc temp -55 125 5	Scan temperature form -55 to 125 with step of 5
M1 d g gnd! B n105 W=300n L=l_n .dc l_n 20n 100n 1n	Scan the transistor length from 20n to 100n with step of 1n

Hspice Simulation (DC Analysis)

- Variables for Y-axis can be defined by 2 ways:

  Hspice will generate some variables by default:

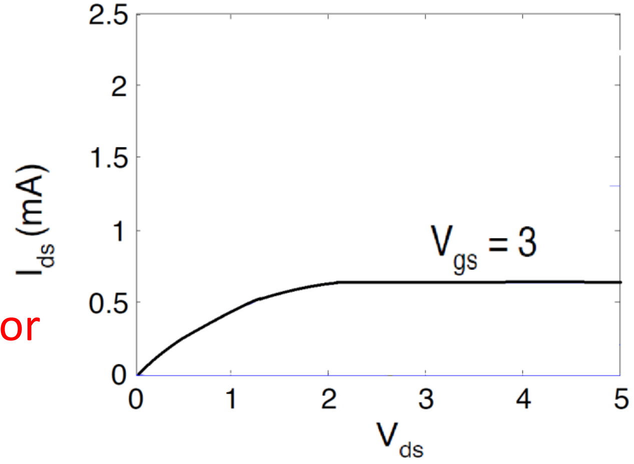


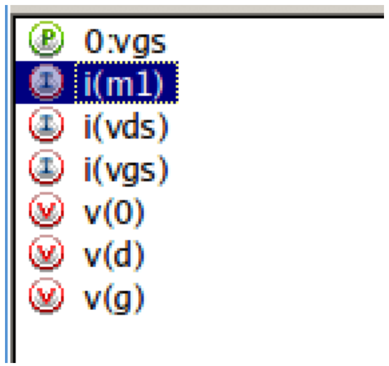
  Define what you want with .probe:

```
*define analysis voltages
     vds d gnd 5
     vgs g gnd 3
     *start dc analysis(sweep
vds)
     .dc vds 0 5 0.05
     *probe Ids (gate current)
     .probe DC i(M1)
```

Add a probe testing the current flow through transistor M1 (Ids)

.probe will work for all analysis





Hspice Simulation (DC Analysis)

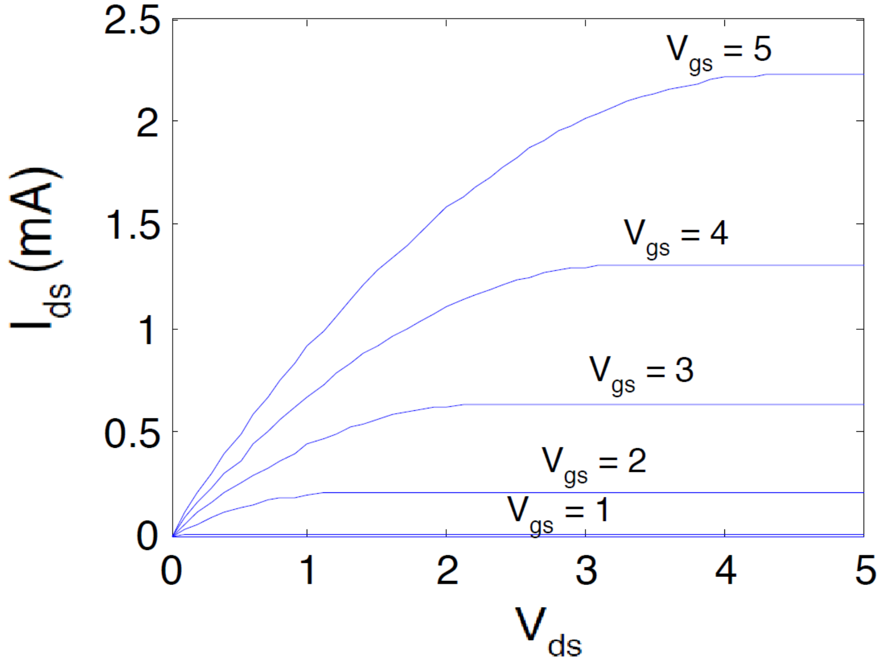
Command	Explanation
.probe dc i(M1)	Probe on the Ids of M1
.probe lv9(M1)	Probe on the Vth of M1

Hspice Simulation (DC Analysis)

- DC Analysis ()
- Syntax 2: .DC var1 start1 stop1 step1 sweep var2 start2 stop2 step2
- Example:

```
*define vds
vds d gnd 5
vgs g gnd 5
*start dc analysis(sweep vds)
.dc vds 0 5 0.05 sweep vgs 0 5 1
*probe Ids (gate current)
.probe DC i(M1)
```

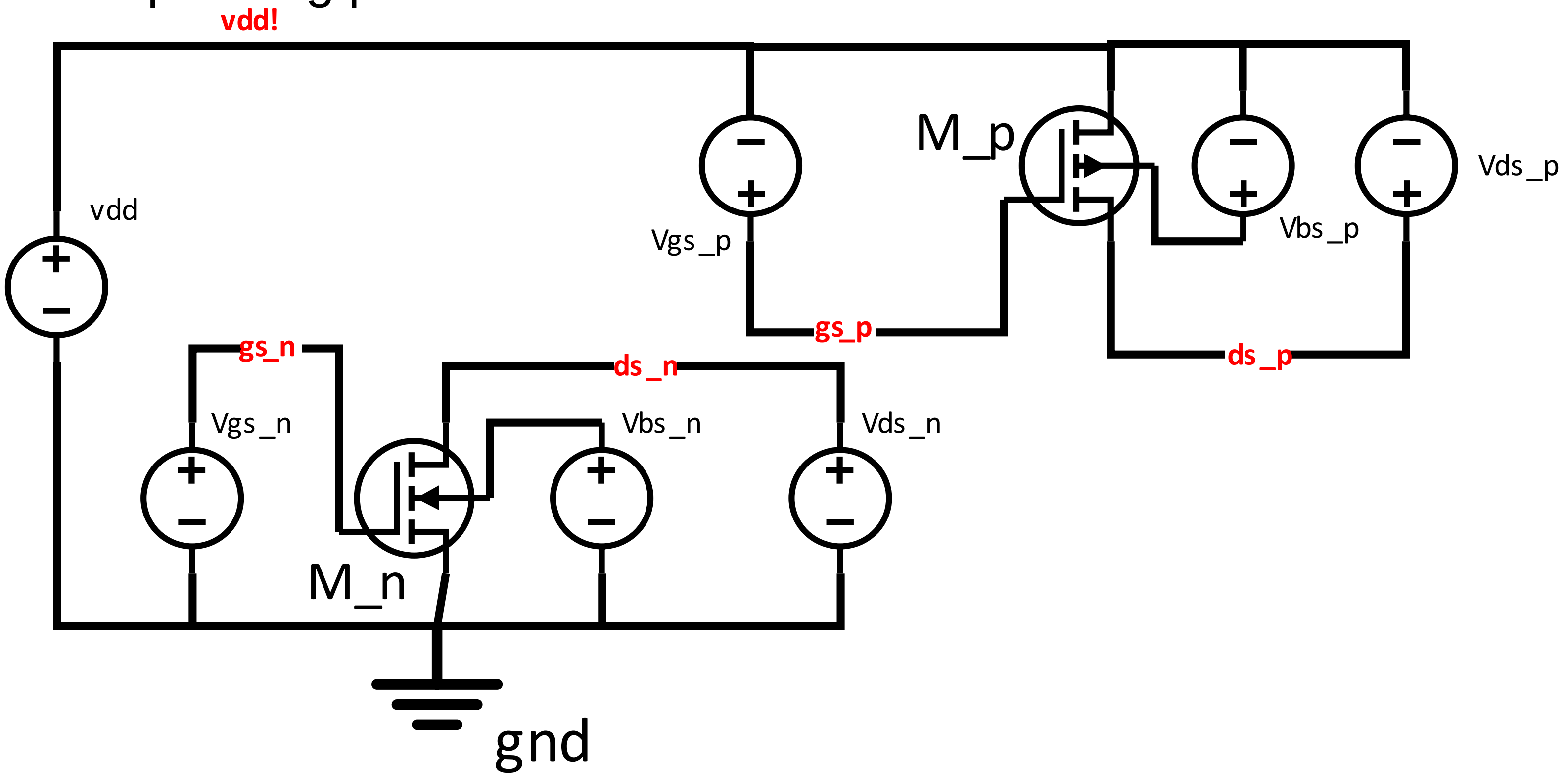
Run dc analysis multiple times with different vgs



Lab01 Submission

- Lab 1 report & Hspice file.
  - Try to include everything in one .sp file.
  - Parameterize as much as possible.
  - Include the equation of the correspor ng parameters

- Connection reference:



Thank you!