EE103 Intro to VLSI Design

Lab 4 Study of Characteristics of CMOS Inverters

Objective:

- Lab 4 is mainly about using HSPICE simulation tool to explore the inverter characteristics and buffer design.
- The **DUE DATE** for this Lab report is **POSTED ON CANVAS**.

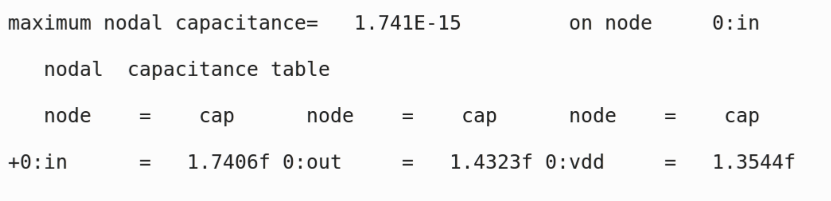
Laboratory Tasks:

- Learn the characteristics of CMOS inverter design.

Assignment:

(Use '6p' as rise and fall time for all your Vpulse)

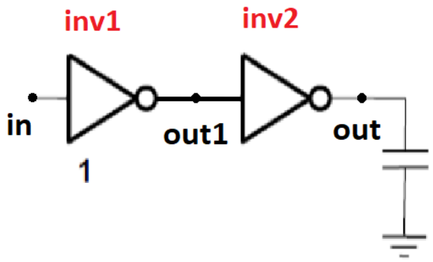
1. Buffer Design:
   In this part you will experiment in designing a buffer. You can either read text books or read the *VLSI-CMOS Inverter.pdf* for more information. Lastly, you are required to generate a table similar to the one in p.40.
   Experiment Steps:
   a. Build an inverter as the first stage of your inverter chain (NMOS: 300n/100n; PMOS: 600n/100n). Measure the **input Capacitance** at the **first stage**. HSPICE command '*.option CAPTAB=1'* can measure all the node capacitances. You need to find the measured input capacitances in the '.lis' file (search for "capacitance").



```
maximum nodal capacitance=   1.741E-15         on node     0:in

   nodal  capacitance table

   node     =    cap       node     =    cap       node     =    cap

+0:in       =    1.7406f 0:out      =    1.4323f 0:vdd      =    1.3544f
```

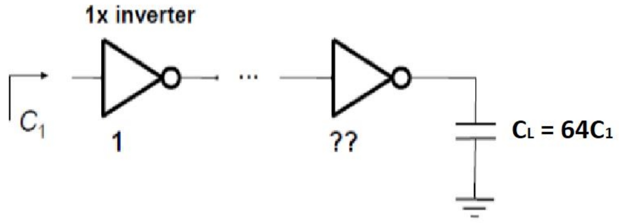
Since for each inverter chain you will have multiple different CMOS, therefore it is suggested to write sub-circuits in the HSPICE file. An example (N = 2) is given below:

```
.subckt inv1 in out
M1 out in vdd! vdd! p105 W=600n L=100n
M2 …
.ends

.subckt inv2 in out
M1 …
M2 …
.ends

XINV1 in out1 inv1
XINV2 out1 out inv2
```



b. Connect a load capacitance at the end of the output of the inverter chain. Make the capacitance value **64** times larger than the value you just measured in step a.

Code: cload out gnd 150f
(CapName) (Nodes) (Value)



c. Use the schematic in p.41 as a reference and construct four inverter chains for N (number of stages) from 1 to 4. For the rest stages, you need to set the CMOS parameters for inverters (except the first one) based on the total number of stages and the design rule learnt in class.

d. Measure the **Delay (Tp)** for each inverter chain (final output) and here you still need to measure both **tpHL** and **tpLH** in order to get the delay **Tp.** Draw a table similar to the one in p.40 in the *VLSI-CMOS Inverter.pdf.*

2. Construct a CMOS inverter. Make the width (300n) and length (100n) fixed for NMOS, and length (100n) fixed for PMOS. Using the HSPICE Optimization tool, find the width of the PMOS for each of the following requirements:
   a. Make $tpLH - tpHL$ as close to zero as possible
   b. Have the smallest average propagation delay (hint: make $(tpLH + tpHL)/2$ as close to zero as possible)

3. Use the same CMOS inverter setting in Problem 2. Use the HSPICE Optimization tool to find the width of the PMOS for the following requirement:
   a. Switching threshold (Vm) equals to half of Vdd. (Balanced Inverter)

You will need to use a new measure command. An example is given below:

```
.Dc vc 0 1.2 0.02 sweep optimize=optrange2 Results=wid Model=opt1

.measure DC wid FIND V(2) WHEN V(1)='0.1*Vdd'

*Then you can run optimization on this measurement

*.MEASURE <DC|TRAN|AC> result FIND out_var1 WHEN out_var2 = out_var3
*+ <TD = val > < RISE = r | LAST > < FALL = f | LAST >
*+ <CROSS = c | LAST> <GOAL = val> <MINVAL = val> <WEIGHT = val>

*this command find the voltage value at node ‘2’ when the voltage value at node ‘1’
equals *0.1*Vdd
```

Submission Requirements

- For part 1:
  Take a screenshot of the input capacitance measurement.
  For each inverter chain: take a screenshot of the tpLH and tpHL. Write down the NMOS and PMOS width and length for each state.
  Construct the table similar to the one in P.40 in VLSI-CMOS Inverter.pdf.

- For part 2:
  For both cases, take screenshots of the .lis file that contains optimized width and optimized goal value

- For part 3:
  Take a screenshot of the .lis file that contains optimized width and optimized goal value

Reference HSPICE code for 1-3

```
*this is an inverter spice file for optimization


.lib '/usr/commercial_amd64/synopsys/libraries/SAED32_EDK/tech/hspice/saed32nm.lib' TT

.include
'/usr/commercial_amd64/synopsys/libraries/SAED32_EDK/lib/stdcell_rvt/hspice/saed32nm_rvt.spf'


*post the results

.option post

.global vdd gnd



*define model

.model n105 nmos level=54

.model p105 pmos level=54


*source declaration

vvdd vdd 0 vdd   *syntax:vname pos_node neg_node voltage_value

vgnd gnd 0 0v
```

```
.param vdd = 1.05
.param l = 100n

M1 vo vi gnd gnd n105 W=300n L=l
M2 vo vi vdd vdd p105 W=wp L=l

.param trf = 4p
.param del = 2u
.param per = 10u
.param pw = 5u

*define analysis voltage
vinput vi gnd pulse 0 vdd del trf trf pw per

.model opt1 opt
.param wp = OPTrange(400n, 200n, 1000n)

*.dc vinput 0 1.05 0.01 sweep optimize=optrange Results=wid Model=opt1
*.measure DC wid FIND V(vi) WHEN V(vo)='0.5*vdd' goal='vdd/2'

*.tran 1p 30u

.measure tran tphl trig v(vi) val='vdd*0.5' rise=2 targ v(vo) val='vdd*0.5' fall=2
.measure tran tplh trig v(vi) val='vdd*0.5' fall=2 targ v(vo) val='vdd*0.5' rise=2
.measure tran tpd param='tphl-tplh' goal=0

.tran 1p '3*per' sweep optimize=OPTrange RESULTS=tpd MODEL=OPT1

.end
```