

A.

ReadMe:

```
1 cycle time: 13
2 FPU Single: Y
3 FPU Double: Y
```

RTL:

Baseline:

```
Verdi> FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the pr
*Verdi> : Create FSDB file 'MIPS.fsd'
*Verdi> : Begin traversing the scope (SingleCycle_tb), layer (0).
*Verdi> : Enable +mda dumping.
*Verdi> : End of traversing.
*Verdi> : Begin traversing the scopes, layer (0).
*Verdi> : End of traversing.
=====The test result is ..... PASS=====

*****
**                                     **
**      Congratulations !!           **
**                                     **
** All instructions have been done successfully! **
**                                     **
*****


Simulation complete via $finish(1) at time 7701 NS + 0
/fbv.v:158                               $finish;
ncsim> exit
[hg6177@cad11 ~]$ hwa_r41s
```

Single:

```
Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may
Verdi* : Create FSDB file 'MIPS.fsdb'
Verdi* : Begin traversing the scope (SingleCycle_tb), layer (0).
Verdi* : Enable +mda dumping.
Verdi* : End of traversing.
Verdi* : Begin traversing the scopes, layer (0).
Verdi* : End of traversing.
=====The test result is .... PASS=====

                                FPU Version

*****
**                               **
**      Congratulations !!      **
**                               **
**      All instructions have been done successfully! **
**                               **
*****


                                     
```

Double:

```
Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
Verdi*: Create FSDB file 'MIPS.fsdb'
Verdi*: Begin traversing the scope (SingleCycle_tb), layer (0).
Verdi*: Enable +mnda dumping.
Verdi*: End of traversing.
Verdi*: Begin traversing the scopes, layer (0).
Verdi*: End of traversing.
=====The test result is ..... PASS=====
```

FPU Version

```
** **** **
**      Congratulations !!          **
**                                  **
** All instructions have been done successfully! **
** **** **
*****
```



Gatelevel:

Baseline:

```

*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
*Verdi* : Create FSDB file 'MIPS.fsdb'
*Verdi* : Begin traversing the scope (SingleCycle_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
using SDF File ./SingleCycleMIPS_syn.sdf for this simulation.
=====The test result is ..... PASS=====

*****
**                                     **
**          Congratulations !!          **
**                                     **
** All instructions have been done successfully! **
**                                     **
*****

```

Single:合成失敗

Double:合成失敗

Timing report:

Baseline:

```

U1243/Y (AND2X8)
0.14      9.72 r
U2302/Y (OAI2BB2X4)
0.10      9.82 f
U1364/Y (BUFX20)
0.21      10.03 f
register_reg_0_31_/D (EDFFTRXL)
0.00      10.03 f
data arrival time
10.03

clock clk (rise edge)
10.00      10.00
clock network delay (ideal)
0.50      10.50
clock uncertainty
-0.10      10.40
register_reg_0_31_/CK (EDFFTRXL)
0.00      10.40 r
library setup time
-0.37      10.03
data required time
10.03

-----
data required time
10.03
data arrival time
-10.03
-----

slack (MET)
0.00

```

Area report:

Baseline:

```

*****
Report : area
Design : SingleCycleMIPS
Version: N-2017.09-SP2
Date   : Tue Dec 31 04:28:48 2019
*****

Library(s) Used:

slow (File: /home/raid7_2/course/cvsd
/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:      490
Number of nets:      4596
Number of cells:      4094
Number of combinational cells: 3026
Number of sequential cells: 1064
Number of macros/black boxes: 0
Number of buf/inv:    606
Number of references: 156

Combinational area:    35847.390919
Buf/Inv area:          4616.927996
Noncombinational area: 39155.623335
Macro/Black Box area:  0.000000
Net Interconnect area: 635556.557312

Total cell area:       75003.014254
Total area:            710559.571566

Hierarchical area distribution
-----
Local cell area      Global cell area
-----

```

B.

$A * T = 975039.2$

C.

照著圖接線,自己加一些 control signal,最大的問題是一開始不知道 memory 怎麼運作,還有 double 的執行,FPU 合成失敗

D.

組員停修, 自己一組

E.

沒有特別去管  $A * T$  值,寫出來就好