

電機三 b06901177 劉凡

1. Rtl_tb1

```

./(((((((((((. /...*/.*** /(\
.(((.....*.##* *.*\(((
(((/ *.*.*.*.*/((#*
(((((((...*/.***.,(((((((..
.,(((((((((((##(((((((*)
*((((((./.*
.. .. * .. ..
.....
=====
Your answer : 0000000000000110000110000100100011000001111000100100001010100011000000110110001111000100001001001000010011
10010101000101101
Correct answer: 000000000000000110000110000100100011000001111000100100001010100011000000110110001111000100001001001000010011
10010101000101101
Simulation complete via $finish(1) at time 195 NS + 0
./testfixture.v:185 $finish;
ncsim> exit

```

2. Rtl_tb2

```
(((((...*/^***..(((((...  
(((((###((((((*)  
*,*(((((/*+  
.  
..*  
. . .  
.....  
=====
```

Your answer : 1000111111101001011000110100011010010110100110100110001111101110000110101101010100010110011101010
0011010101101011
Correct answer: 1000111111101001011000110100011010010110100110100110001111101110000110101101010100010110011101010
0011010101101011
Simulation complete via Sfinish(1) at time 195 NS + 0
./testfixture.v:185 \$finish;
ncsim> exit

3. Gatelevel tb1

```
-----
START!!! Simulation Start .....
-----
SDF File ./matvecmult_syn.sdf were used for this simulation.
=====
Congratulations!!! Your answer is correct!
```

4. Gatelevle_tb2

```
START!!! Simulation Start .....
```

```
SDF File ./matvecmult_syn.sdf were used for this simulation.  
=====
```

Congratulations!!! Your answer is correct!

5. No latch

```

Inferred memory devices in process
in routine matvecmult line 123 in file
'home/raid7_2/userb06/b06177/HW3/matvecmult.v'.

```

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
vector_v_r_reg	Flip-flop	128	Y	N	Y	N	N	N	N
counter_r_r_reg	Flip-flop	4	Y	N	Y	N	N	N	N
finish_r_r_reg	Flip-flop	1	N	N	Y	N	N	N	N

```

Statistics for MUX_Ops

```

block name/line	Inputs	Outputs	# sel inputs
matvecmult/107	16	16	4

```

Presto compilation completed successfully.
Current design is now 'home/raid7_2/userb06/b06177/HW3/matvecmult.db:matvecmult'
Loaded 1 design.
Current design is 'matvecmult'.
Current design is 'matvecmult'.

```

```

Linking design 'matvecmult'
Using the following designs and libraries:
-----
matvecmult                /home/raid7_2/userb06/b06177/HW3/matvecmult.db
slow (library)            /home/raid7_2/course/cvsd/CBDK_IC Contest/CIC/SynopsysDC/db/slow.db
typical (library)         /home/raid7_2/course/cvsd/CBDK_IC Contest/CIC/SynopsysDC/db/typical.db
fast (library)            /home/raid7_2/course/cvsd/CBDK_IC Contest/CIC/SynopsysDC/db/fast.db
dw_foundation.sldb (library) /usr/cad/synopsys/synthesis/cur/libraries/syn/dw_foundation.sldb

```

6. Timing report

```
add_1_root_add_0_root_add_84_15/B_5_ (matvecmult_DW01_add_1) 0.00 6.25 r
add_1_root_add_0_root_add_84_15/U9/Y (XOR3X1) 0.95 7.20 r
add_1_root_add_0_root_add_84_15/SUM_5_ (matvecmult_DW01_add_1) 0.00 7.20 r
add_0_root_add_0_root_add_84_15/B_5_ (matvecmult_DW01_add_0) 0.00 7.20 r
add_0_root_add_0_root_add_84_15/U2/Y (XOR3X1) 0.76 7.95 r
add_0_root_add_0_root_add_84_15/SUM_5_ (matvecmult_DW01_add_0) 0.00 7.95 r
add_0_root_add_0_root_add_107_2/B_5_ (matvecmult_DW01_add_17) 0.00 7.95 r
add_0_root_add_0_root_add_107_2/U1_5/C0 (ADDFXL) 0.87 8.83 r
add_0_root_add_0_root_add_107_2/U1_6/C0 (ADDFX2) 0.35 9.17 r
add_0_root_add_0_root_add_107_2/U1_7/Y (XOR3X2) 0.30 9.47 r
add_0_root_add_0_root_add_107_2/SUM_7_ (matvecmult_DW01_add_17) 0.00 9.47 r
U176/Y (INVX4) 0.25 9.72 f
U297/Y (OA12BB2XL) 0.46 10.18 r
vector_y_r_reg_7_7/D (DFFRX2) 0.00 10.18 r
data arrival time 10.18

clock CLK (rise edge) 10.00 10.00
clock network delay (ideal) 0.50 10.50
clock uncertainty -0.10 10.40
vector_y_r_reg_7_7/CK (DFFRX2) 0.00 10.40 r
library setup time -0.22 10.18
data required time 10.18
-----
data required time 10.18
data arrival time -10.18
-----
slack (MET) 0.00
```

7. Area report

```
ic_shell> report_area
*****
report : area
design : matvecmult
version: N-2017.09-SP2
date : Mon Dec 2 17:33:40 2019
*****

library(s) Used:

slow (File: /home/raid7_2/course/cvstd/CBDK_IC_Constest/CIC/SynopsysDC/db/slow.db)

Number of ports: 1262
Number of nets: 3152
Number of cells: 1789
Number of combinational cells: 1584
Number of sequential cells: 170
Number of macros/black boxes: 0
Number of buf/inv: 225
Number of references: 57

Combinational area: 19750.946633
Buf/Inv area: 933.569987
Noncombinational area: 4920.762608
Macro/Black Box area: 0.000000
Net Interconnect area: 203934.356842

total cell area: 24671.709240
total area: 228606.066082
```

8. 參考 sample 的檔案寫出來的,在研究 sequential circuit 怎麼運作時花了很多時間,由於我是第一次寫 verilog,目前對於怎麼讀出檔案還不太會,寫完作業四應該可以更加熟悉