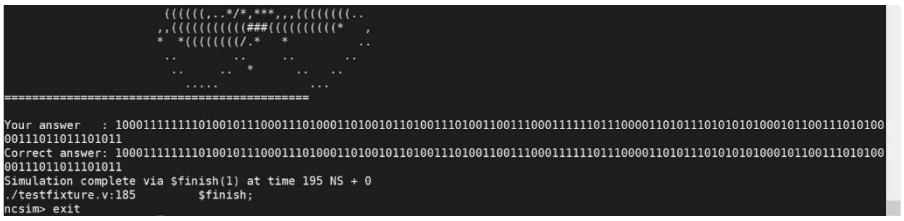
Report

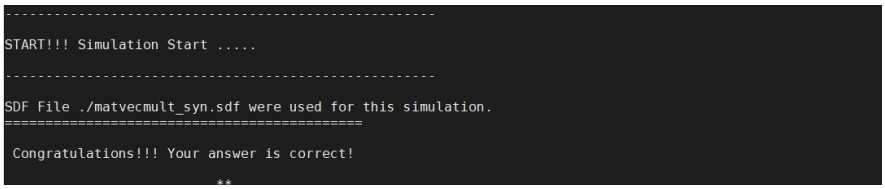
電機三 b06901177 劉凡

1. Rtl_tb1

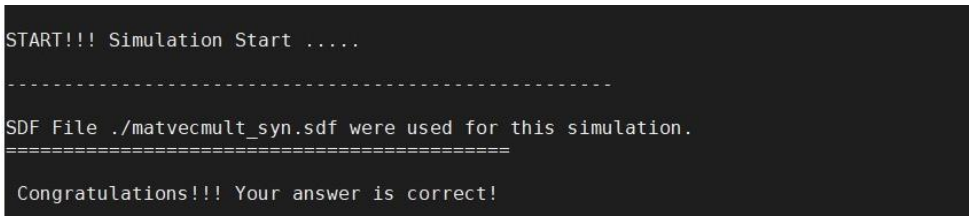
2. Rtl_tb2



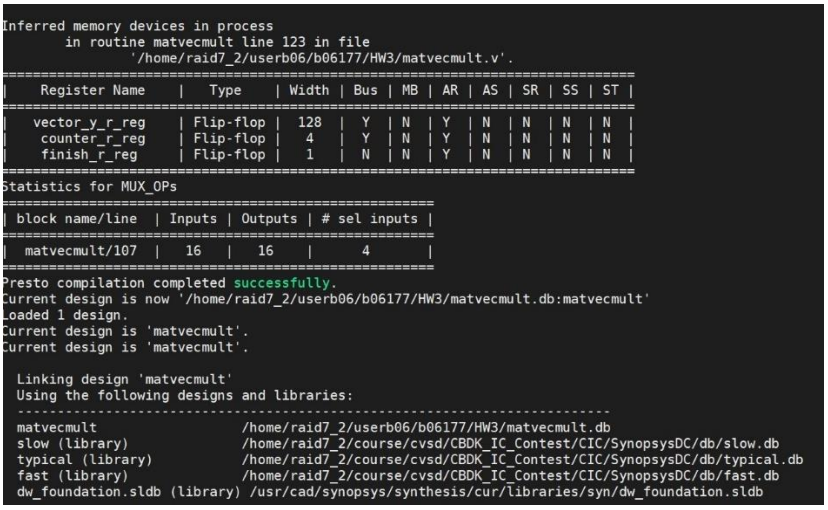
3. Gatelevel_tb1



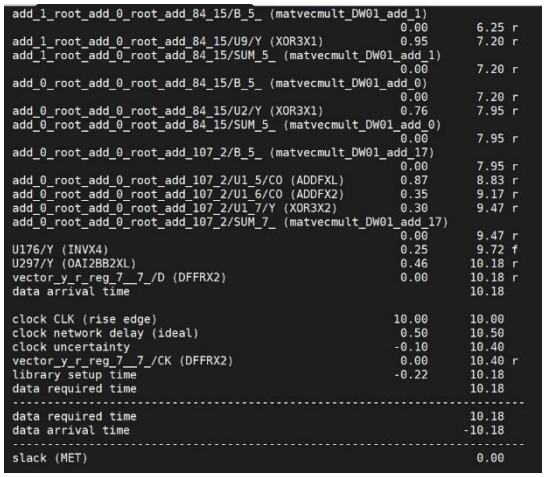
4. Gatelevle_tb2



5. No latch



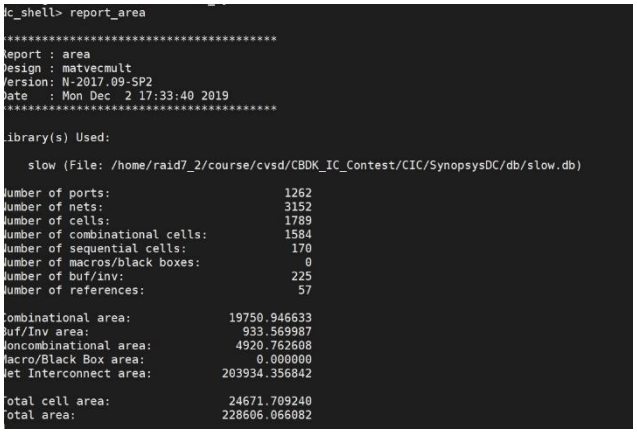
6. Timing report



```
 add_1_root_add_0_root_add_84_15/B_5_ (matvecmult_DW01_add_1)
                                                    0.00       6.25 r
 add_1_root_add_0_root_add_84_15/U9/Y (XOR3X1)      0.95       7.20 r
 add_1_root_add_0_root_add_84_15/SUM_5_ (matvecmult_DW01_add_1)
                                                    0.00       7.20 r
 add_0_root_add_0_root_add_84_15/B_5_ (matvecmult_DW01_add_0)
                                                    0.00       7.20 r
 add_0_root_add_0_root_add_84_15/U2/Y (XOR3X1)      0.76       7.95 r
 add_0_root_add_0_root_add_84_15/SUM_5_ (matvecmult_DW01_add_0)
                                                    0.00       7.95 r
 add_0_root_add_0_root_add_107_2/B_5_ (matvecmult_DW01_add_17)
                                                    0.00       7.95 r
 add_0_root_add_0_root_add_107_2/U1_5/CO (ADDFXL)   0.87       8.83 r
 add_0_root_add_0_root_add_107_2/U1_6/CO (ADDFX2)   0.35       9.17 r
 add_0_root_add_0_root_add_107_2/U1_7/Y (XOR3X2)    0.30       9.47 r
 add_0_root_add_0_root_add_107_2/SUM_7_ (matvecmult_DW01_add_17)
                                                    0.00       9.47 r
 U176/Y (INVX4)                                     0.25       9.72 f
 U297/Y (OAI2BB2XL)                                 0.46      10.18 r
 vector_y_r_reg_7__7_/D (DFFRX2)                    0.00      10.18 r
 data arrival time                                            10.18

 clock CLK (rise edge)                             10.00      10.00
 clock network delay (ideal)                        0.50      10.50
 clock uncertainty                                 -0.10      10.40
 vector_y_r_reg_7__7_/CK (DFFRX2)                   0.00      10.40 r
 library setup time                                -0.22      10.18
 data required time                                           10.18
 ---------------------------------------------------------------------
 data required time                                           10.18
 data arrival time                                           -10.18
 ---------------------------------------------------------------------
 slack (MET)                                                  0.00
```

7. Area report



```
dc_shell> report_area

****************************************
Report : area
Design : matvecmult
Version: N-2017.09-SP2
Date   : Mon Dec  2 17:33:40 2019
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:                         1262
Number of nets:                          3152
Number of cells:                         1789
Number of combinational cells:           1584
Number of sequential cells:               170
Number of macros/black boxes:               0
Number of buf/inv:                        225
Number of references:                      57

Combinational area:              19750.946633
Buf/Inv area:                      933.569987
Noncombinational area:            4920.762608
Macro/Black Box area:                0.000000
Net Interconnect area:          203934.356842

Total cell area:                  24671.709240
Total area:                     228606.066082
```

8. 參考 sample 的檔案寫出來的,在研究 sequential circuit 怎麼運作時花了很多時間,由於我是第一次寫 verilog,目前對於怎麼讀出檔案還不太會,寫完作業四應該可以更加熟悉