

DSD Final Project Scores (RISC-V)

1. Baseline

(1) Area: (um²)

截圖: 314170.067183 um²

```
*****
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Sun Jun 28 17:57:53 2020
*****

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsvd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:          3418
Number of nets:           26994
Number of cells:          24077
Number of combinational cells: 19834
Number of sequential cells:  4229
Number of macros/black boxes: 0
Number of buf/inv:         4606
Number of references:      16

Combinational area:       205023.850652
Buf/Inv area:             34236.557844
Noncombinational area:    109146.216532
Macro/Black Box area:     0.000000
Net Interconnect area:    3268923.286682

Total cell area:          314170.067183
Total area:               3583093.353865
1
design_vision> report_timing
*****
```

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖: 9967.95 ns

```
=====
                NOW!      AFter reset
=====

Warning! Glitch suppression
Scheduled event for delayed signal of net "D" at time 8893710 PS was canceled!
File: ./tsmc13.v, line = 19876
Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[6]
Time: 8893530 PS

----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
Simulation complete via $finish(1) at time 9967950 PS + 0
./Final_tb.v:162          #(`CYCLE) $finish;
ncsim> exit
[b06176@cad29 src]$ █
```

(3) Area*Total Simulation Time: (um² * ns)

Area*Total Simulation Time = 3131631521.176785 um² * ns.

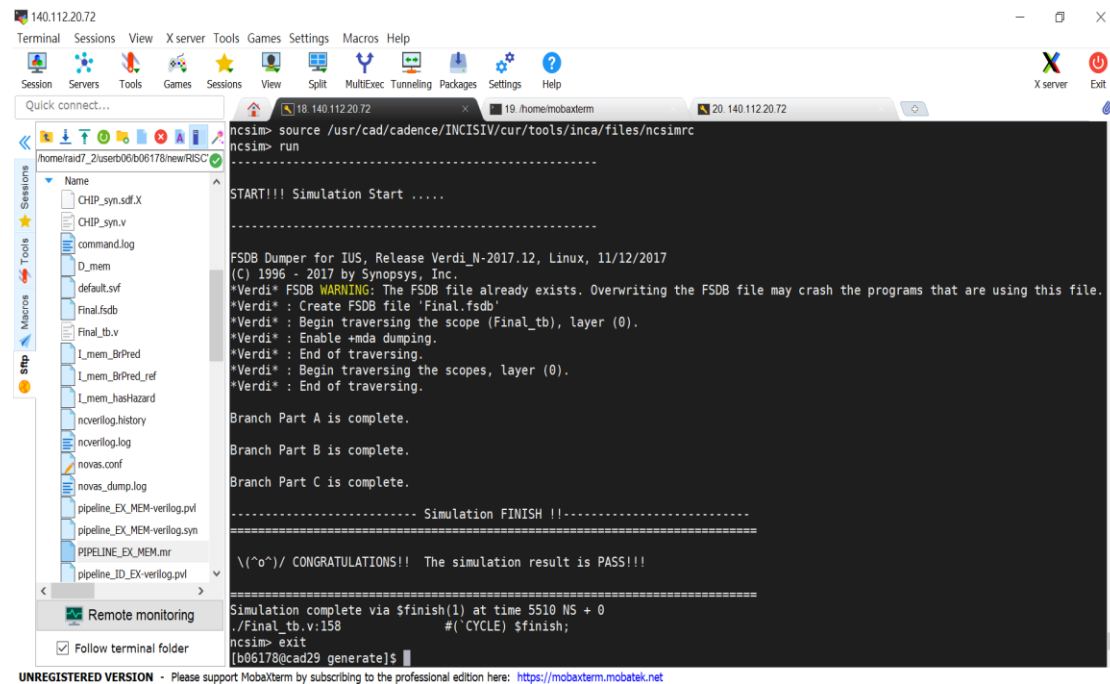
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

sdc: 4.0 ns, testbench: 5.1ns.

2. BrPred (以下cycle time皆為20ns)

(1) Total execution cycles of given I_mem_BrPred:

截圖:



```
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run

START!!! Simulation Start .....

FSDb Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDb WARNING: The FSDb file already exists. Overwriting the FSDb file may crash the programs that are using this file.
*Verdi* : Create FSDb file 'Final.fsd'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.

Branch Part A is complete.
Branch Part B is complete.
Branch Part C is complete.

..... Simulation FINISH !!.....

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

Simulation complete via $finish(1) at time 5510 NS + 0
./Final_tb.v:158          #('CYCLE') $finish;
ncsim> exit
[b06178@cad29 generate]$
```

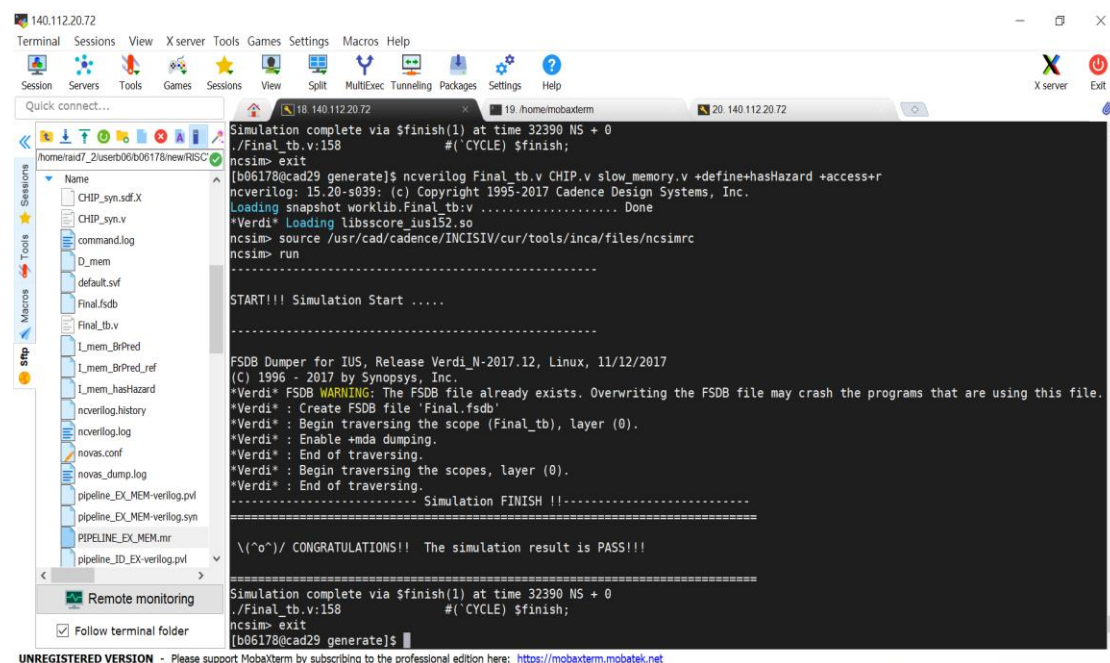
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

cycle time=20ns

cycle count=5510/20=275.5

(2) Total execution cycles of given I_mem_hasHazard:

截圖:



```
Simulation complete via $finish(1) at time 32390 NS + 0
./Final_tb.v:158          #('CYCLE') $finish;
ncsim> exit
[b06178@cad29 generate]$ ncvverilog Final_tb.v CHIP.v slow_memory.v +define+hasHazard +access+r
ncvverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
Loading snapshot worklib.Final_tb.v ..... Done
*Verdi* Loading libsscore_ius152.so ..... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run

START!!! Simulation Start .....

FSDb Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDb WARNING: The FSDb file already exists. Overwriting the FSDb file may crash the programs that are using this file.
*Verdi* : Create FSDb file 'Final.fsd'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.

..... Simulation FINISH !!.....

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

Simulation complete via $finish(1) at time 32390 NS + 0
./Final_tb.v:158          #('CYCLE') $finish;
ncsim> exit
[b06178@cad29 generate]$
```

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cycle time=20ns

cycle count=32390/20=1619.5

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um²)

BPU截圖:

The screenshot shows the MobaXterm interface with a terminal window displaying a Verilog synthesis report. The left sidebar shows a file tree with various design files. The terminal output includes a warning about Verilog statements, a command to write a ddc file, and a report area command. The report details the design's statistics and area calculations.

```
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
Writing ddc file 'CHIP_syn.ddc'.
design_vision> report_area

*****
Report : area
Design : CHIP
Version : N-2017.09-SP2
Date   : Mon Jun 29 16:31:49 2020
*****

Library(s) Used:

    typical (File: /home/raid7_2/course/cvscd/CBDK_IC_Constest/CIC/SynopsysDC/db/typical.db)

Number of ports:          4631
Number of nets:           26164
Number of cells:          21984
Number of combinational cells: 17839
Number of sequential cells:  4122
Number of macros/black boxes: 0
Number of buf/inv:        3857
Number of references:      5

Combinational area:      169517.637445
Buf/Inv area:            23778.876318
Noncombinational area:   112530.830503
Macro/Black Box area:    0.000000
Net Interconnect area:   3198316.222137

Total cell area:         282048.467948
Total area:              3480364.690086
1
design_vision>
```

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Baseline 截圖:

The screenshot shows the MobaXterm interface with a terminal window displaying a Verilog synthesis report for a Baseline design. The left sidebar shows a file tree with various design files. The terminal output includes a warning about Verilog statements, a command to write a ddc file, and a report area command. The report details the design's statistics and area calculations.

```
ge_names command to make the correct changes before invoking the verilog writer. (VO-11)
Writing ddc file 'CHIP_syn.ddc'.
design_vision> report_area

*****
Report : area
Design : CHIP
Version : N-2017.09-SP2
Date   : Mon Jun 29 17:00:07 2020
*****

Library(s) Used:

    typical (File: /home/raid7_2/course/cvscd/CBDK_IC_Constest/CIC/SynopsysDC/db/typical.db)

Number of ports:          3418
Number of nets:           24554
Number of cells:          21505
Number of combinational cells: 17388
Number of sequential cells:  4103
Number of macros/black boxes: 0
Number of buf/inv:        3751
Number of references:      5

Combinational area:      164977.092451
Buf/Inv area:            22965.821728
Noncombinational area:   105157.326490
Macro/Black Box area:    0.000000
Net Interconnect area:   3096582.386505

Total cell area:         270134.418941
Total area:              3366716.805446
1
design_vision>
```

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So Synthesis area of BPU = $282048 - 270134 = 11914 \text{ um}^2$

3. L2 Cache

(1) Average memory access time: (ns)

7.39(ns)

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖:

(用cycle = 4.5ns合成, cycle = 6.5ns通過simulation)

```
----- Simulation FINISH !!-----  
=====
```

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

```
=====
```

Simulation complete via \$finish(1) at time 279399250 PS + 0
./Final_tb_.v:163 #(`CYCLE) \$finish;
ncsim> exit

4. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

```
1  
design_vision> report_area  
  
*****  
Report : area  
Design : CHIP  
Version: N-2017.09-SP2  
Date : Sun Jun 28 22:15:52 2020  
*****  
  
Library(s) Used:  
  
typical (File: /home/raid7_2/course/cvsvd/CBDK_IC_Constest/CIC/SynopsysDC/db/typical.db)  
  
Number of ports: 4429  
Number of nets: 27179  
Number of cells: 21271  
Number of combinational cells: 16707  
Number of sequential cells: 4543  
Number of macros/black boxes: 0  
Number of buf/inv: 4465  
Number of references: 23  
  
Combinational area: 189933.966197  
Buf/Inv area: 38987.580402  
Noncombinational area: 128752.880806  
Macro/Black Box area: 0.000000  
Net Interconnect area: 2943655.068390  
  
Total cell area: 318686.847003  
Total area: 3262341.915393  
1  
design_vision> █
```

Area Total = $318686.847003 \text{ um}^2$

So Synthesis area of BPU = $318686.847003 - 314170.067183 = 4516.77982 \text{ um}^2$

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:

```
=====
Now After reset
=====

Warning! Glitch suppression
Scheduled event for delayed signal of net "D" at time 1220354 PS was canceled!
File: ./tsmc13.v, line = 19876
Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[26]
Time: 1220196 PS

Warning! Glitch suppression
Scheduled event for delayed signal of net "D" at time 1420954 PS was canceled!
File: ./tsmc13.v, line = 19876
Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[26]
Time: 1420796 PS

Warning! Glitch suppression
Scheduled event for delayed signal of net "D" at time 1521254 PS was canceled!
File: ./tsmc13.v, line = 19876
Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[26]
Time: 1521096 PS

Warning! Glitch suppression
Scheduled event for delayed signal of net "D" at time 1621554 PS was canceled!
File: ./tsmc13.v, line = 19876
Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[26]
Time: 1621396 PS

----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
Simulation complete via $finish(1) at time 2280350 PS + 0
./Final_tb.v:162                               #(`CYCLE) $finish;
ncsim> exit
[b06176@cad29 DEADxF625]$
```

Total Simulation Time of given I_mem_compression = 2280.350 ns.

(3) Area*Total Simulation Time: (um² * ns)

Area*Total Simulation Time = 726717551.5632911 um² * ns.

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

sdc: 4.0 ns, testbench: 5.9ns.