DSD Final Project Scores (RISC-V)

1. Baseline

(1) Area: (um^2)

截圖: 314170.067183 um^2

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****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Sun Jun 28 17:57:53 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         3418
Number of nets:                         26994
Number of cells:                        24077
Number of combinational cells:          19834
Number of sequential cells:              4229
Number of macros/black boxes:               0
Number of buf/inv:                       4606
Number of references:                      16

Combinational area:             205023.850652
Buf/Inv area:                    34236.557844
Noncombinational area:          109146.216532
Macro/Black Box area:                0.000000
Net Interconnect area:         3268923.286682

Total cell area:                314170.067183
Total area:                    3583093.353865
1
design_vision> report_timing

****************************************
```

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖: 9967.95 ns

```
================================================================================

           NOW!     AFter reset



================================================================================

Warning!  Glitch suppression
           Scheduled event for delayed signal of net "D" at time 8893710 PS was canceled!
            File: ./tsmc13.v, line = 19876
           Scope: Final_tb.chip0.i_RISCV.pipeline3.\o_result_r_reg[6]
            Time: 8893530 PS

-------------------------- Simulation FINISH !!---------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 9967950 PS + 0
./Final_tb.v:162              #(`CYCLE) $finish;
ncsim> exit
[b06176@cad29 src]$
```

(3) Area*Total Simulation Time: (um^2 * ns)

Area*Total Simulation Time = 3131631521.176785 um^2 * ns.

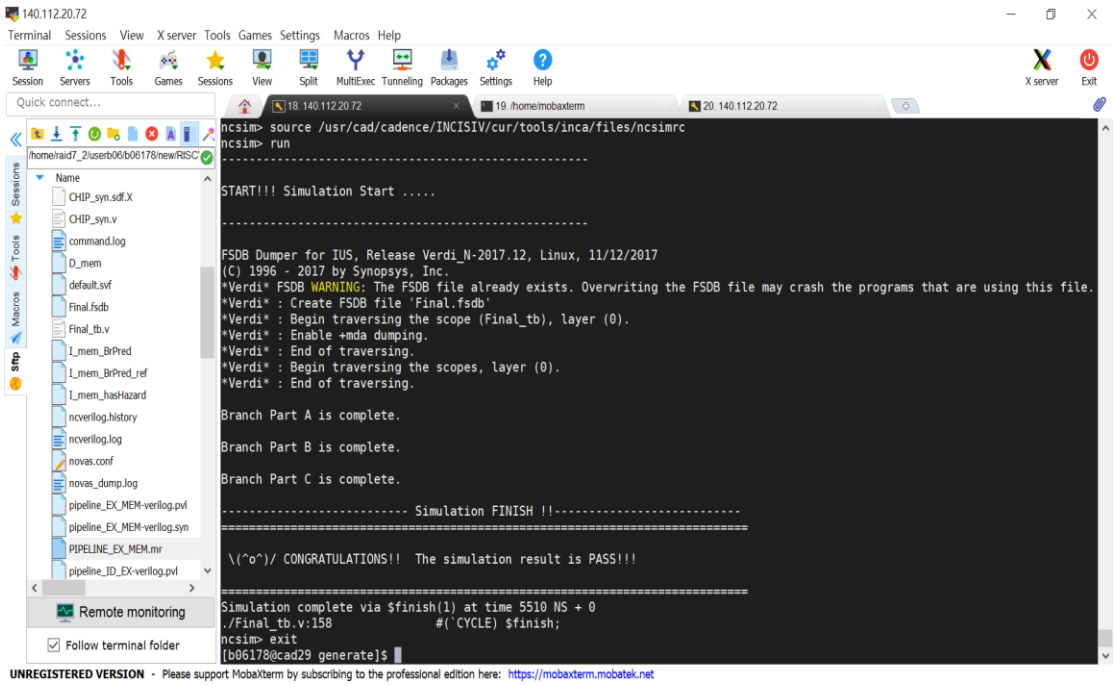
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

sdc: 4.0 ns, testbench: 5.1ns.

2. BrPred (以下cylce time皆為20ns)

(1) Total execution cycles of given I_mem_BrPred:

截圖:

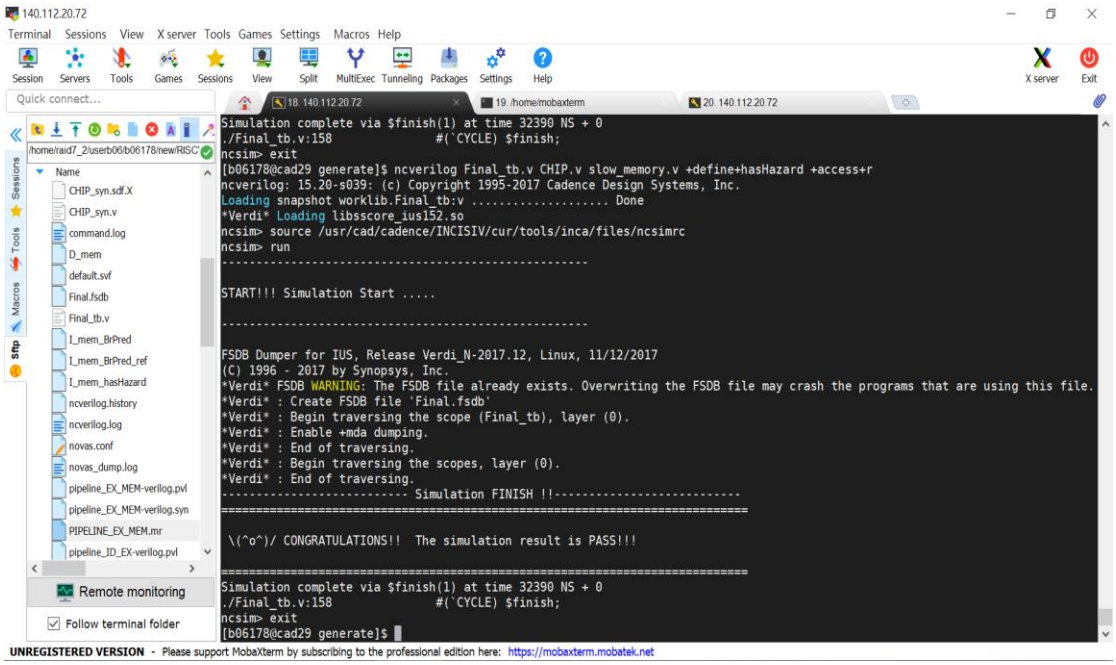


cycle time=20ns

cycle count=5510/20=275.5

(2) Total execution cycles of given I_mem_hasHazard:

截圖:

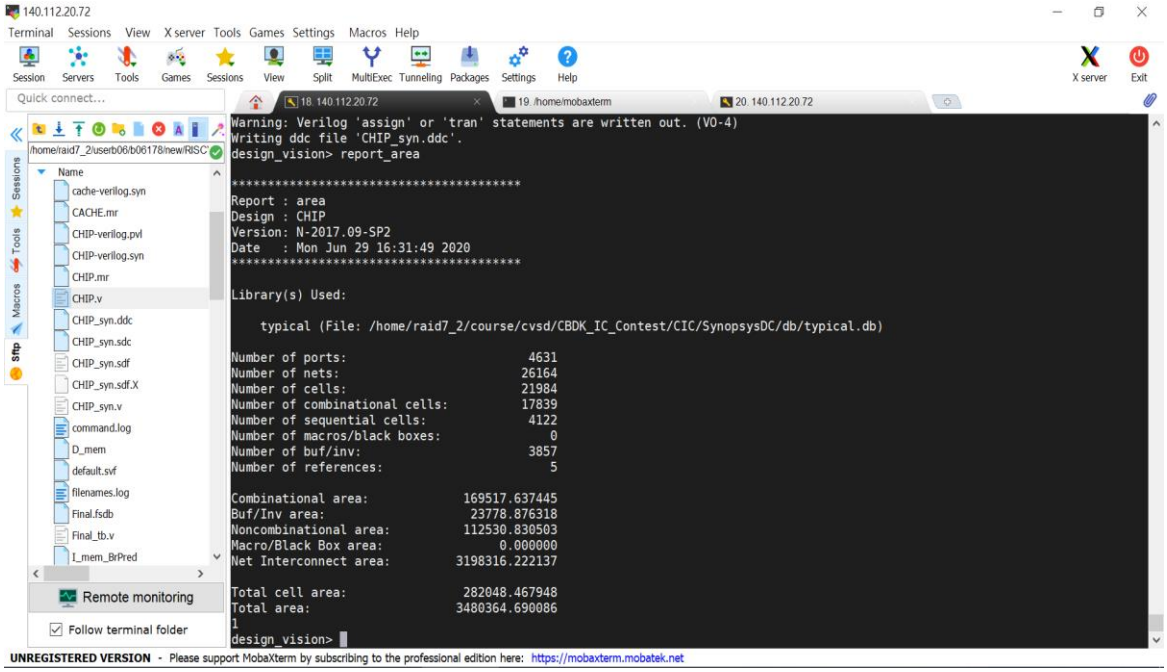


cycle time=20ns

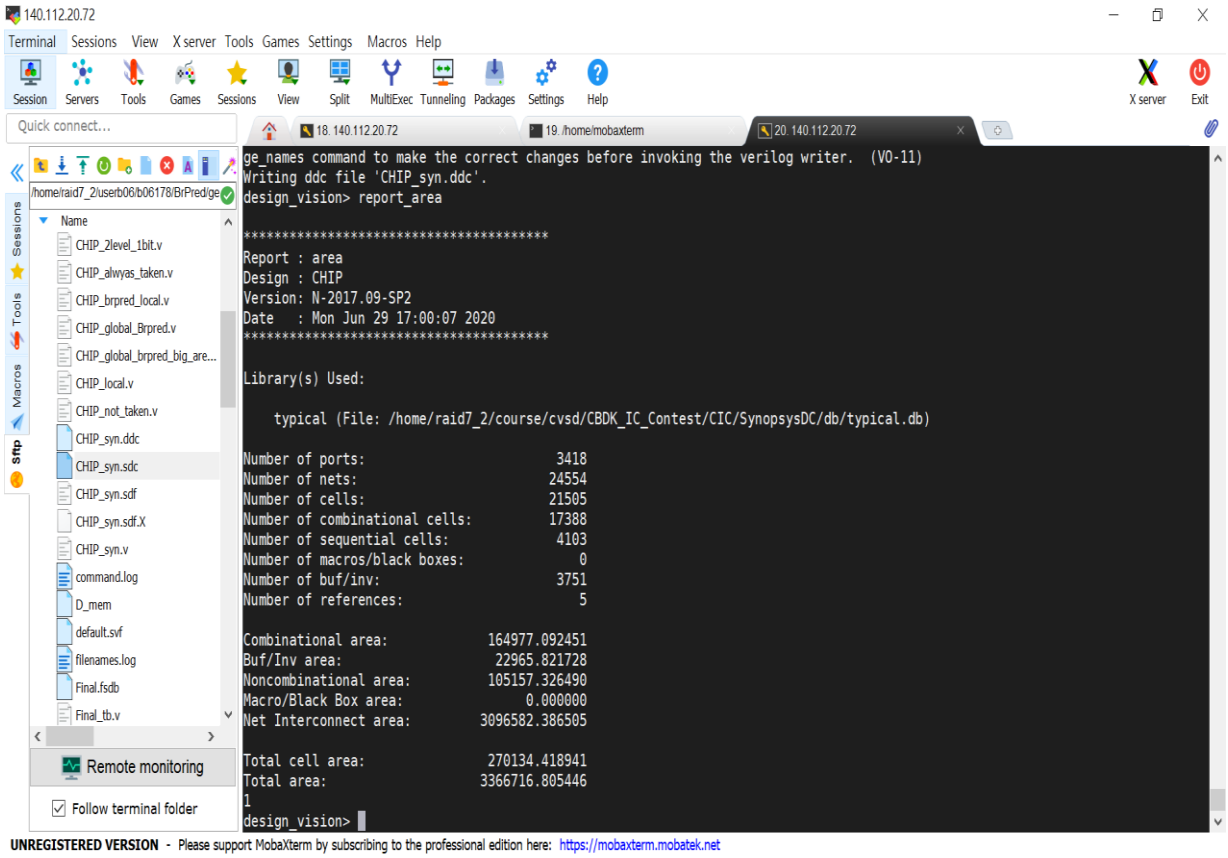
cycle count=32390/20=1619.5

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

BPU截圖:



Baseline 截圖:



So Synthesis area of BPU =282048-270134=11914 um^2

3. L2 Cache

(1) Average memory access time: (ns)

7.39(ns)

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖:

(用cycle = 4.5ns合成, cycle = 6.5ns通過simulation)

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--------------------------- Simulation FINISH !!---------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 279399250 PS + 0
./Final_tb_.v:163              #(`CYCLE) $finish;
ncsim> exit
```

4. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

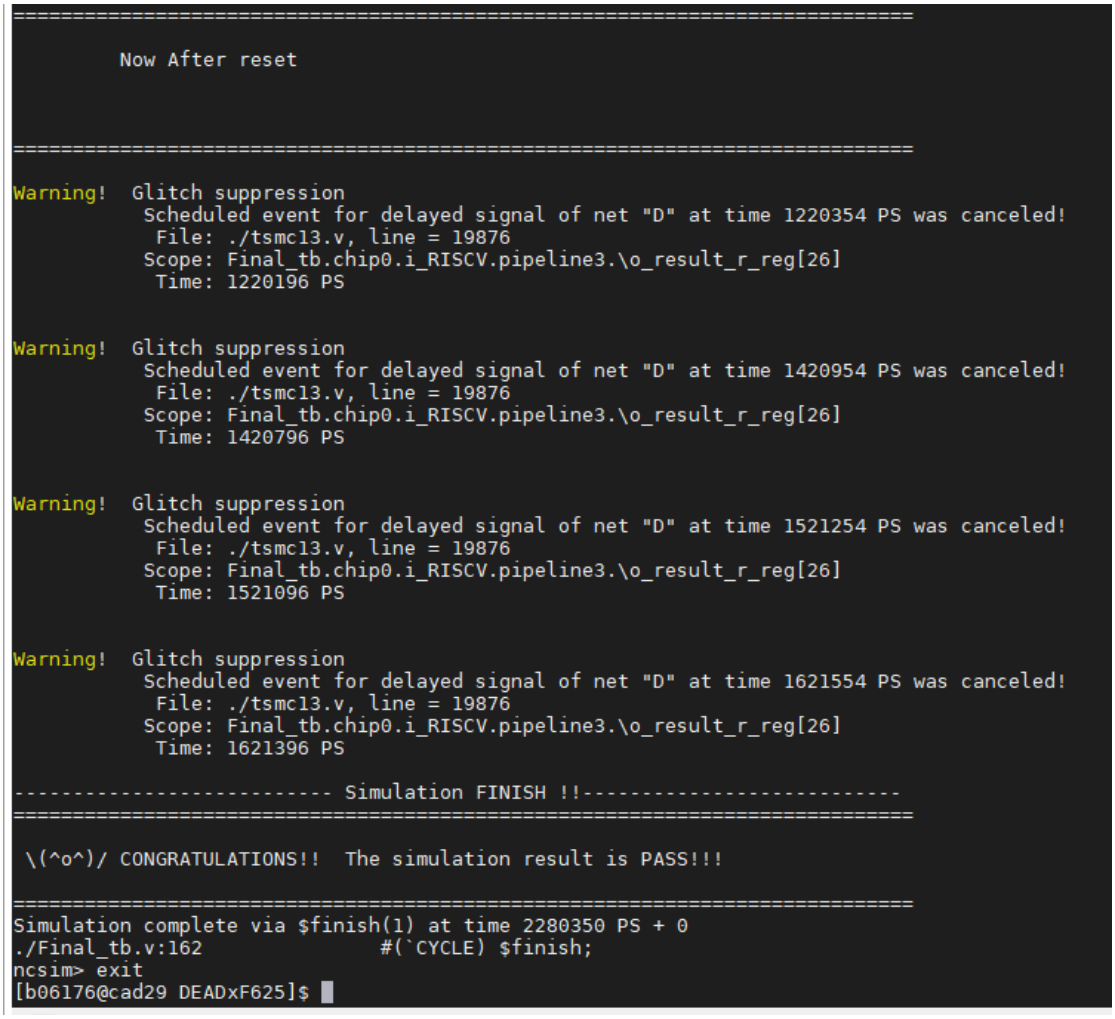
```
1
design_vision> report_area

****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Sun Jun 28 22:15:52 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         4429
Number of nets:                         27179
Number of cells:                        21271
Number of combinational cells:          16707
Number of sequential cells:              4543
Number of macros/black boxes:               0
Number of buf/inv:                       4465
Number of references:                      23

Combinational area:             189933.966197
Buf/Inv area:                    38987.580402
Noncombinational area:          128752.880806
Macro/Black Box area:                0.000000
Net Interconnect area:         2943655.068390

Total cell area:                318686.847003
Total area:                    3262341.915393
1
design_vision>
```

Area Total = 318686.847003 um^2

So Synthesis area of BPU = 318686.847003 - 314170.067183 = 4516.77982 um^2

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:



Total Simulation Time of given I_mem_compression = 2280.350 ns.

(3) Area*Total Simulation Time: (um^2 * ns)

Area*Total Simulation Time = 726717551.5632911 um^2 * ns.

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

sdc: 4.0 ns, testbench: 5.9ns.