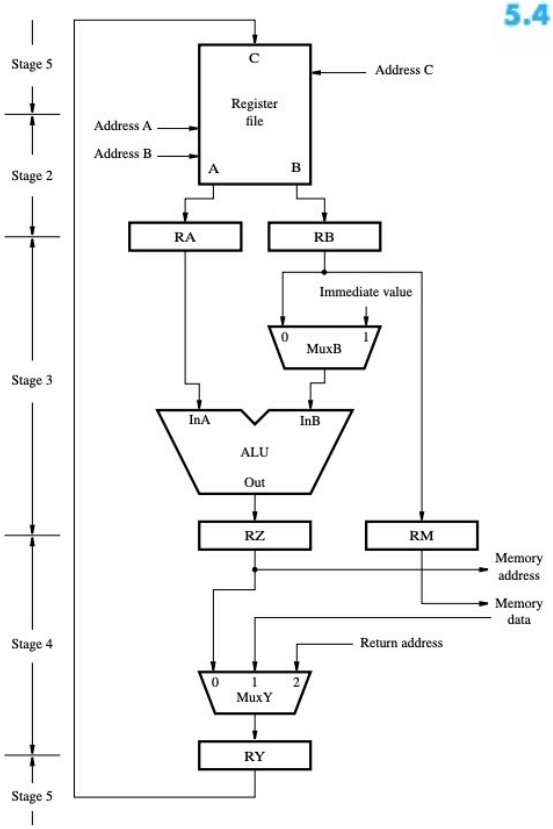
Homework #5 : Matt Krieger



5.4 [M] At some point in the execution of a program, registers R4, R6, and R7 contain the values 1000, 7500, and 2500, respectively. Show the contents of registers RA, RB, RZ, RY, and R6 in Figure 5.8 during steps 3 to 5 as the instruction

Subtract R6, R4, R7

is fetched and executed, and also during step 1 of the instruction that is fetched next.

Subtract R6, R4, R7

1. memory address ← [PC], Read Memory, IR ← memory data, PC ← [PC] + 4
2. Decode Instruction, RA ← [R4], RB ← [R7]
3. RZ ← [RA] - [RB]
4. RY ← [RZ]
5. R6 ← [RY]

Step	RA	RB	RZ	RY	R6
3	7500	2500	5000	?	1000
4	7500	2500	5000	5000	1000
5	7500	2500	5000	5000	5000

5.11 [M] A RISC processor that uses the five-step sequence in Figure 5.4 is driven by a 1-GHz clock. Instruction statistics in a large program are as follows:

Branch	20%
Load	20%
Store	10%
Computational instructions	50%

Estimate the rate of instruction execution in each of the following cases:

(*a*) Access to the memory is always completed in 1 clock cycle.

(*b*) 90% of instruction fetch operations are completed in one clock cycle and 10% are completed in 4 clock cycles. On average, access to the data operands of a Load or Store instruction is completed in 3 clock cycles.

Step	Action
1	Fetch an instruction and increment the program counter.
2	Decode the instruction and read registers from the register file.
3	Perform an ALU operation.
4	Read or write memory data if the instruction involves a memory operand.
5	Write the result into the destination register, if needed.

a)

instruction execution Rate = $\frac{\text{clock speed}}{\text{clock cycles per instruction}}$

$= \frac{1\text{GHz}}{5} = 200\ \text{MIPS}$

b)

(0.9 × 1) + (0.1 × 4) = 0.9 + 0.4 = 1.3 cycles

(0.8 × 3) + (0.2 × 8.33) + (0.1 × 8.33) + (0.2 × 5) = 2.5 + 1.66 + 0.83 + 1 ≈ 6 cycles per instruction

Execution Rate = $\frac{1\text{GHz}}{6} = 166.7\ \text{MIPS}$

5.12 [E] The execution of computational instructions follows the pattern given in Figure 5.11 for the Add instruction, in which no processing actions are performed in step 4. Consider a program that has the instruction statistics given in Problem 5.11. Estimate the increase in instruction execution rate if this step is eliminated, assuming that all execution steps are completed in one clock cycle.

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R4], RB ← [R5]
3	RZ ← [RA] + [RB]
4	RY ← [RZ]
5	R3 ← [RY]

new: 4 steps
old: 5 steps

1:4 cycle : step
1:5

Increase Factor = $\frac{\text{New Execution Rate}}{\text{old Execution Rate}} = \frac{1/4}{1/5} = \frac{5}{4} = 1.25$

% increase = $\left(\frac{5-4}{5}\right) \cdot 100 = 25\%$

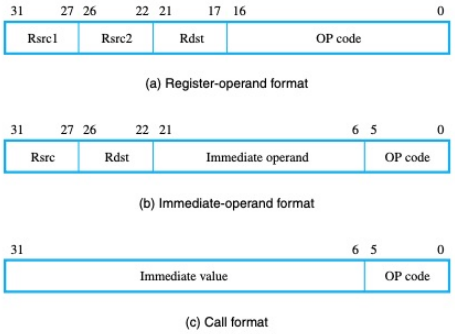
5.14 **[M]** The instructions of a computer are encoded as shown in Figure 5.12. When an immediate value is given in an instruction, it has to be extended to a 32-bit value. Assume that the immediate value is used in three different ways:

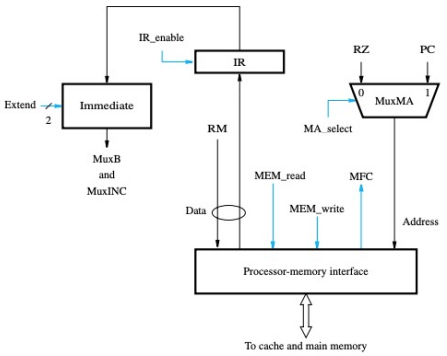
(*a*) A 16-bit value is sign-extended for use in arithmetic operations.

(*b*) A 16-bit value is padded with zeros to the left for use in logic operations.

(*c*) A 26-bit value is padded with 2 zeros to the right and the 4 high-order bits of the PC are appended to the left for use in subroutine-call instructions.

Show an implementation for the Immediate block in Figure 5.19 that would perform the required extensions.





a) Register-operand format :
- Rsrc1, Rsrc2, Rdst & OP-code
- no immediate value present

b) Immediate-operand format :
- Rsrc, Rdst & OP-code
- immediate operand is 16-bit → 32 bit.

c) Call format :
- 26-bit immediate value and OP code field.
- requires 2 zero padding 4 bits from PC 26+2+4 = 32 bits

Select :
00
01
10