Matt Krueger – Computer Architecture Homework #2

**Q1. What is the basic design unit of Verilog?**

Module – modules are the basic design unit that encapsulate functionality and model hardware components. Models have ports, wires, and registers to describe functionality. **Q2. What are the two Verilog procedural block types and how are they used?**

1. Initial block – executes at the start of the program. Used for initialization of variables.
2. Always block – executes repeatedly on sensitivity list. And is used to model sequential or combinational logic.

**Q3. What are the two basic Verilog signal types?**

1. Registers – holds a value (assignment)
2. Wires – represents a physical connection between components.

**Q4. What are the four Verilog signal values?**

1. 0 – logic low
2. 1 – logic high
3. Z – high impedance
4. X – unknown value