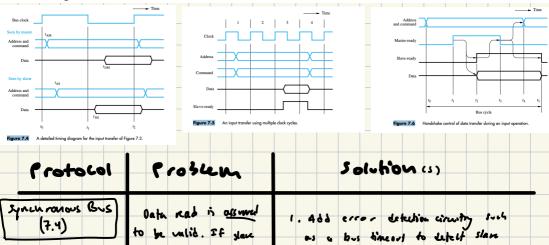
Chapter 7 problems 7.4, 7.10, 7.16, 7.18. Maft Kny

[M] Figures 7.4, 7.5, and 7.6 show three protocols for transferring data between a master and a slave. What happens in each case if the addressed device does not respond due to a malfunction during a Read operation? What problems would this cause and what remedies are possible?



didn't respond the to matter / slave synchro malfunction, state/bad Jaka is latched to clock yell ourst be low eaugh to tolerate most Mastro register.

be formance

BAO DATA LATCHED! If slave new asurb

signal then master may indefinity be liskny for a call that will not come. This majes

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Master seeds yest by rainy "Marke rady" 5-6 "slaw realy" new correct This is like previous cooper signal.

mal Ruchon

2. Add states (Ack/NACK) flags

1. Add himout same reasoning of

1. watchdog times for reetting stare

or exception flogs to

make system rob-14

1. as you probably guessed: Another timeous

if "slaw rady" not received the stop when three is a bus "mater ray". This can be done via an lock/Hread Stonetion excepton waitiz... promone

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(1.5)

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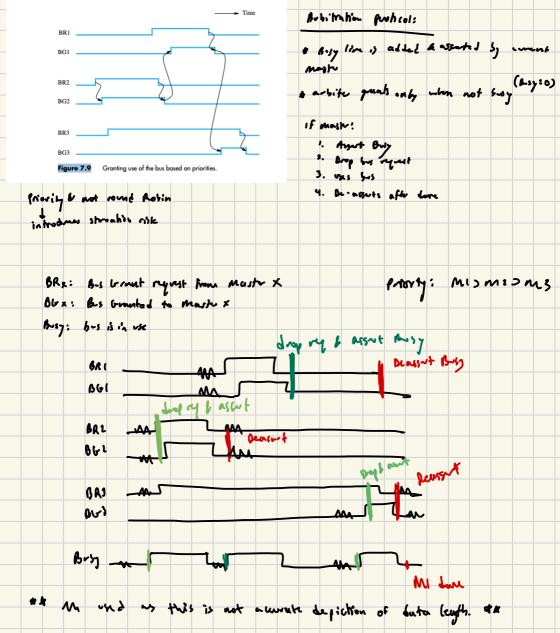
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Asynchronous Bus

(7.6)

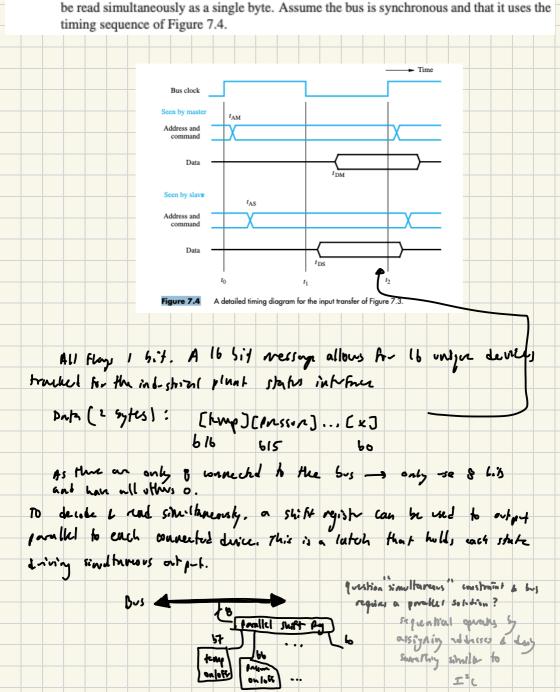
Chapter 7 problems 7.4, 7.10, 7.16, 7.18. **Maff Knyy**

[M] In the arbiter protocol example depicted in Figure 7.9, the master that receives a bus grant maintains its request line in the asserted state until it is ready to relinquish bus mastership. Assume that a common line called Busy is available, which is asserted by the master that is currently using the bus. The arbiter grants the bus only when Busy is inactive. Once a master receives a grant, it asserts Busy and drops its request, and in response the arbiter drops the grant. The master deactivates Busy when it is finished using the bus. Draw a timing diagram equivalent to Figure 7.9 for this mode of operation.



Chapter 7 problems 7.4, 7.10, 7.16, 7.18. Maff Kny

7.16 [M] An industrial plant uses several sensors to monitor temperature, pressure, and other factors. Each sensor includes a switch that moves to the ON position when the corresponding parameter exceeds a preset limit. Eight such sensors need to be connected to the bus of a 16-bit computer. Design an appropriate interface to enable the state of all eight switches to



Chapter 7 problems 7.4, 7.10, 7.16, 7.18. MI Data are stored in a small memory in an input interface connected to a synchronous bus that uses the protocol of Figure 7.5. Read and Write operations on the bus are indicated by a Command line called R/W. The speed of the memory is such that two clock cycles are required to read data from the memory. Design a circuit to generate the Slave-ready response of this interface. Cycle 1. Cycle 1. Cycle 1. Shall actually shall be shall	Chant	- 7 proble	mas 7.4	710.7	14 7 10			r.n.		
bus that uses the protocol of Figure 7.5. Read and Write operations on the bus are indicated by a Command line called R/W. The speed of the memory is such that two clock cycles are required to read data from the memory. Design a circuit to generate the Slave-ready response of this interface. Cycle 1: Cav soul, althers, command 2: Slave accuses sponell recovery connected 3: Data calid; Slave ready ascentel 4: Master reads data; slave ready deactored circuit dass; a: clock to synchronizer address decoder / command decoder to dataset taled read accuse the slave of the sponential sylvy slave ready. If no store the store of the st									7	
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