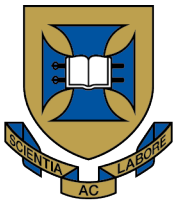

THE UNIVERSITY OF QUEENSLAND

AUSTRALIA

RF Switching system for Biomedical Radar systems

by

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Submitted for the degree of
Bachelor of Engineering
in the field of Electrical Engineering

November 3, 2016

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November 3, 2016

Prof Paul Strooper
Head of School
School of Information Technology and Electrical Engineering
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Dear Professor Strooper,

In accordance with the requirements of the degree of Bachelor of Engineering in the division of Electrical Engineering I present the following thesis entitled "RF Switching System for Biomedical Radar Systems". This work was performed under the supervision of Dr. Konstanty Bialkowski.
I declare that the work submitted in this thesis is my own, except as acknowledged in the text and footnotes, and has not been previously submitted for a degree at The University of Queensland or any other institution.

Yours sincerely,

Matt Pascoe

Matt Pascoe.

Abstract

This document is a skeleton thesis for 4th-year students. The printable versions (`skel.dvi, skel.ps, skel.pdf`) show the structure of a typical thesis with some notes on the content and purpose of each part. The notes are meant to be informative but not necessarily illustrative; for example, this paragraph is not really an abstract, because it contains information not found elsewhere in the document. The LaTeX 2_ε source file (`skel.tex`) contains some non-printing comments giving additional information for students who wish to typeset their theses in LaTeX. You can download the source, edit out the unwanted material, insert your own frontmatter and bibliographic entries, and in-line or `\include{}` your own chapter files. Of course the content of a particular thesis will influence the form to a large extent. Hence this document should not be seen as an attempt to force every thesis into the same mold. If in doubt about the structure of your thesis, seek advice from your supervisor.

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Chapter 1

Introduction

1.1 Background

There has been a growing demand for the development of wireless systems, to meet the increasing demands of consumers. In order to meet this demand researchers have looked to software defined radio's (SDR); this interest in SDR is due to the ease and simplicity for the development and implementation in various applications. This rise in interest has led to a large spike in development of SDR, which is resulting in a broadened application for SDR. [1]

SDR's are being applied in a variety of different scenarios, but this thesis focuses primarily on the development of a switching system to complement the research done using SDR as a tool for medical imaging. The use of SDR in microwave imaging has provided an alternative diagnostic tool that presents significant benefits of current technology, primarily because of its low cost, portability, non-invasiveness and uses non-ionization radiation. This allows the system to be compact and suitable for medical application in the field. [2] [3]

As the demand for faster wireless systems increases, so does the interest in researching the application of using multiple antenna wireless links for digital communication; using multiple antennas introduces a greater range of possibilities by increasing the speed of the networks traffic [4]. To accommodate for the control of multiple radio frequency (RF) front ends the communication system will require a RF switching system; there are two primary categories for RF and microwave switches, electromechanical relay (EMR) and solid-state relay (SSR).

There are advantages and disadvantages in use either, SSR's are available in smaller packages and have a higher switching speed but are restricted to single pole, EMR's have a lower isolation loss but are have slower speed due to their physical construction. SSR don't have a wearable switching mechanism while EMR do, making them

impractical in scenarios which require large amounts of switching [5]. Therefore, this thesis will primarily focus on utilising SSR's as opposed to EMR's, to meet the high speed requirements while maintaining a low cost and compact design.

This thesis project looks into the development of an RF switching system to allow an RF front end to be connected to a large number of antennas or sensors, by developing a RF switch matrix that provides a high speed switching on multiple antennas. The results obtained from this will facilitate and support the expansion in the current development of biomedical RF imaging systems as well as future projects.

1.2 Aims/Objectives

This thesis aims to evaluate the current available designs and products to develop a low-cost and portable RF switch matrix.
The primary objective are to complete the following tasks:

- Evaluate and Design a RF Switch matrix
- Develop and Construct the RF Switch matrix
- Finalise and construct a housing for the switch matrix

1.3 Thesis Structure

Chapter 2 investigates the prior technology available that can be adapted or utilised in order to assist in the development of RF switching system.
Chapter 3 defines the relevant theory that is required to understand the topics discussed in this thesis.
Chapter 4 looks into the analysis and development of RF switches.
Chapter 5 depicts the flow of the project, starting from the thesis's definition and following it through the solution, design, simulation, implementation and results.
Chapter 6 contains performance results of the RF switch matrix, and the RF switch matrix's characteristics.
Chapter 7 discusses the performance of the produced switch matrix and future work.

1.4 Expected Contribution

The thesis will look at developing a low-cost RF switch matrix capable of providing a 2 input, 16 output switching matrix. It should reveal the possibility of developing switch matrix's that are better suited to low-cost, portable projects in contrast to commercially available switches.

This thesis is expected to produce a proprietary switch matrix that can enable the further development of low-power RF development in biomedical and radar applications.

Chapter 2

Literature review

2.1 Prior Art

This chapter looks into the currently available designs used for high speed RF switching as well as relevant theory that has and is being completed in the field.

2.1.1 Currently Available Technology

There is currently a wide variety of application for RF switching systems, EMR are primarily used but there has been recent interest in SSR applications. EMR switching systems are a predominate choice due to their low losses and have been utilised in many various applications. A journal article in [6] looks at the performance of micro-electromechanical systems (MEMS) and the wide field of application for MEMS in communications, medical and aerospace; this wide field means that there is a large application that can benefit from the development of RF switching systems. As seen in [6] RF switching systems have a wide range of application, it can be seen in [25], which investigate the interference problem of a MIMO beam-switching antenna. In order to control the multiple beam switching antennas requires a high speed switching system, therefore they utilised a SSR allowing them to achieve speeds from 1-100ns; this high speed capability is ideal for the application of the thesis [7].

There is also a large application for RF switching systems in medical imaging, which is the primary focus of this thesis. The journal article in [3] describes a medical imaging system that uses a RF system, it rotates a body around an antenna by a stepper motor to obtain measurements from antenna at different positions; this system utilises a SDR and a single antenna to obtain its measurements as it rotates around the body. It was determined that the current microwave imaging system currently takes 45 minutes to complete its analysis, but by replacing the rotating platform with an array of 20 antennas using a EMR switching network could reduce

the time to less than 1 minutes [3]. Since we are expecting SSR to provide a faster switching speed reducing the time taken for the measurements to be completed.

The journal articles [8], [9] that discuss the use of EMR technology to allow a RF front end to control multiple antennas in different applications of biomedical engineering. In [8] a network of EMR is used to allow a VNA to perform radar measurements through 16 antennas in the frequency domain. The switches are controlled by a computer and takes around 3 minutes for the measurements to be taken [8]. An article from [9] looks at using an array of RF antennas switched by an EMR so they can image a head to detect a haemorrhage stroke. [9] The need for RF switching systems can be seen but the use of SSR instead of EMR can potentially reduce the size and noise of the switching while increasing the speed allowing their design to be faster, more compact and quieter which is potentially ideal for medical applications.

2.1.2 Previous designs

In order to develop the PCB

2.2 Software Defined Radio

The application of the RF switching system this thesis looks a developing, is to provide an RF front end such as a software defined radio (SDR) or Vector Network Analyser (VNA) with the ability to communicate multiple antennas or sensors. An SDR is a radio that is partially or entirely controlled by software in the physical layer in the Open Systems Interconnection (OSI) model. The OSI model is used to describe the subsystems of a communication system, where the physical layer represents the data. This allows for the software or firmware to be adjusted resulting in the change the carrier frequency, data rate, modulation, coding, etc. without having the reconstruct the hardware of the radio [10]. This project doesn't look into the control of an SDR, instead focuses on interfacing the switching system with the SDR. It is expected that the SDR will have an impedance of $50\,\Omega$ which is common of most SDR technology or a less common impedance of $75\,\Omega$ [11].

2.2.1 Analysing SDR Signals

2.2.2 Radar Signal Analysis

2.3 Microwave Theory

To design and develop microwave circuits a fundamental understanding of how microwaves operate and ... in ... is required

2.3.1 Transmission Line Theory

A transmission line is a medium that transfers electromagnetic energy along its path, an example can be seen in Figure 2.1. Transmission lines will form the primary basis of this thesis since it will be primary medium for the signal travelling through the RF switching system. It is crucial to ensure that the transmission line matches the source and antenna; otherwise it can cause the power to be reflected back.

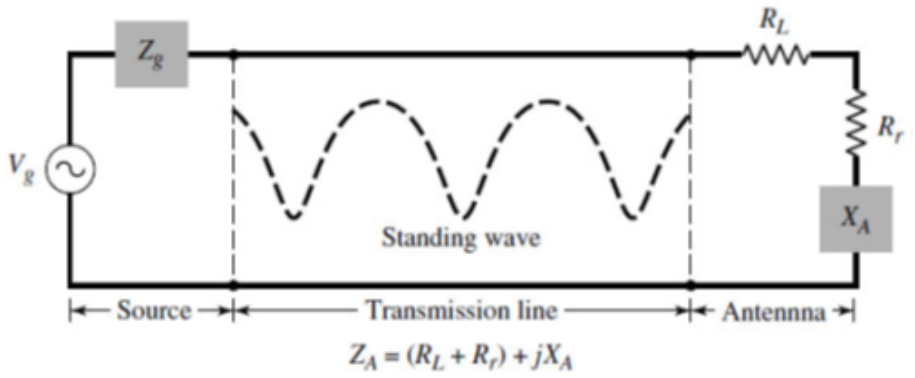

Figure 2.1: Transmission line Thevenin equivalent of antenna and transmitter

To prevent this reflection, the impedances at each end must be matched to the transmission lines characteristic impedance. This can be done through L-section matching, stepped transmission lines or filters.

L-section is a method used for matching transmission lines; this involves using a capacitor and inductor in a series and parallel combination to match the load. Stepped transmission lines provides impedance matching for lumped elements. Finally, filters can also be used for impedance matching; they are typically used to provide an adjustable match for the circuit over different frequencies. By inserting a filter that is a perfect match for the transmission line at a known frequency [12]. This theory will be considered when evaluating the design for the development boards and if required the PCB so they are perfectly matched to reduce any unnecessary losses in the system.

2.3.2 Scattering Parameters

Scattering parameters (S-Parameters) are a matrix that describes the behaviour of linear electrical networks; this matrix is used over a broad range of disciplines of electrical engineering but is particularly useful in microwave engineering.
Since the RF switching system this thesis is designing will not generating its own signal or provide any RF front end's; even though the system is switching, it will always have a single input and single output. Therefore, this design can be simplified to be a 2-port network, as shown in Figure 2.2.

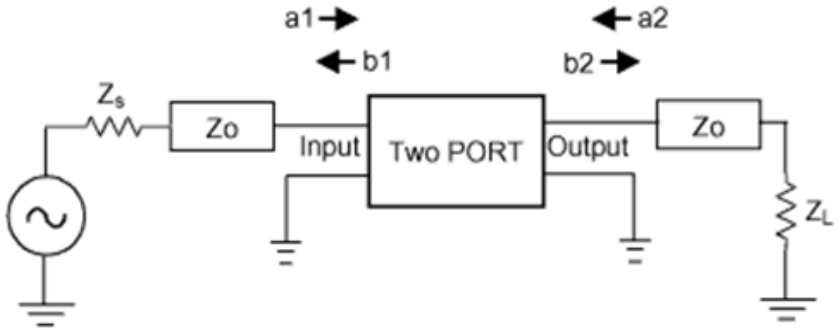

Figure 2.2: 2-port switching system [10]

2-port networks are most commonly used and can easily be adapted to systems that are more complex, Figure 2.2 shows a simple diagram of a 2-port network and Equation 2.1 shows the matrix and equations given for the network [12].

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{11} & S_{12} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$
$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

These parameters can be directly measured with a network analyser and will be used to determine the characteristics of the different RF switches.

2.3.3 System Losses

When working with RF and microwave systems it is important to understand the different types of losses that can occur in the system and how it will affect the performance. There are three significant losses to be consider, these are insertion loss, return loss and isolation.
Insertion loss is the loss of the signals power in decibels (dB) from the insertion of a

device in the input or output of the system. The loss can be determined given the scattering equation of the system, as defined in Equation 2.2.

$$Insertion\ loss = -20 \cdot \log_{10}(|\Gamma|) \tag{2.2}$$

The return loss is the loss of the signals power in dB from the signal reflection; this is often caused by an impedance mismatch on the load. The loss can be determined given the reflection coefficient, as shown in Equation 2.4.

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{2.3}$$

$$Return\ loss = -20 \cdot \log_{10}(|\Gamma|) \tag{2.4}$$

The isolation is the degree of attenuation from other signals from outside or on other channels in the system. Increasing the isolation of the device reduces the influence of other signals. The isolation of the system can be determined by measuring the signal strength at an output where the input is not routed to. [12] All of these parameters need to be seriously considered, and form the base of the analysis for the design and development of the RF switching system.

2.4 RF Switch

There are two typical types of switches that are used in RF and microwave switching systems, electromechanical switches (EMR) and solid-state switches (SSR). These switches are often available in four different topologies:

- Single-pole double-throw (SPDT)
- Single-pole-multiple-throw (SPnT)
- Double-pole-double-throw (DPDT)
- Bypass switch [11]

This project is interested in the development of a single input with multiple outputs so will look into utilising combinations of SPDT and SPnT topologies to meet this requirement.
Solid-state relay's (SSR) are typically constructed in semiconductor packaging, giving them a small size and are switched by applying an external voltage across its control terminals. Since there are no physical switching mechanisms for SSR, there is no component to wear out allowing the SSR to potentially switch an infinite amount of times.
Whereas electromechanical relays (EMR) rely on a mechanical contact to switch the outputs, resulting in an often larger size. Since there is a physical movement required to switch the outputs the EMR, there will be limit on the number of switches

before it begins to fail; this is not particularly idea for the RF switching system this thesis is looking at as it will require switches to be replaced after set period depending on its usage.
EMR's have a larger frequency range than most SSR's, they support frequencies from DC to the GHz range whereas SSR's often begin around the KHz up to GHz; both switches are ideal as the switch will be working in high frequencies. The insertion loss is often greater in SSR compared to most EMR's but SSR's provide a greater isolation in comparison against EMR. On average, the SSR's provide a greater switching speed with significantly lower settling time making them ideal for high speed switching [5].
Both switches have advantages and disadvantages; however, this project looks into the development of a switching system to switch at high speeds with minimal losses, size, noise and power. SSR are the most suitable for meeting these requirements and will therefore be the primary focus of this project.

2.5 RF Switches Matrix

This thesis topic looks into the development of a RF switching system, this will be done by utilising RF and microwave switches to create an RF switching matrix. An RF switch matrix are used to route RF signals from an input to an output.
There are several different types of switching matrix's, there is multiple input multiple output (MIMO), multiple input single output (MISO), single input multiple output (SIMO) and single input single output (SISO) [13]. For this project we are looking at controlling multiple outputs with a single input, so will be implementing a SIMO RF switching matrix.

2.5.1 Switch Architecture

2.5.2 Switch Topologies

When constructing a RF switch there are two typical topologies, these are multiplexers and general purpose relays; examples can be seen in Figure 3. General purpose relays are commonly a SPDT or SDnT relay's that are used for routing a signal between multiple paths. Multiplexers are devices that route a single input to multiple outputs or vice versa, they are commonly built from multiple SPDT relays but have a greater inherited insertion loss from this configuration [14].

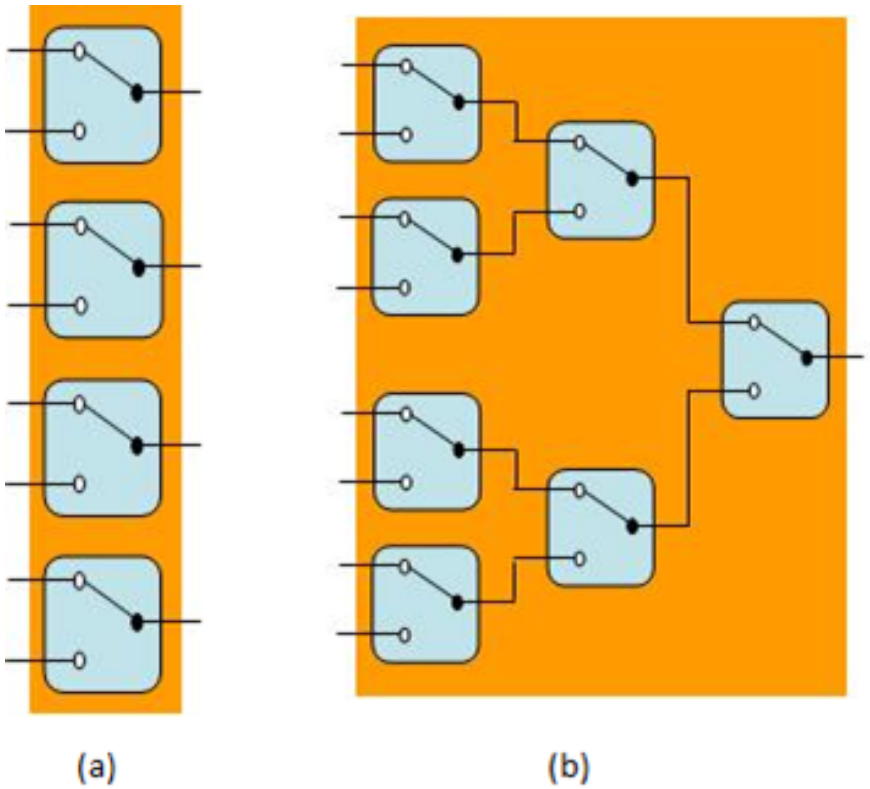

Figure 2.3: (a) is a Quad SPDT, (b) 8x1 multiplexer

Looking at Figure 2.3 (b) it can be assumed that there will be losses through each path it takes, insertion loses through first switch, first cable/track, second switch, etc. Therefore, it is ideal to develop a topology as close to Figure 2.3 (a) to ensure there is little loss through multiple cascaded switches and cable/tracks. This thesis will be looking into designing a 2x16 MIMO multiplexer, similar to the design in Figure 2.3 (b) to provide the available ports as well as a consistent loss through the system.

2.5.3 Cabling

When developing the RF switching system it is probable to require cables to connect the switches together. If the development boards are used it will be a requirement, and the PCB development could be built into separate daughter boards and connected together via cable.
There are three main types of coax cabling:

- Semi-rigid
- Comfortable
- Flexible

This project will look into the use of semi-rigid SMA cables, as they typically have low losses for signal transmission and are well suited for fixed devices [16]. The connection between will need to be measured and matched as discussed in Section 2.3.1 to ensure that the signal retains its integrity.

2.6 Substrate Selection

There are various substrates that are available for developing the RF switching matrix. Four key substrates were looked at these include:

- FR-4
- Epoxy

Table B.1 contains the characteristics of these four substrates that are utilised to calculate the dimensions of the RF tracks. When designing PCB's for

2.7 RF Transmission Line Design

For designing the RF transmission line on the PCB there are three primary options available

- Micro-strip
- Coplanar Wave-guide, and
- Strip-line

RF tracks provide ...
For designing the tracks we need to consider:

$$\lambda = \frac{c}{f\sqrt{\epsilon_{eff}}} \tag{2.5}$$

$$\theta = \frac{2\pi}{\lambda} \tag{2.6}$$

We need to consider the Figure 2.5 and 2.6 as these are the fundamentals for designing any type of track. To determine which track is best suited this thesis will look at each available option.
These equations are used for the approximate design of RF tracks, in order to obtain a more precise design which consider a wider range of variables dedicated software is used to further verify the design of the tracks.

2.7.1 Micro-strip

Microstrip RF tracks are the most common RF transmission line currently used in practice. Figure 2.4 presents a typical microstrip which has been labelled the critical

dimensions of this transmission line.

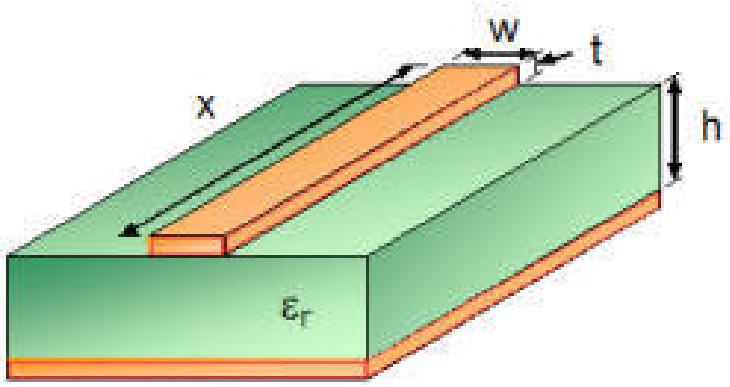

Figure 2.4: Microstrip diagram

We are able to calculate the dimensions shown in Figure 2.4 by using the following:

$$W = \frac{t}{\pi}\left[ln\left(\frac{2h}{t}\right) + 1\right] \tag{2.7}$$

$$H = h - 2t \tag{2.8}$$

$$\epsilon_{eff} = \begin{cases} \frac{\epsilon_r + 1}{2} + \frac{\epsilon - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12H}{W}}} + 0.04\left(1 - \frac{W}{H}\right)^2\right] & when\left(\frac{W}{H}\right) < 1 \quad (2.9a) \\ \frac{\epsilon + 1}{2} + \frac{\epsilon - 1}{2\sqrt{1 + \frac{12H}{W}}} & when\left(\frac{W}{H}\right) > 1 \quad (2.9b) \end{cases}$$

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}} \cdot ln\left(\frac{8H}{W} + \frac{W}{4H}\right), & when\left(\frac{W}{H}\right) < 1 \quad (2.10a) \\ \frac{120\pi}{\sqrt{\epsilon_{eff}} \cdot \left[\frac{W}{H} + 1.393 + \frac{2}{3}ln\left(\frac{W}{H} + 1.444\right)\right]}, & when\left(\frac{W}{H}\right) > 1 \quad (2.10b) \end{cases}$$

In order to calculate the dimensions of the micro-strip track we are required to make key decisions for the design. By selecting the frequency range, impedance, phase shift substrate and track thickness we are able to determine the dimensions for the track.

We are able to determine the width (W) and length(X) of the track by selecting a substrate determining the dielectric constant (ϵ_{eff}), copper thickness (t) and height(H). We can set the

2.7.2 Strip-line

Strip-line RF tracks are ...

We are able to calculate the dimensions shown in Figure 3.2

$$\begin{aligned}\beta &= \frac{\omega}{v_p} \\ &= \sqrt{\epsilon_r} \cdot k_0 \end{aligned} \tag{2.11}$$

$$\begin{aligned}Z_0 &= \sqrt{\frac{L}{C}} \\ &= \frac{1}{v_p \cdot C} \end{aligned} \tag{2.12}$$

$$\frac{W_e}{b} = \begin{cases} \dfrac{W}{b} & when\left(\frac{W}{b}\right) > 0.35 \quad (2.13a) \\ \dfrac{W}{b} - \left(0.35 - \dfrac{W}{b}\right)^2 & when\left(\frac{W}{b}\right) < 0.35 \quad (2.13b) \end{cases}$$

$$\frac{W}{b} = \begin{cases} x & when\sqrt{\epsilon_r} \cdot Z_0 < 120\,\Omega \quad (2.14a) \\ 0.85 - \sqrt{0.6 - x} & when\sqrt{\epsilon_r} \cdot Z_0 < 120\,\Omega \quad (2.14b) \end{cases}$$

$$x = \frac{20\pi}{\sqrt{\epsilon_r \cdot Z_0}} \tag{2.15}$$

2.7.3 Coplanar Wave-guide

C

2.8 Radiation Emission

2.8.1 Picket Fencing Technique

2.8.2 Shielding

Chapter 3

Methodology

This chapter of the thesis looks at the methodology employed in the design and development of the RF switch matrix. For this Thesis the design stage has been broken into five primary sections:

- Evaluation of RF switches
- Design a switch matrix
- Develop PCB design
- Evaluate the RF switch matrix
- Construction of matrix enclosure

These sections will be further discussed to analyse the progression of the design and development of the RF switch matrix.

3.1 Evaluation

This section looks at evaluating the currently available RF switch evaluation boards listed in Section 3.1.1 that can be used, and alternative possibilities in developing a custom RF switch matrix.

3.1.1 Evaluation Boards

We currently have 4 evaluation RF switch boards available; these include:

asdf	$50 USD
asdf	$50 USD
asdf	$50 USD

The three available evaluation boards we investigated using a Anritsu MS46322A Vector Network Analyser (VNA); each switch was wired so that the input is connected to the output, while all other ports were 50 Ω terminated. The switch was powered and the controls set to allow the signal to propagate down the open path,

then changed the state to have a closed path; this was conducted for each evaluation board. The results were exported to a *.s2p* file to be analysed using ADS, and the results can be seen in Appendix **??** 's Figure's **??**, **??** & **??**.
These simulations
The results of ... is the most ideal RF switch out of the three boards, but the overall price to construct the switch matrix is far too expensive to construct as it will cost $50 which is unrealistic to rival

3.1.2 RF Switches

It was seen in previous section that the EMR and switch relay provided significantly better results for: insertion, isolation and reflection but are significantly larger and heavier than SSR's tested. Since this thesis is looking at developing a lightweight switch matrix it is decided that high performance SSR's will be looked at instead of EMR.

For constructing the switch matrix there are three primary topolgies that will be looked at since, SP16T are not largely available at a low price, instead this thesis will look at cascading two or more switches that are SPDT, SP4T or SP8T; to create a custom SP16T switch.
There is a large variety of RF switches available in varying topologies, the following RF switches were identified as interesting:

asdf	$50 USD
asdf	$50 USD
asdf	$50 USD

These are the RF switches that will be further investigated in this thesis to determine if a custom RF switch design is able to constructed at a competitive price to the evaluation boards seen in Section 3.1.1. It can already be seen that the individual price is significantly cheaper but will require a PCB to be constructed; this will allow the design to be custom designed to fit in the most space efficient package possible to allow for a portable and lightweight design.

3.1.3 Transmission Line Design

Using the ADS three different transmission lines were tested, using the parameters seen in Appendix B, Table 3.1 was constructed.

Track Type	Width	Length	Gap
Micro-strip			-
Strip-line			-
Co-planar Wave-guide			

Table 3.1: Transmission Line Design Parameters

Therefore looking at Table 3.1 it can be seen that the most space efficient transmission line is the CPWG design; therefore, the CPWG design allows the PCB to be the most space efficient design for the RF switch design.
In addition to the Grounded CPWG, picket fencing will be added to the tracks to ensure that there is minimal amount of losses or noise entering the system as seen in Section 2.8.1. The picket fence was a single row of via's spaced from the track by ...mm and each other by ...mm, the diameter of the via's were ...mm following the standard method for adding picket fences specified in .... []

3.2 Design

For the design of the RF switch matrix, several key design citerias were identified to be required for the final product of the switch matrix; these specifications are:

- Two RF inputs
- Sixteen RF outputs
- Maximum path loss of 3dB
- Power-able from low-power device (such as USB)
- Input and output of switch matrix are $50\,\Omega$

In order to construct the DP16T switch matrix the the design will be split into two stages, an input and output stage. The input stage will take a two different inputs, the switch will be controlled to route a path from the input to the output; this will require two separate SP16T RF switch. Each output of DP16T matrix needs to be able to switch between the two outputs of each SP16T switch, therefore this design will require 16 SPDT switches. An example of the way the switch matrix will be wired can be seen in Figure 3.1.

In order to meet these specifications several different designs have been developed, which can be seen in Section 3.2.1 - 3.2.5. There are three different SP16T switch designs for the input and two SPDT output switch designs for the output; to determine the most suitable design these five designs are designed to determine a suitable low-loss, high isolation switch matrix.

All the design's for the SP16T switches will feature an SMA input for the input to

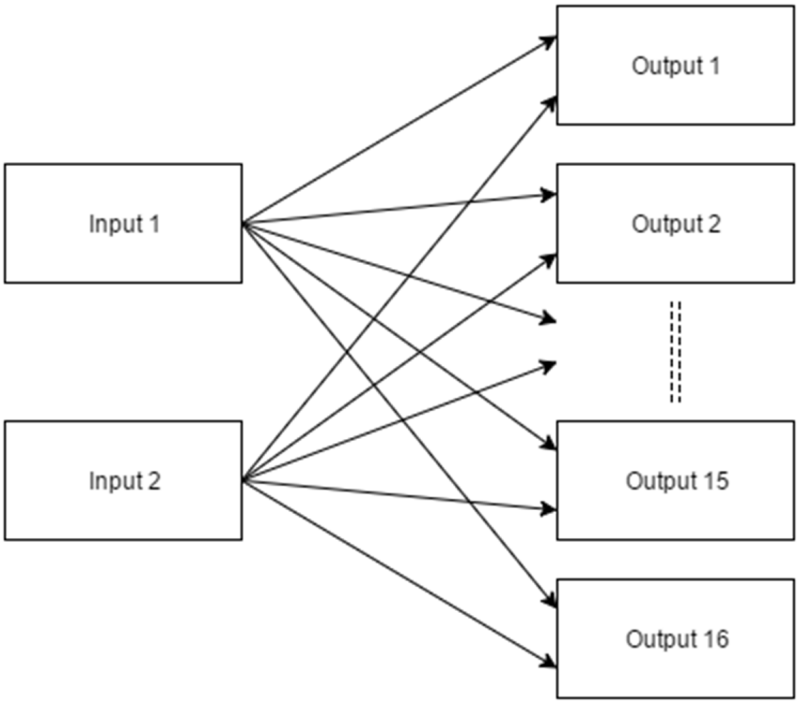

Figure 3.1: Block Diagram of Switch Matrix

the switch matrix, and UFL connectors on the output. Since the internals of the design will be restricted from the consumer UFL cabling allows for a much more compact and flexible design. This selection is expected to have a poor insertion loss compared to SMA but is significantly more flexible and thinner allowing for the overall size of the switch matrix to be reduced significantly.
The output switches will feature a similar design; where the input to the SPDT switch is SMA and the two outputs will be UFL. The SPDT switch will need to be $50\,\Omega$ terminated when inactive to ensure that there isn't any reflections occurring within the switch if the signal is being routed to the same output, since the design in a blocking switch matrix.

3.2.1 Design 1

This design looks at constructing a SP16T RF switch using the SKY13418-485LF and MASWSS0115 cascaded together. The SKY13418 is a SP8T switch that provides a low insertion loss that has a frequency range from 100MHz to 3Ghz. The chip features the input in the centre with 4 outputs either side of the input. This allows for the tracks to be spaced by 30^o segments, and the remainder to be space for logic. To get full 16 outputs the design requires a MASWSS0115 SPDT switch on each output of the SP8T; from the switches that are being evaluated the MASWSS0115 provides the lowest insertion loss, although it has a poor reflection on the output. The SKY13418 has DC blocking integrated into the chip by the MASWSS0115

doesn't, therefore it requires DC blocking capacitors of 33 pF to be placed on all of the RF inputs and outputs.

This design was developed in Altium Designer and can be seen in Figure 3.2.

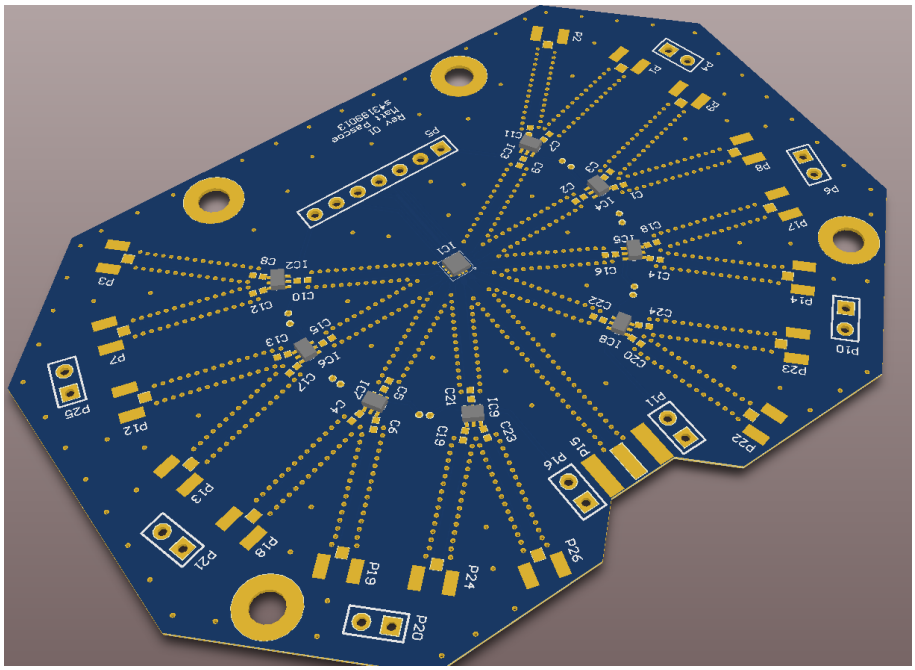

Figure 3.2: PCB Design for 'Design 1'

Specifications

Therefore using this combination of SP8T and SPDT switches we are able to estimate the parameters of the switch based off of the specifications in the data-sheet as seen in Table 3.14.

Parameter	Value				
	100MHz	1GHz	2GHz	3GHz	4Ghz
Insertion					
Isolation					
Input Reflection					
Output Reflection (Inactive)					
Max. Switching Speed					

Table 3.2: Design 1 - Ideal parameters

It can be seen that the expected insertion loss is relatively low at a maximum of 1dB loss, the isolation is not too bad with a minimum of 1dB.

SP8T			
State	V_1	V_2	V_3
RF1	Off	Off	Off
RF2	Off	Off	On
RF3	Off	On	Off
RF4	Off	On	On
RF5	On	Off	Off
RF6	On	Off	On
RF7	On	On	Off
RF8	On	On	On

SPDT		
State	V_1	V_2
RF1	On	Off
RF2	Off	On

Table 3.4: Logic Control Table for 'Design 1'

Control

In order to control this board there are 3 control pins for the SP8T switch, and 16 control pins for the SPDT switches. The logic voltages for this board are detailed in Table 3.3.

RF Switch	Off	On
SP8T	0V$\pm$0.3V	1.35V - 2.7V
SPDT	0V$\pm$0.2V	2.3V - 5V

Table 3.3: Logic Voltage Control

Therefore this the device can be controlled using a 4-bit number representing the current active switch for the input. Using the logic control table specified in Table 3.4 a logic table has been drawn to design a suitable method to control the SP16T switch with minimal amount of cabling and components required; the results can be seen in Appendix D.1. Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first bits are connected to each SPDT switch and the last three bits are connected to the SP8T switch.

3.2.2 Design 2

This design looks at constructing an alternative design to SP16T RF switch using a different topology from Section 3.2.1; it was found that the SP4T PE42441 Evaluation Board tested in Section 3.1.1 provided good performance for both insertion and isolation. By cascading the SP4T together with itself would provide 16 possible transmission lines for the switch. By using the same transmission line design used

in Design 1, an alternative construction of the SP16T switch can be designed. By designing this board on a PCB it is able to significantly more space efficient, cost effective with less cabling than what would be required to construct it from the tested evaluation board seen in Section 3.1.1.

The pins on the PE42441 were spaced so that the transmission lines could be angled 45^o apart from each other. This was done for each chip leading from the SMA to UFL. Similar to 'Design 1' the track length was designed to provide enough spacing for the PE42441 chips and UFL connectors from each other and the header connectors. The chips do not require DC blocking so no capacitors are required on the input or outputs; following the specifications on the PE42441's data-sheet, 0.1 μFdecoupling capacitors were added to the V_{cc}, V_0 and V_1.

This design was developed in Altium Designer and can be seen in Figure 3.3.

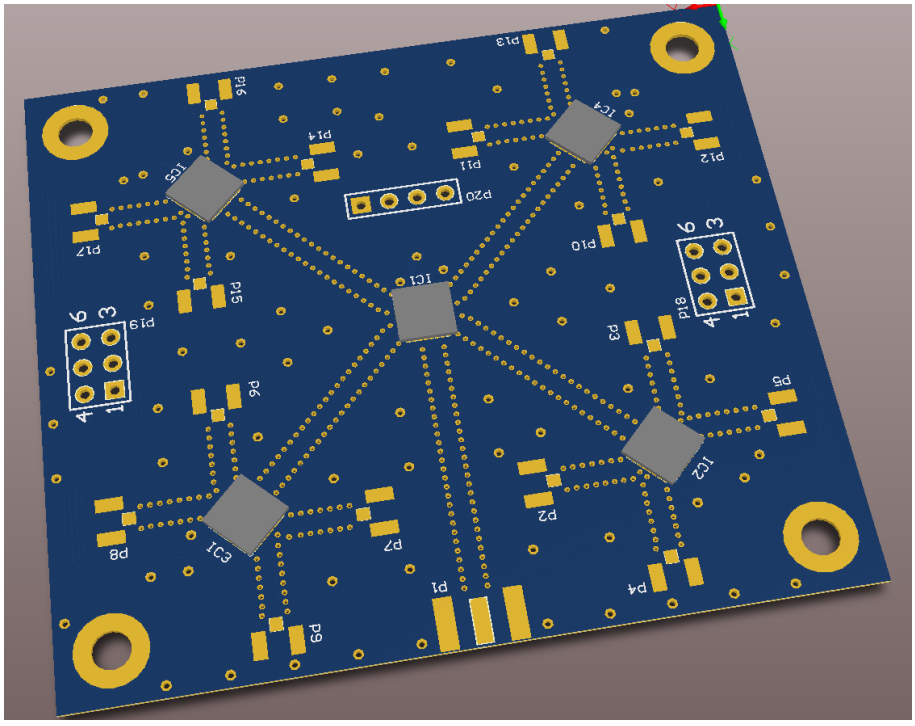

Figure 3.3: PCB Design for 'Design 2'

Specifications

Therefore using the SP4T switches cascaded together the performance of the switch can be estimate the parameters of the switch based off of the specifications presented in the PE42441's data-sheet; the estimated performance can be seen in Table 3.14.

Parameter	Value				
	100MHz	1GHz	2GHz	3GHz	4Ghz
Insertion Isolation Input Reflection Output Reflection Max. Switching Speed					

Table 3.5: Design 1 - Ideal parameters

It can be seen that the expected insertion loss is relatively low at a maximum of 1dB loss, the isolation is not too bad with a minimum of 1dB.

Control

In order to control this board there are 10 control pins for the SP4T switch; the logic voltages for this board are detailed in Table 3.12.

RF Switch	On	Off
SP4T	0V$\pm$0.3V	1.35V - 2.7V

Table 3.6: Logic Voltage Control

Therefore this the device can be controlled using a 4-bit number representing the current active switch for the input. Using the logic control table specified in Table **??** a logic table has been drawn to design a suitable method to control the SP16T switch with minimal amount of cabling and components required; the results can be seen in Appendix **??**.

State	V_1	V_2
RF1	Off	Off
RF2	On	Off
RF3	Off	On
RF4	On	On

Table 3.7: Logic Control Table for 'Design 2'

Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first two bits are connected to each of the cascaded SP4T switches and the last two bits are connected to the centre SP4T switch.

3.2.3 Design 3

This design looks at constructing a SP16T RF switch using an similar design to Design 2, this utilises the PE42442 chip which is from the same family as the PE42441. Similar to the PE42441, the PE42442 is a SP4T RF switch that slightly varies in their specifications. The PE42442 provides a lower input power, but provides a slightly better insertion and isolation response in comparison to the PE42441. This allowed for a similar set-up for the board layout where the first SP4T switch leads to a second cascaded SP4T switch.

The device is able to be compacted into a smaller board due to the alternate arrangement of pins in comparison to Design 2; this new Altium design can be seen in Figure 3.7. The boards are arranged so that they are symmetrical down the centre, each chip is spaced to provide enough space for the logic control lines and V_{cc} to be able to be connected to the chip without running underneath any of the transmission lines. This required the two centre outputs from the first RF chip, IC2 and IC5, to be spaced 90^o apart from each other the two edge chips were then spaced 60^o away to provide enough room for the data lines to connect to the RF chips.

This design was developed in Altium Designer and can be seen in Figure 3.7.

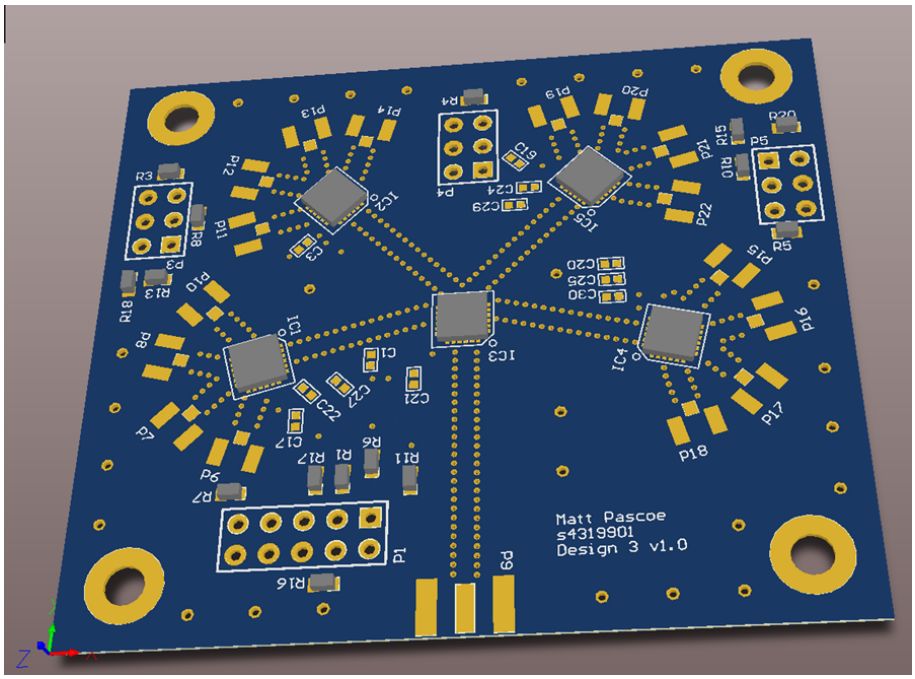

Figure 3.4: PCB Design for 'Design 3'

Specifications

Therefore using the SP4T switches cascaded together the performance of the switch can be estimate the parameters of the switch based off of the specifications presented

in the PE42442's data-sheet; the estimated performance can be seen in Table 3.14.

Parameter	Value				
	100MHz	1GHz	2GHz	3GHz	4Ghz
Insertion Isolation Input Reflection Output Reflection Max. Switching Speed					

Table 3.8: Design 1 - Ideal parameters

It can be seen that the expected insertion loss is relatively low at a maximum of 1dB loss, the isolation is not too bad with a minimum of 1dB.

Control

In order to control this board there are 15 control pins for the SP4T switch, but since this design doesn't require an all-on or all-off state we are able to ground the third voltage pin and only use 10 control pins for switching the SP4T; the logic voltages for this board are detailed in Table 3.15.

RF Switch	On	Off
SP4T	$0V \pm 0.3V$	1.35V - 2.7V

Table 3.9: Logic Voltage Control

Therefore this the device can be controlled using a 4-bit number representing the current active switch for the input. Using the logic control table specified in Table 3.16 a logic table has been drawn to design a suitable method to control the SP16T switch with minimal amount of cabling and components required; the results can be seen in Appendix **??**.

State	V_1	V_2
RF4	Off	Off
RF1	Off	On
RF2	On	Off
RF3	On	On

Table 3.10: Logic Control Table for 'Design 3'

Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first two bits are connected to each of the cascaded SP4T switches and the last two bits are connected to the centre SP4T switch.

3.2.4 Output 1

The output design requires constructing a SPDT switch for the output of the RF switch matrix, this requires a switch that has low insertion loss and isn't reflective. The switch should also include

This design was developed in Altium Designer and can be seen in Figure 3.5.

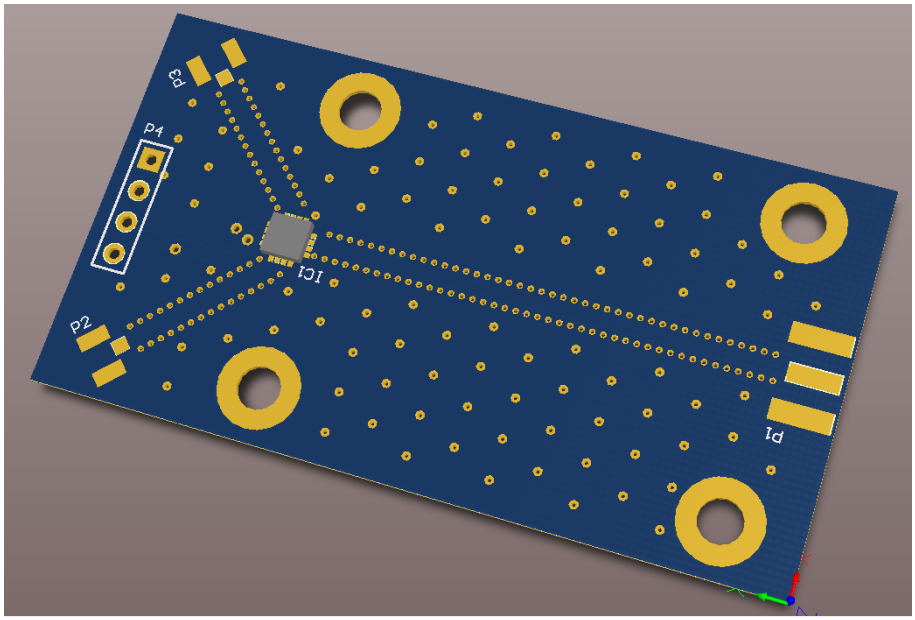

Figure 3.5: PCB Design for 'Output 1'

Since it was later found in Section **??** that this RF Switch was better suited that 'Output 2' it was decided to construct the switch matrix output of 16 PE42423 SPDT switches. Fitting 16 of the PCB boards seen in Figure 3.5 would be take up more spacing than required and since FR-4 substrate was used could lead to a large amount of variance in dielectric constant between each board. Therefore a larger board which contains 4 separate PE42423 RF switch was designed in Altium Designer which can be seen in Figure 3.6. This also allows for a more structurally sound board which is able to fit into case easier.

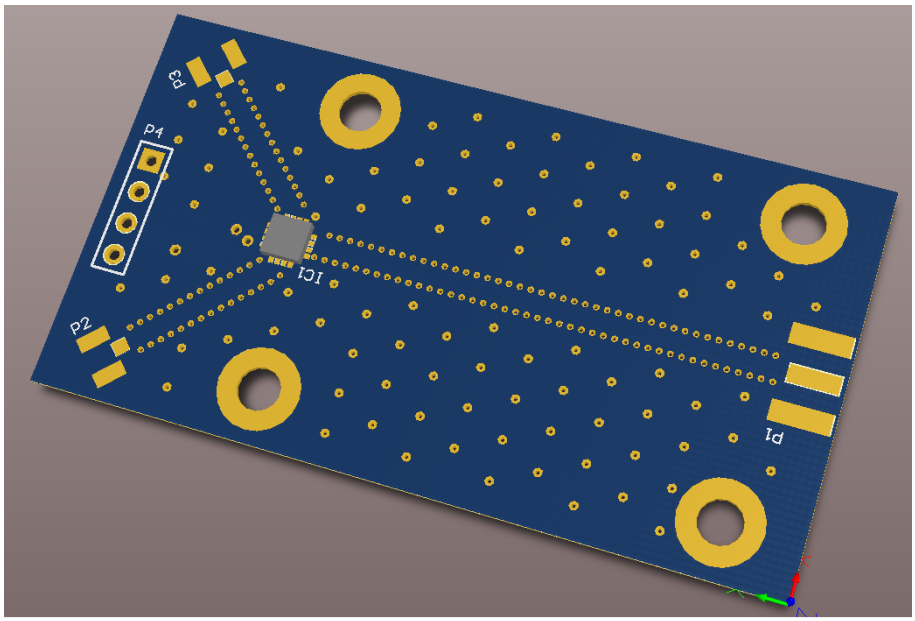

Figure 3.6: Combined PCB Design for 'Output 1'

Parameter	Value			
	1GHz	2GHz	3GHz	4Ghz
Insertion Isolation Input Reflection Output Reflection Max Switching Speed				

Table 3.11: Design 3 Ideal parameters

It can be seen that the expected insertion loss is relatively low at a maximum of 1dB loss, the isolation is not too bad with a minimum of 1dB.

Control

In order to control this board there are 2 control pins for the SP4T switch, but since this design doesn't require an all-on or all-off state we are able to ground the third voltage pin and only use 10 control pins for switching the SP4T; the logic voltages for this board are detailed in Table 3.12.

RF Switch	On	Off
SPDT	0V$\pm$0.3V	1.35V - 2.7V

Table 3.12: Logic Voltage Control

Therefore this the device can be controlled using a 4-bit number representing the current active switch for the input. Using the logic control table specified in Table 3.16 a logic table has been drawn to design a suitable method to control the SP16T switch with minimal amount of cabling and components required; the results can be seen in Appendix **??**.

State	V_1	V_2
RF4	Off	Off
RF1	Off	On
RF2	On	Off
RF3	On	On

Table 3.13: Logic Control Table for 'Design 3'

Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first two bits are connected to each of the cascaded SP4T switches and the last two bits are connected to the centre SP4T switch. Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first two bits are connected to each of the cascaded SP4T switches and the last two bits are connected to the centre SP4T switch.

3.2.5 Output 2

This design looks at constructing a SP16T RF switch using an similar design to Design 2, this utilises the PE42442 chip which is from the same family as the PE42441. Similar to the PE42441, the PE42442 is a SP4T RF switch that slightly varies in their specifications. The PE42442 provides a lower input power, but provides a slightly better insertion and isolation response in comparison to the PE42441. This allowed for a similar set-up for the board layout where the first SP4T switch leads to a second cascaded SP4T switch.

The device is able to be compacted into a smaller board due to the alternate arrangement of pins in comparison to Design 2; this new Altium design can be seen in Figure 3.7. The boards are arranged so that they are symmetrical down the centre, each chip is spaced to provide enough space for the logic control lines and V_{cc} to be able to be connected to the chip without running underneath any of the transmission lines. This required the two centre outputs from the first RF chip, IC2 and IC5, to be spaced 90^o apart from each other the two edge chips were then spaced 60^o away to provide enough room for the data lines to connect to the RF chips.

This design was developed in Altium Designer and can be seen in Figure 3.7.

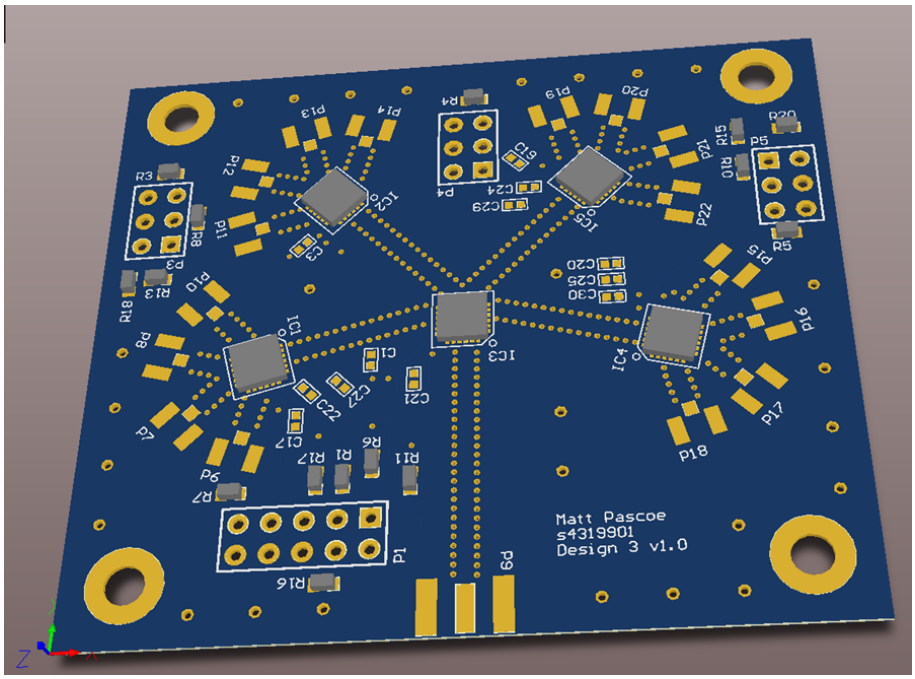

Figure 3.7: PCB Design for 'Design 3'

Specifications

Therefore using the SP4T switches cascaded together the performance of the switch can be estimate the parameters of the switch based off of the specifications presented in the PE42442's data-sheet; the estimated performance can be seen in Table 3.14.

Parameter	Value				
	100MHz	1GHz	2GHz	3GHz	4Ghz
Insertion Isolation Input Reflection Output Reflection Max. Switching Speed					

Table 3.14: Design 1 - Ideal parameters

It can be seen that the expected insertion loss is relatively low at a maximum of 1dB loss, the isolation is not too bad with a minimum of 1dB.

Control

In order to control this board there are 15 control pins for the SP4T switch, but since this design doesn't require an all-on or all-off state we are able to ground the

third voltage pin and only use 10 control pins for switching the SP4T; the logic voltages for this board are detailed in Table 3.15.

RF Switch	On	Off
SP4T	0V$\pm$0.3V	1.35V - 2.7V

Table 3.15: Logic Voltage Control

Therefore this the device can be controlled using a 4-bit number representing the current active switch for the input. Using the logic control table specified in Table 3.16 a logic table has been drawn to design a suitable method to control the SP16T switch with minimal amount of cabling and components required; the results can be seen in Appendix **??**.

State	V_1	V_2
RF4	Off	Off
RF1	Off	On
RF2	On	Off
RF3	On	On

Table 3.16: Logic Control Table for 'Design 3'

Therefore this design can be easily controlled using the output logic from the micro-controller where the output signal is 4-bits, the first two bits are connected to each of the cascaded SP4T switches and the last two bits are connected to the centre SP4T switch.

3.3 Development

This section of the report looks at the construction and development of the PCB boards and

3.3.1 PCB Development

After the design of the PCB had been completed the order was processed by a PCB development company. During this project two companies were used: PCBZone and PCBWay. The key difference between these companies was price, quantity and quality;

Once the PCB's and components arrived they were soldered and constructed to be fully tested and analysed in Section 4; the constructed boards can be seen from Figure 3.8 - 3.13.

Figure 3.8: PCB Construction of 'Design 1'

Figure 3.9: PCB Construction of 'Design 2'

Figure 3.10: PCB Construction of 'Design 3'

Figure 3.11: PCB Construction of 'Output 1'

Figure 3.12: PCB Construction of 'Output 1 - Large'

Figure 3.13: PCB Construction of 'Output 2'

These boards will be used to evaluate the functionality of the SSR's as high-speed RF switches as well as for the construction of the RF Switch Matrix.

3.4 Physical Construction

This section of the report looks at the construction of the housing for the RF Switch Matrix, the case should be:

- Cheap, light-weight and ....
- Material is conductive to provide RF shielding
- Able to be cut and reshaped

3.4.1 Case Design

The case was constructed from a 0.5 mmthick aluminium sheet to provide a RF shielding case to reduce the amount of RF signals from entering or leaving the switch matrix and causing interference to the RF equipment being attached to the switch matrix.

Using the requirements previously stated a suitable design for the case was developed which would provide a tight fit for the PCB's as well as the micro-controller designed in Section 3.5. The schematics for the case can be seen in Figure 3.14.

Figure 3.14: Schematics for Case Design

Using the drawing from Figure 3.14 the case was constructed using tin-snips to cut the aluminium sheeting into the two separate ....., since the aluminium was light it was able to folded over a block of wood to obtain the 90^o bends. A template was designed to ensure that the 4×4 grid of SMA connectors would be able to fit onto a cardboard template to ensure that the design was suitable and transferred to the final aluminium sheet; power-tools were used to drill the holes for the switches, SMA connectors and USB Type-B connector. The final construction was tested to ensure that all the board would fit into the case; 1 cmnylon spacers were used to stand the boards apart from eachother. The final design of the case can be seen in Figure 3.15.

Figure 3.15: RF Switch Matrix Case

3.5 Micro-controller Development

In order to control and operate the RF Switch system a some type of micro-controller is required to be used to switch the inputs and outputs of the system. The micro-controller needs to meet the following key design parameters:

- Capable of supporting .... control pins.
- Enable a switch speed of 100 ns
- Low power requirements, less than 5 W
- Source power from USB, and communicate using 15260 Baud rate.
- Capability to sync other controllers,

The ideal device is a low-powered micro-controller, for this project the PSOC4-BLE has been selected to ensure that it is able to control the

3.5.1 Design

In order to control the PSOC4-BLE code was written to control the RF Switch matrix, a flow-chart was developed to initialise the development of the micro-controller; the flowchart for the micro-controller can be seen in Figure 3.16.

Figure 3.16: Micro-controller Flowchart

For each development board a logic table was developed, these logic tables can be seen in Appendix D which were developed for each board; these table determines the logic required to ensure that the number of control pins to a minimum.

3.5.2 Components

In order to control all of the RF switches we need utilise all of the GPIO pins on the PSOC micro-controller; to control both SP16T RF switches we require atleast 8 GPIO pins, and 16 GPIO pins for each SPDT switch. To make the micro-controller more functional a feature to control the switch matrix with an external controller was included, this requires 8 GPIO pins to read the data in as well as a clock pin to latch the data through the system as well as a pin to toggle between the micro-controller code and user input data. Two GPIO pins were are required for T_x and R_x for UART communications so that the user is able to control the speed and active pins of the switch matrix.

In order to achieve this two $1-8$ multiplexers were used, this allows for 8 unique paths for a single voltage which is suitable for the SPDT switches. Therefore using two $1-8$ multiplexers the 16 SPDT can be controlled by 8 GPIO pins instead of 16. For powering and communicating with the micro-controller a USB Tpye-B port was used, this was connected to a USB-Serial converter to provide UART communication between a computer and the micro-controller as well as a voltage supply.

Therefore the block diagram for the controller can be developed which can be seen in Figure 3.17.

Figure 3.17: Micro-controller Block Diagram

3.5.3 Evaluation

Chapter 4

Verification

4.1 Individual Board's

This section looks at the results obtain from each of the individual boards, each board was tested with a Anritsu MS46322A VNA. By evaluating these boards it can be determined which is most suited for the final design of the RF switch matrix; Section 4.1.1 - 4.1.5 details the analysed results and discuses the benefits and disadvantages of that design.

4.1.1 Design 1

The design for 'Design 1' which was designed in Section 3.2.1 was constructed and developed according to the design. This section looks at analysing the SP16T RF switch developed to determine the losses, speed and power requirements of the design and comparing them against the specifications detailed in the RF switches data-sheet.
A Anritsu MS46322A VNA is used to analyse the SP16T; this is used to determine the losses of the system, the micro-controller is used to increment the switch speed of the device to determine the frequency where the SP16T is unable to maintain the losses seen in the previous section. Finally the

Losses

Design 1 has been tested with a VNA to obtain 3 different results for the device which shows an open transmission line seen in Figure 4.1. Additional tests were conducted to determine the effects of the SP16T when one or all of the switches are closed to determine the internal reflections of the device; these results can be seen in Figure 4.2 - 4.8.

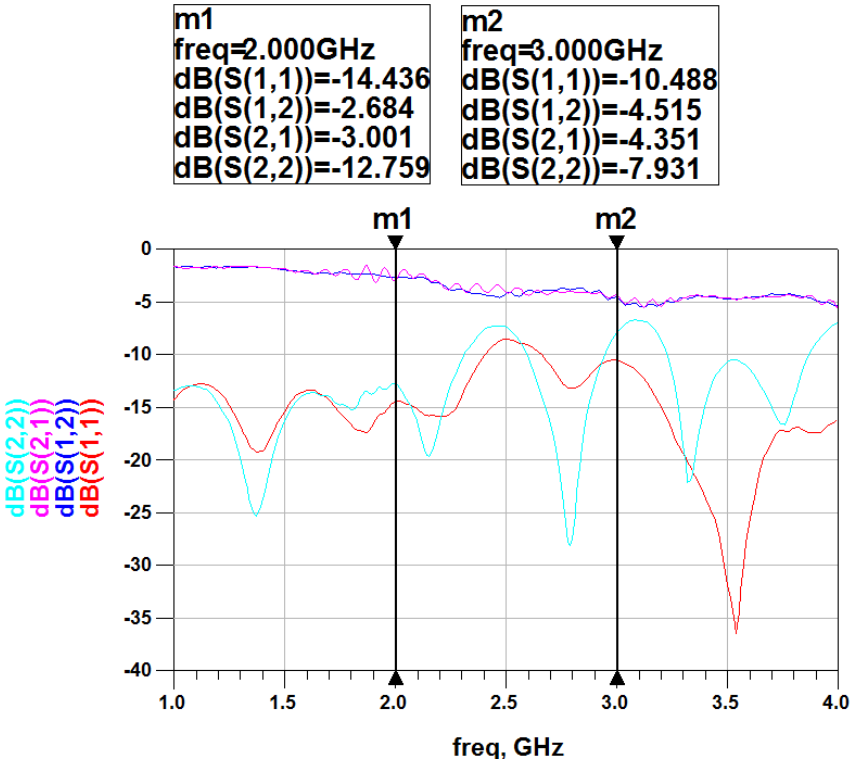

Figure 4.1: Design 1 S-Parameters - Insertion Loss

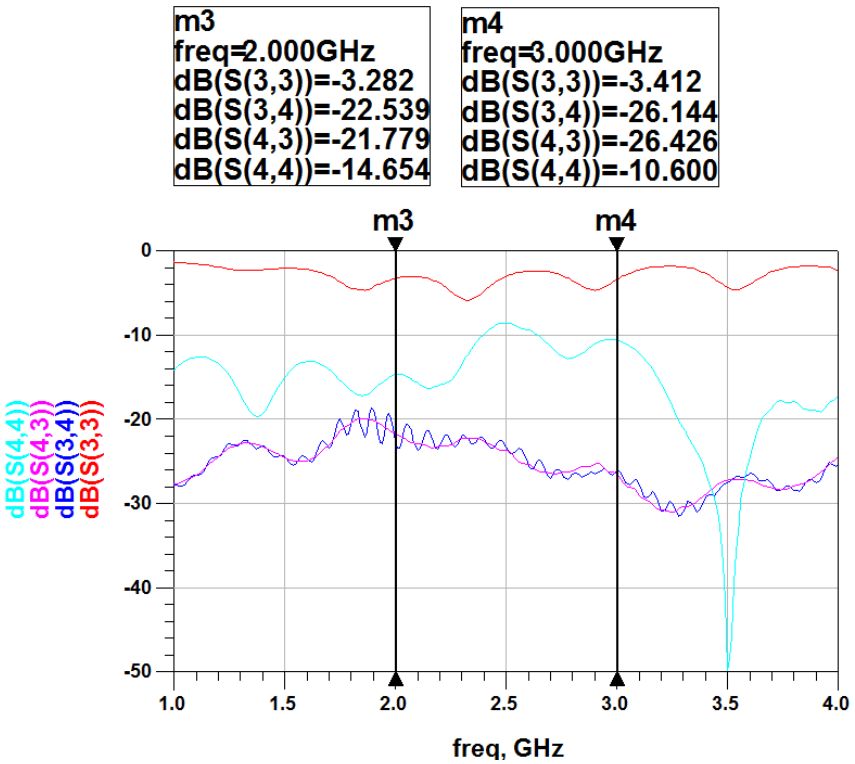

Figure 4.2: Design 1 S-Parameters - Isolation (Best case)

Figure 4.3: Design 1 S-Parameters - Isolation (Worst case)

It can be seen looking at the results that the results obtained in Figure **??**

Comparison

4.1.2 Design 2

The design for 'Design 2' which was completed in Section 3.2.2 was constructed and developed according to the design. This section looks at analysing the SP16T RF switch developed to determine the losses, operation requirements of this design against the specifications detailed in the RF switches data-sheets.

It was found that this board was not functioning, after wiring the board upto the micro-controller it was found that the changing the logic on the centre PE42441 chip didn't make a significant change to the insertion of the board. Whereas changing the logic on the second PE42441 chip cascaded had a small change on the insertion loss of the device; this change can be seen in Figure 4.4 and 4.5.

Figure 4.4: Design 2 S-Parameters - Insertion (Best case)

Figure 4.5: Design 2 S-Parameters - Insertion (Worst case)

Therefore it can be seen that there is an issue within the first chip, this issue is likely due to an issue from soldering.

Therefore, due to time constraints of the thesis this design was terminated as the design expectations from Section 3.2.2 had poorer insertion losses than the 'Design 1' or 'Design 3' so under the allocated budget was not worth further investigating.

4.1.3 Design 3

The design for 'Design 3' which was designed in Section 3.2.3 was constructed and developed according to the design. This section looks at analysing the SP16T RF switch developed to determine the losses, speed and power requirements of the design and comparing them against the specifications detailed in the RF switches data-sheet.

A Anritsu MS46322A VNA is used to analyse the SP16T; this is used to determine the losses of the system, the micro-controller is used to increment the switch speed of the device to determine the frequency where the SP16T is unable to maintain the losses seen in the previous section. Finally the

Losses

Design 3 has been tested with a VNA to obtain 3 different results for the device which shows an open transmission line seen in Figure 4.6. Additional tests were conducted to determine the effects of the SP16T when one or all of the switches are closed to determine the internal reflections of the device; these results can be seen in Figure 4.7 - ??.

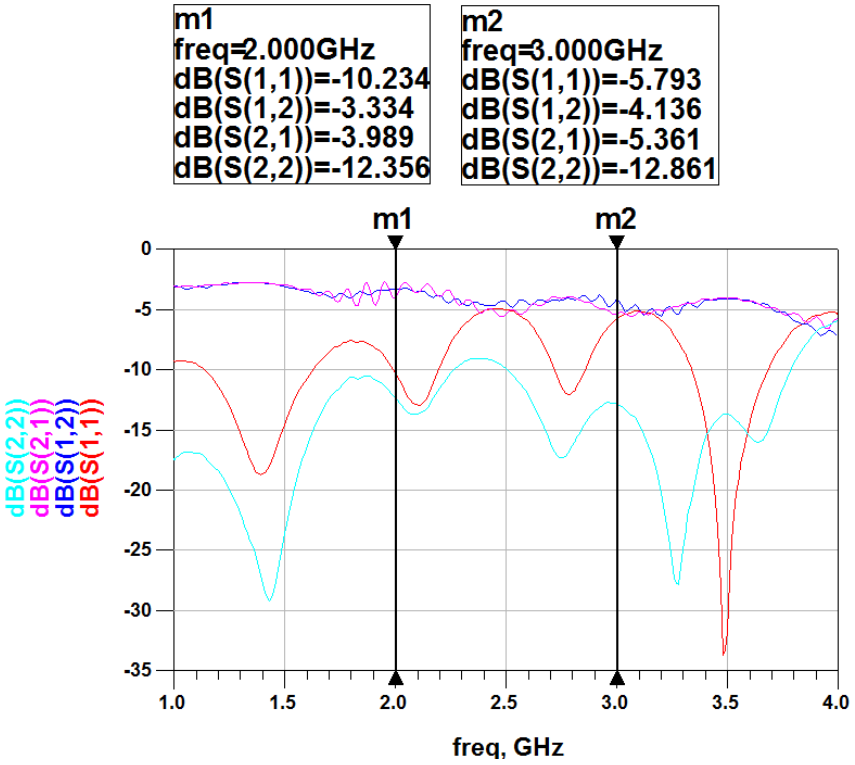

Figure 4.6: Design 1 S-Parameters - Insertion Loss

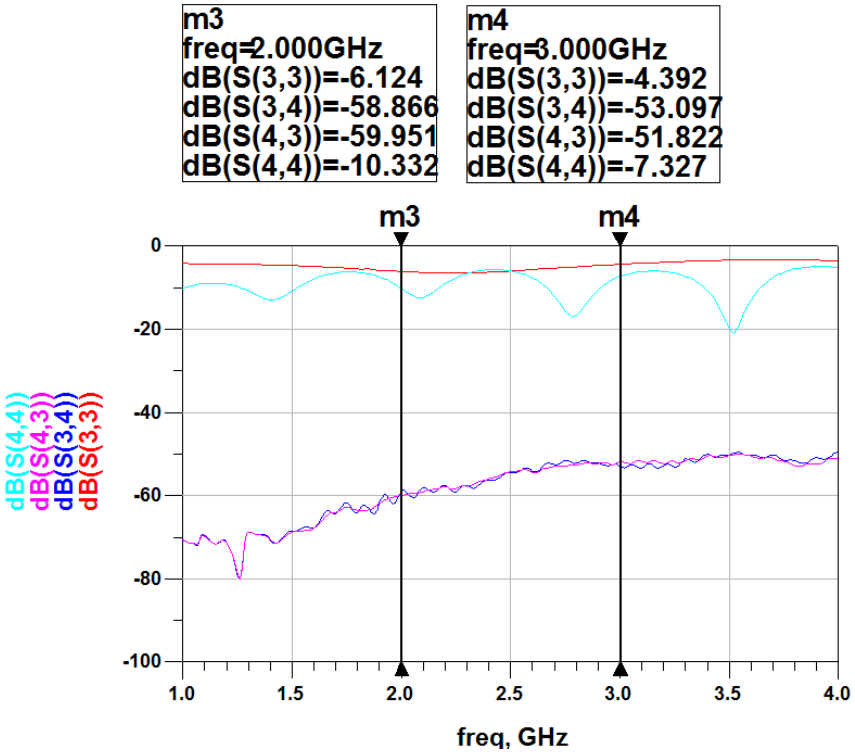

Figure 4.7: Design 1 S-Parameters - Isolation (Best case)

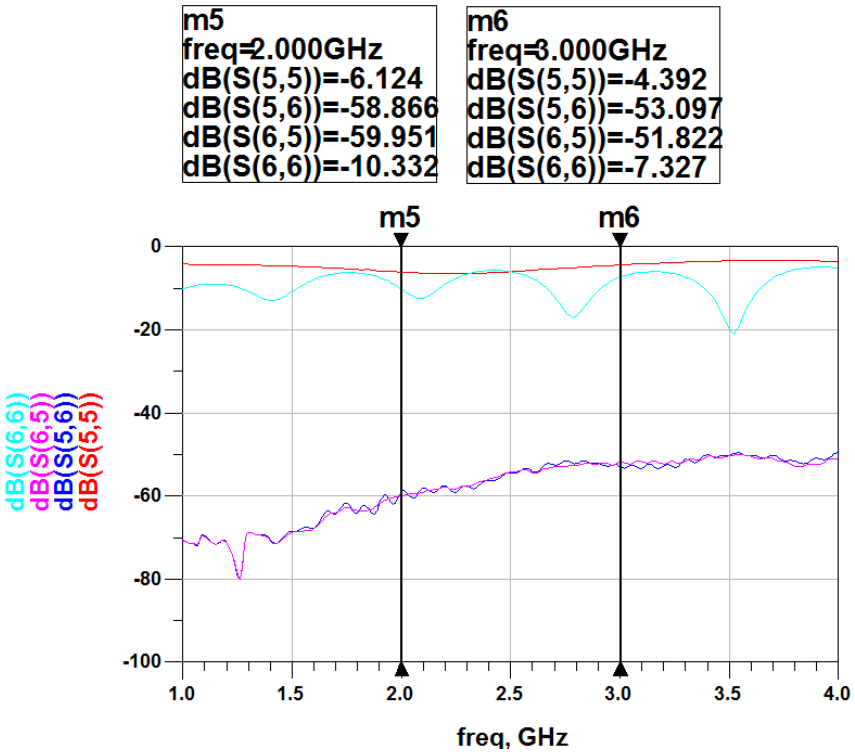

Figure 4.8: Design 1 S-Parameters - Isolation (Worst case)

Switch Speed

Power Requirements

4.1.4 Output 1

Output 1 has been tested with a VNA, there are 3 different characteristics that are key to the analysis of the SP16T RF switch: losses, speed and power.

Losses

Figure 4.9: Output 1 S-Parameters

Switch Speed

Power Requirements

4.1.5 Output 2

The design for 'Output 2' seen in Section 3.2.5 was developed and tested using a VNA; it was found that the design wasn't operating. So due to time constraints, since the RF chip was not functioning it was decided to disregard this design as it would be too expensive and time consuming to re-design & develop this design.

4.1.6 Cabling

There are several different cabling options available; three different cabling options have been looked at, this includes flexible and rigid SMA cables, and UFL cabling. Looking at Figure 4.10 - 4.13 we can determine the effects of cabling in the final design.

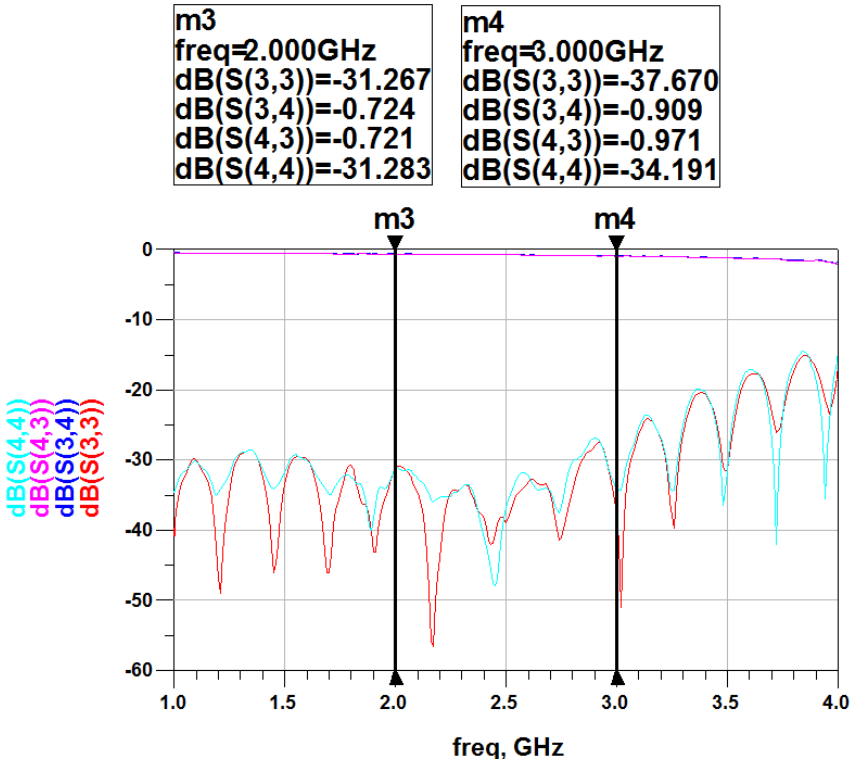

Figure 4.10: Flexable 0.5m SMA cable S-Parameters

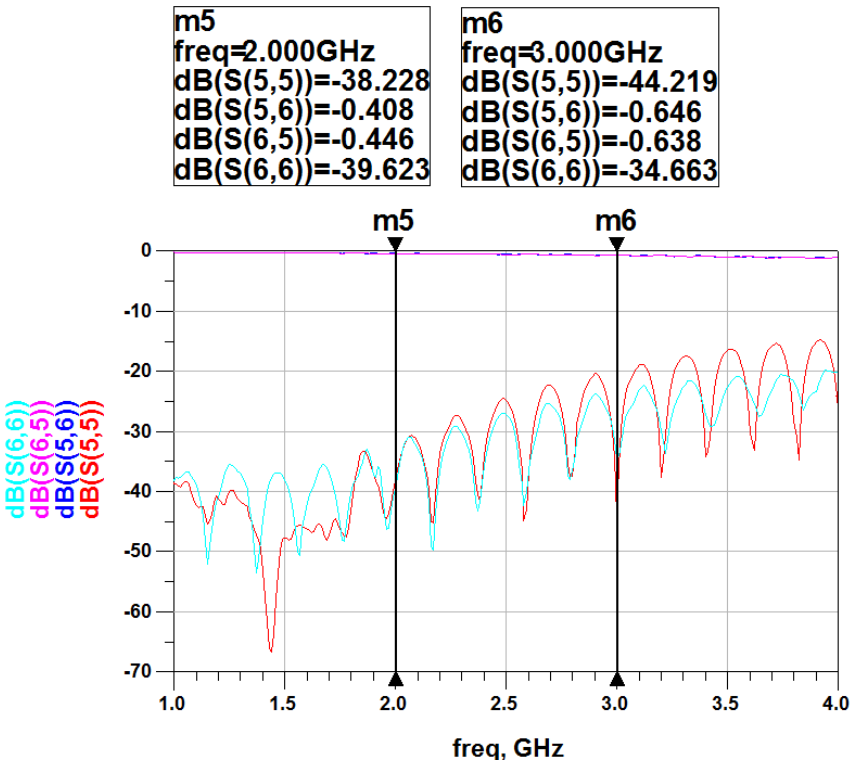

Figure 4.11: Rigid 0.5m SMA cable S-Parameters

It can be seen that more rigid cable has a far better response for insertion,

although both these cables are particularly bulky in their size.

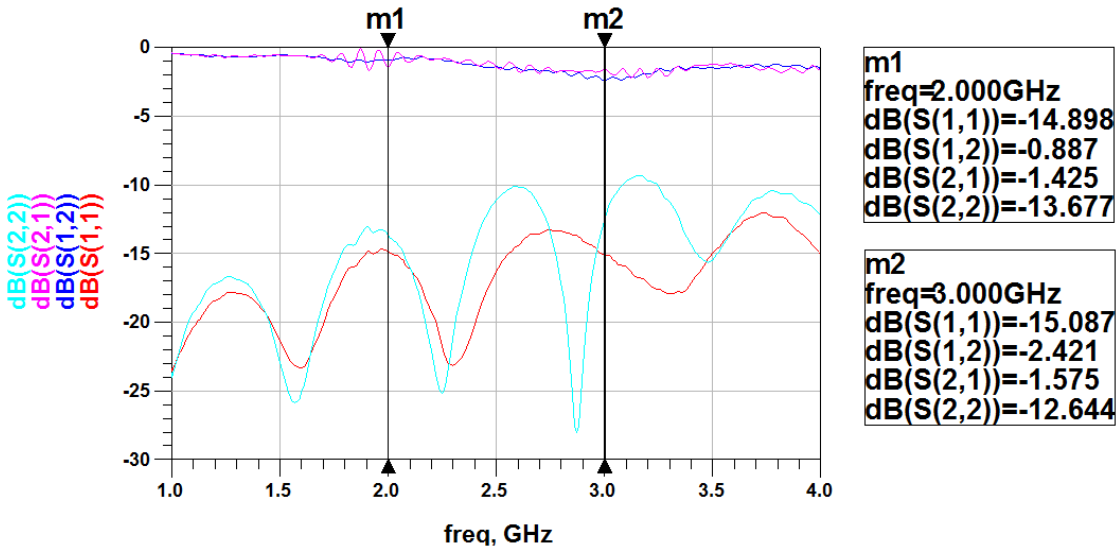

Figure 4.12: 0.5m UFL cable S-Parameters

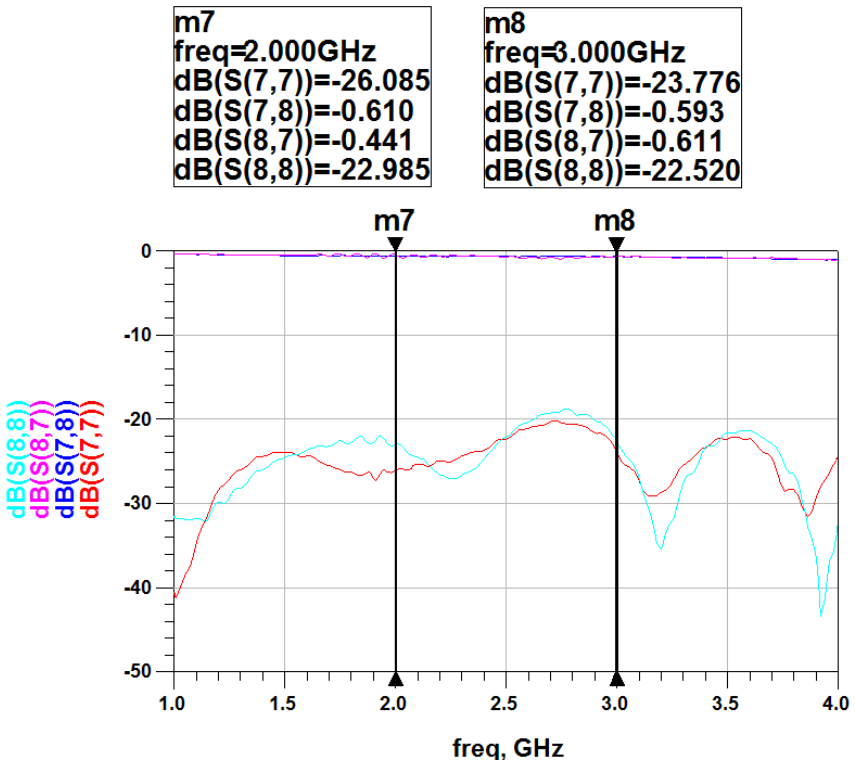

Figure 4.13: 0.5m UFL cable S-Parameters

It can be seen that there is a larger loss from the UFL cable seen in Figure 4.13 in comparison to the SMA cabling seen in Figure 4.10 and 4.11. It has been decided that the design would suffer this loss in order to allow for a more flexible cabling method allowing for a device which is significantly more portable and smaller.

An issue was found that can be seen in Figure 4.12, this is a UFL connector that has been connected and disconnected multiple times; UFL cabling is commonly designed for less than 20 mating's. A new UFL cable was tested which can be seen in Figure 4.13, giving a significantly better response for insertion and reflection.

4.2 RF Switch Matrix

This section looks at the overall characteristics of the final RF switch matrix design. To determine the overall performance of the system, this required evaluating the performance, speed, size and power constraints.

4.2.1 Final Design

From looking at the results obtained in Section 4.1 it can be seen that the only option for the output SPDT switch is 'Output 1'. Therefore the 16 output terminals will have the reflection seen in Figure 4.9 S_{22} signal, this will be connected to the SP16T via a UFL-UFL connector seen in Figure 4.13.
Looking at the results obtained, it can be seen that 'Design ...' has an insertion loss of ...dB

Therefore the final design will use 'Design ...' and 'Output 1'.

4.2.2 Analysis

Losses

In order to determine the characteristics of the designed RF switch matrix, its characteristics of can be modelled using S-Parameters to evaluate the final design. Using the Anritsu MS46322A VNA the switch matrix was analysed to determine the amount of losses that are present in the system.
Looking at Figure **??** we can determine the performance of the overall system. There are multiple paths that need to be considered in order to fully evaluate the RF switch, there are 9 different paths that can be taken; these can be seen below in Figure 4.14 - **??**.

Figure 4.14: S-Parameters of RF switch matrix
Insertion Loss

Figure 4.15: S-Parameters of RF switch matrix
Isolation (Best case)

Figure 4.16: S-Parameters of RF switch matrix
Isolation (Worst case)

Speed

We know from Section 3.5 that micro-controller is capable of controlling the switches at 1500 μs, but the SSR's are capable of operating above this speed. Therefore the maximum switching frequency needs to be determined for this RF switch.
Using the specifications from the datasheets, it can be said that the maximum switching speed for the switch matrix is 150 μs. The 150 μsis determined by the slowest chip in this system which bottlenecks the maximum switching speed of the overall performance of the switch matrix. Therefore we can say that theoretical switching speed is limited to .... μs.

With the fully developed RF switch matrix it can be fully evaluated to determine its performance in regard to speed; as can be seen in Figure 5.1 the switch matrix is wired so that one input and output are connected to the VNA.

Figure 4.17: Speed test set-up for RF Switch Matrix

Using the set-up shown in Figure 5.1 the VNA monitor's the signal strength to determine the speed which causes the insertion loss to drop bellow the level seen in Figure 4.14. By doing this it was determined that the maximum switching speed of the micro-controller is ... μs, which is close to the expected limitation of the ..... RF chip.

Power Requirements & Control

Size Requirements

Chapter 5

Discussion

5.1 Problems

It was seen that there was a poor reflection in the results from Design 1, Design 3, Output 1 and the final switch matrix; a cause of this poor result is was identified when analysing the cabling in Section 4.1.6.

5.1.1 Converting 'Design 1' to a Non-Reflective Switch

5.1.2 Impedance Mismatch

It can be seen looking at the results obtained for the RF Switch Matrix in Figure **??** that there are significant reflections on $S_{(1,1)}$ and $S_{(2,2)}$. After reviewing the design of the RF switches, PCB design's and equipment used to analyse and measure the RF switches, upon further inspection of the RF tracks it can be seen in Figure **??** that there are two different mismatches that occur in the circuit.

Figure 5.1: Speed test set-up for RF Switch Matrix

The first input/output of each PCB has a small change in width, which causes a small impedance change; the effects of this impedance change can be visualised in Figure 5.2. The second mismatch is at the input/output of the RF chip; in order to connect the transmission line to the RF chip it must change from length to a more suitable size to connect all of the pins. This mismatch can be seen in Figure 5.3, this width change is unavoidable and need to step down; this can be rectified by adding an impedance transformer to the input/output.

Simulations

To determine the effect of the impedance mismatch ADS was used to simulate the impedance mismatch for both types previously discussed. These simulations can be seen in Figure 5.2 & 5.3.

Figure 5.2: Impedance Mismatch on SMA/UFL

Figure 5.3: Impedance Mismatch on RF Chip

Resolving Impedance Mismatch

The effects of the mismatch for the input/output are minimal and can be easily rectified on a second PCB order, whereas the mismatch due to RF chips require additional design requirements. Using the code provided in Appendix **??** we are able to construct a Chebychev transformer that can reduce the losses in the RF board; a Chebychev transformer was selected since it provides a wide frequency match as opposed to a Binomial transformer. The MATLAB code provided calculates the changes in impedance for the transmission line. LineCalc was used afterwards to determine the new transmission line design, using this new design a new simulation was run the determine the new losses of the tracks; this can be seen in Figure 5.4.

Figure 5.4: Impedance Mismatch on RF Chip

5.1.3 Removing Mismatch Losses from RF Switch Matrix

Using the results obtained in Section 5.1.2 simulations were found which described the losses from the mismatch it was investigated as to how the system would perform with the recommendations in-place. Instead of reconstructing the PCB's this section looks at de-embeding the S-parameters obtained in the previous simulations from the measured results from the VNA. This is done using the code in Appendix **??** which takes a selected input for the previous losses, new losses and the overall system losses and then performs a series of calculations previously discussed in Section **??**. This script returns two plots, the first is the result without any losses due to tracks which should be approximate to the specifications given in the data-sheets and Section 3.2

5.1.4 Resource Availability

5.2 Removing Losses from VNA Results

Since the loss due to the mismatch discussed in Section 5.1.2 can be simulated in ADS as seen in Figure **??** we are able to write MATLAB code given in Section **??**. This MATLAB code de-embeds the S-Parameters of the RF chips from the mismatch caused by the micro-strip track; this result is plotted to estimate the ideal insertion loss and reflection of the switch matrix without the impedance mismatch.

Figure 5.5: Ideal S-Parameters of Switch Matrix

Therefore it can be seen comparing the results in Figure 5.5 against the analysed results in Figure **??** has improved as the frequency increases. It should be noted that this is not the actual frequency response of a corrected PCB; using ADS a new simulation can be computed to simulated the new loss due to the transmission lines. By adding the S-Parameters of a corrected board without

Figure 5.6: Corrected S-Parameters of Switch Matrix

Figure 5.7: Corrected S-Parameters of Switch Matrix

5.3 Objective Fulfilment

This section of the report looks at the

5.3.1 Comparison to Available Technology

To evaluate the performance of the RF Switch matrix it was compared against two different types of RF Switch Matrix's. The RF switch matrix's that will be looked at are the:

- 1
- 2

5.4 Contributions

This thesis has provided a

Chapter 6

Conclusions and Future Work

6.1 Conclusion

6.2 Future Work

Appendix A

PCB Design

A.1 Design 1

A.2 Design 2

A.3 Design 3

A.4 Output Design 1

A.5 Output Design 2

A.6 Output Design 3

Appendix B

Substrate Parameters

The following tables contain the parameters and details for the substrates investigated in this thesis.

Substrate	Parameter	Value
FR-4	Er	4.7
	Mur	1
	H	even
Epoxy	Er	4.7
	Mur	1
	H	even

Table B.1: *Parameters for simulation of PCB substrate's*

Appendix C

Bill of Materials

In order to construct the design of the Switching Matrix we require the following components, a Bill of Materials has been constructed and can be seen in Table C.1.

Name	Description	Digikey Part no.	Min Order no.	Price	Quantity	Total

Total:	$100

Table C.1: *Bill of Materials*

Appendix D

RF Switch Controls

D.1 Design 1

Table D.1: 'Design 1' Logic Control Table

Input				**Output**																		
				$SPDT_1$		$SPDT_2$		$SPDT_3$		$SPDT_4$		$SPDT_5$		$SPDT_6$		$SPDT_7$		$SPDT_8$		$SP8T$		
x_3	x_2	x_1	x_0	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V1**	**V2**	**V3**
0	0	0	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	0	0	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	0	1	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	0	1	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	1	0	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	1	0	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	1	1	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
0	1	1	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	0	0	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	0	0	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	0	1	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	0	1	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	1	0	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	1	0	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	1	1	0	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3
1	1	1	1	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_0	$\bar{x_0}$	x_1	x_2	x_3

D.1.1 Design 2

D.1.2 Design 3

D.1.3 Output 1

D.1.4 Output 2

Appendix E

Companion disk

If you wish to make some computer files available to your examiners, you can list and describe the files here. The files can be supplied on a disk and inserted in a pocket fixed to the inside back cover.

The disk will not be needed if you can specify a URL from which the files can be downloaded.

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