THE UNIVERSITY OF QUEENSLAND

AUSTRALIA

FPGA Web Interface and Ethernet Network Controller using the RISC-V Processor

Project Proposal

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List of Abbreviations

Abbreviations	
MAC	Medium Access Control
ISA	Instruction Set Architecture
etc.	*etc.*

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Topic

The proposed thesis project

The IEEE 802.3 standard [1], more commonly known by the name of 'Ethernet' defines the *'Medium Access Control'* (MAC) protocol amongst other things for two or more devices to communicate over a network. This standard is just one part in the layered network models such as the OSI model and TCP/IP models.

RISC-V, a reduced instruction set computer architecture, is an open and royalty free instruction set architecture (ISA)

Chapter 2

Background

Introduce the broad layout of the chapter.

2.1 Introduction

Add your text here.

Chapter 3

Conclusion

Conclude your thesis.

Bibliography

[1] “IEEE Standard for Ethernet,” standard, The Institute of Electrical and Electronics Engineers, Inc., New York, USA, Dec. 2012.

Appendix A

Appendix

Write your appendix here. Following two are examples.

A.1 Name of Appendix-1

A.2 Name of Appendix-2