



THE UNIVERSITY OF QUEENSLAND  
AUSTRALIA

# **FPGA Web Interface and Ethernet Network Controller using the RISC-V Processor**

## *Project Proposal*

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Semester 1, 2023

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# Chapter 1

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## Introduction

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### 1.1 Your thesis topic

Introduce your topic. [1]

## Chapter 2

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# Background

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Introduce the broad layout of the chapter.

### 2.1 Introduction

Add your text here.

## **Chapter 3**

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## **Conclusion**

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Conclude your thesis.

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# Bibliography

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- [1] “IEEE Standard for Ethernet,” standard, The Institute of Electrical and Electronics Engineers, Inc., New York, USA, Dec. 2012.

## **Appendix A**

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## **Appendix**

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Write your appendix here. Following two are examples.

### **A.1 Name of Appendix-1**

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