



THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

FPGA Web Interface and Ethernet Network Controller using the RISC-V Processor

Project Proposal

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Chapter 1

Introduction

1.1 Your thesis topic

Introduce your topic.

Chapter 2

Background

Introduce the broad layout of the chapter.

2.1 Introduction

Add your text here.

Chapter 3

Conclusion

Conclude your thesis.

Bibliography

Appendix A

Appendix

Write your appendix here. Following two are examples.

A.1 Name of Appendix-1

A.2 Name of Appendix-2