Progress Seminar

An automated triple modular redundancy EDA flow for Yosys

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16 September 2024

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Background

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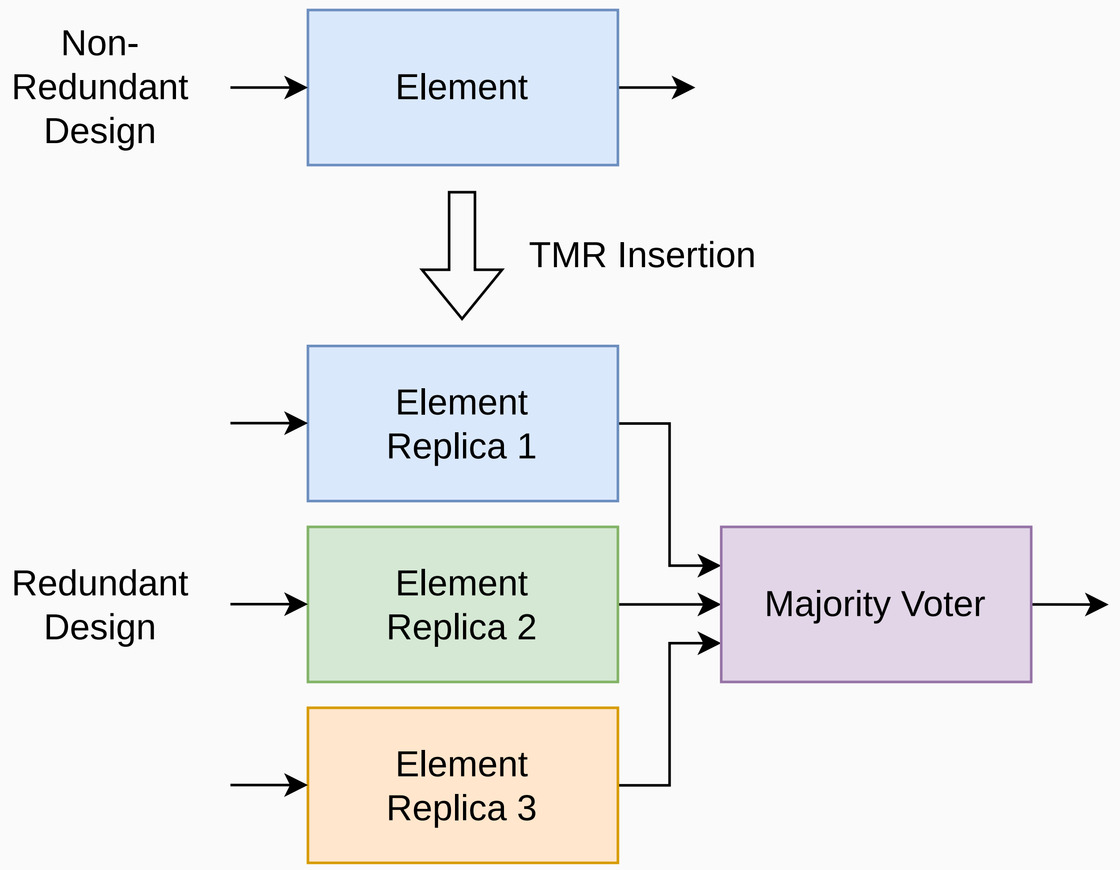
ASICs and FPGAs commonly deployed in space (and on Earth)... but protection from SEUs remains expensive!

RAD750 CPU [1] is commonly used, but costs >$200,000 USD [2]!

Triple Modular Redundancy



Triple Modular Redundancy

TMR can be added manually...

but this is **time consuming** and **error prone**.

Can we automate it?

TaMaRa

Concept

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I introduce *TaMaRa*: An automated triple modular redundancy EDA flow *for Yosys*

Existing works

Two main paradigms:

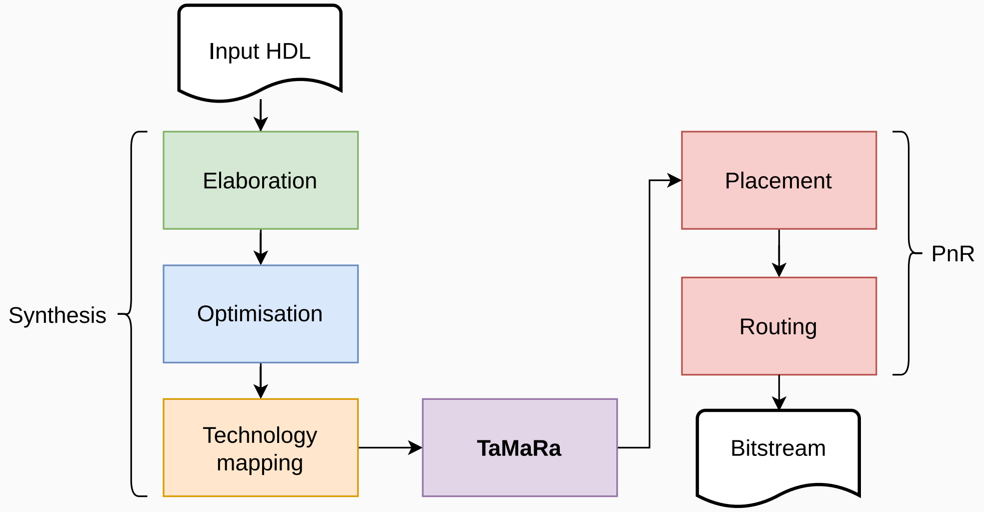
- **Design-level approaches** (“thinking in terms of HDL”)
  - Kulis [4], Lee [5]
- **Netlist-level approaches** (“thinking in terms of circuits”)
  - Johnson [6], Benites [7], Skouson [8]

The TaMaRa algorithm

TaMaRa will mainly be netlist-driven, using Johnson's [6] (TODO NOT TRUE) voter insertion algorithm.

Also aim to propagate a `(* triplicate *)` HDL annotation to select TMR granularity (similar to Kulis [4]).

Runs after techmapping (i.e. after `abc` in Yosys)



The TaMaRa algorithm

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Why netlist driven with the `(* triplicate *)` annotation?

- Removes the possibility of Yosys optimisation eliminating redundant TMR logic
- Removes the necessity of complex blackboxing logic and trickery to bypass the normal design flow
- Cell type shouldn't matter, TaMaRa targets FPGAs and ASICs
- Still allows selecting TMR granularity - **best of both worlds**

Verification

Comprehensive verification procedure using formal methods, simulation and fuzzing.

Driven by SymbiYosys tools *eqy* and *mcy*

- In turn driven by theorem provers/SAT solvers

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Also considering Beltrame's verification tool [9], and other literature on TMR formal verification.

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Idea:

1. Use Verismith [10] to generate random Verilog RTL.
2. Run TaMaRa synthesis end-to-end.
3. Use formal equivalence checking to verify the random circuits behave the same before/after TMR.

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Problem: Mutation

- We need valid testbenches for these random circuits, how would we generate that?
- Under active research in academia (may not be possible at the moment)

Simulation

We want to simulate an SEU environment.

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Use one of Verilator, Icarus Verilog or Yosys’ own cxxrtl to simulate a full design.

- Each simulator has different trade-offs
- Currently considering picorv32 or Hazard3 as the DUT
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Concept:

- Iterate over the netlist, randomly consider flipping a bit every cycle
- Write a self-checking testbench and ensure that the DUT responds correctly

Technical implementation

Implemented in C++20, using CMake.

Load into Yosys: `plugin -i libtamara.so`

TMR is implemented as two separate commands: `tamara_propagate` and `tamara_tmr`

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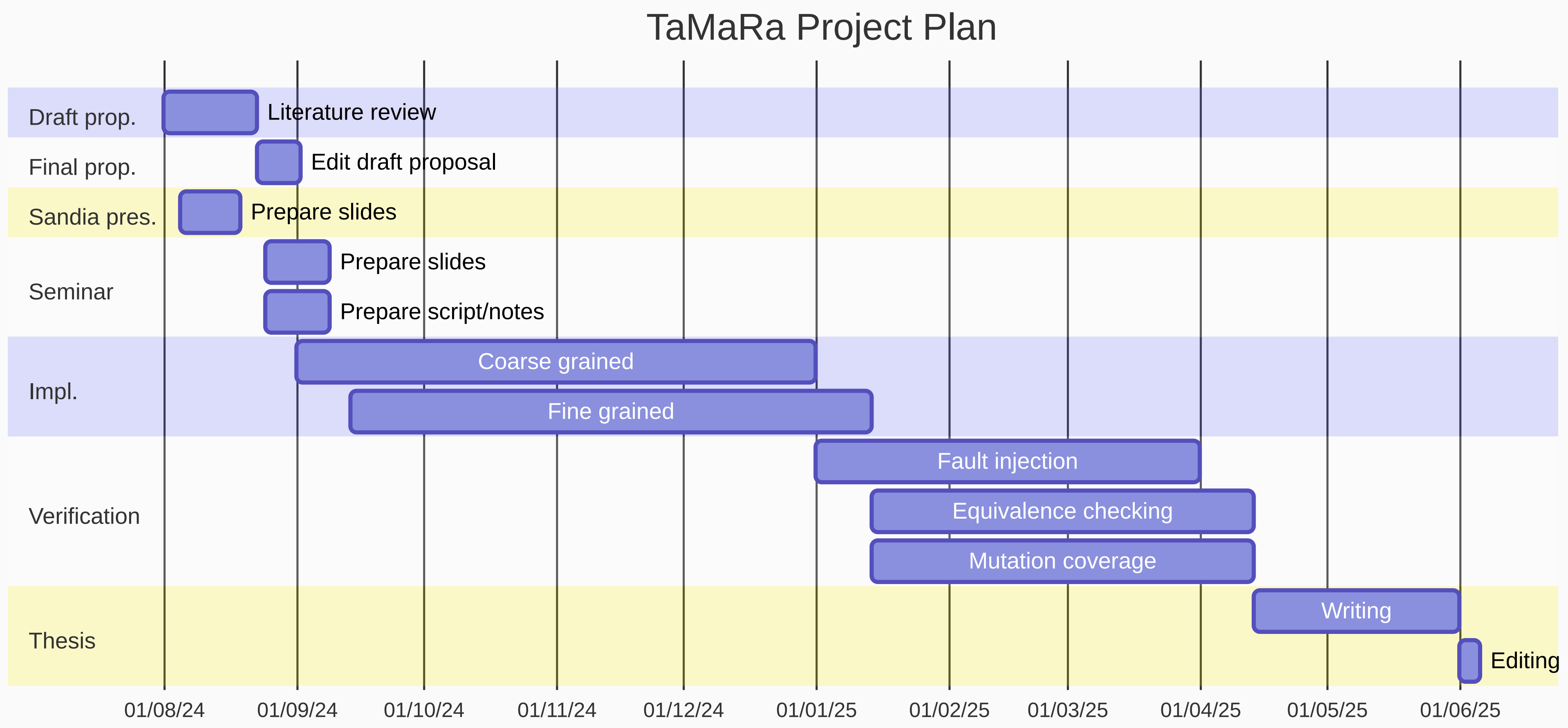
Run `tamara_tmr` after techmapping to perform triplication and voter insertion (add TMR).

Current status & future

Current status

TODO

The future



TaMaRa Project Plan
Draft prop.
Literature review
Final prop.
Edit draft proposal
Sandia pres.
Prepare slides
Seminar
Prepare slides
Prepare script/notes
Impl.
Coarse grained
Fine grained
Verification
Fault injection
Equivalence checking
Mutation coverage
Thesis
Writing
Editing
01/08/24
01/09/24
01/10/24
01/11/24
01/12/24
01/01/25
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01/06/25

The future

Programming hopefully finished *around* February 2025, verification by April 2025.

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Ideally, TaMaRa will be released open-source under MPL 2.0.

- Pending university IP shenanigans...

Conclusion

Summary

- TaMaRa: Automated triple modular redundancy EDA flow for Yosys
- Fully integrated into Yosys suite
- Takes any circuit, helps to prevent it from experiencing SEUs by adding TMR
- Netlist-driven algorithm based on Johnson's work [6] (TODO NOT TRUE)
- **Key goal:** "Click a button" and have any circuit run in space/in high reliability environments!

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Thank you! Any questions?