Progress Seminar
An automated triple modular redundancy EDA flow for Yosys

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Supervisor: Assoc. Prof. John Williams
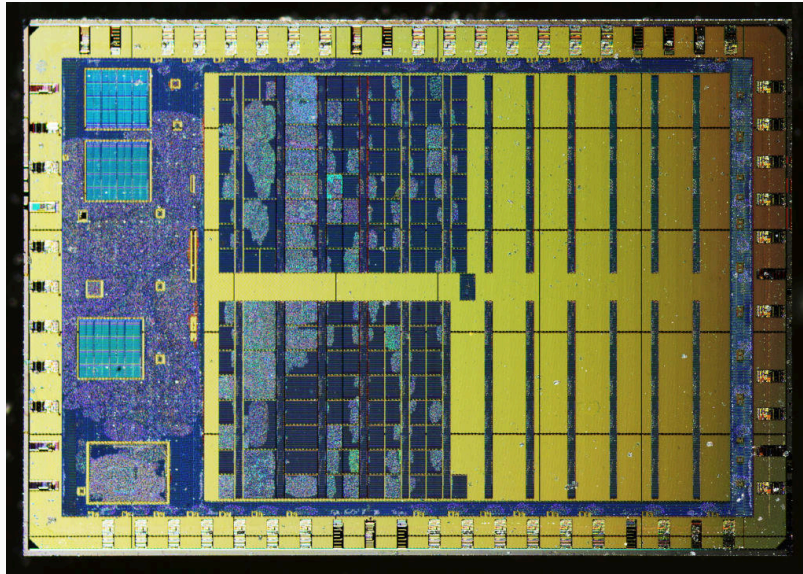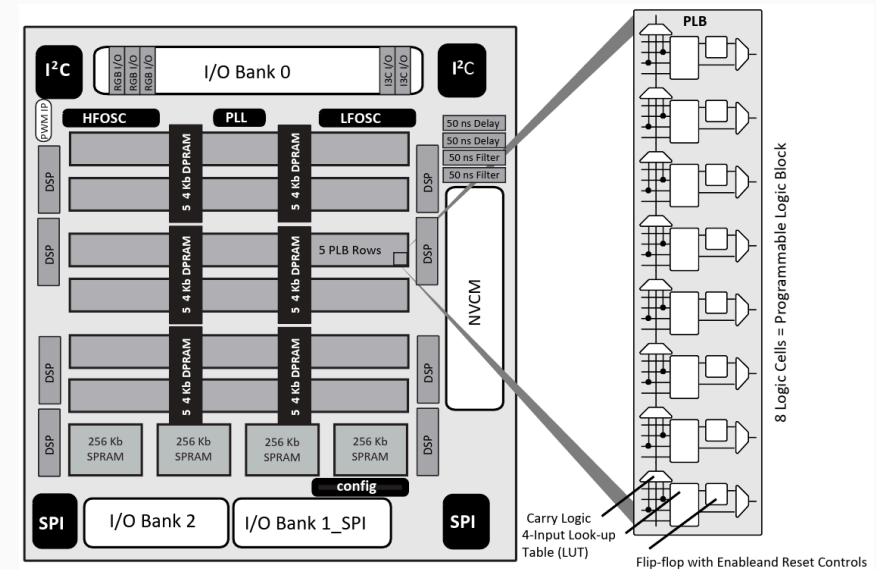
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Background

Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) commonly deployed in space (and on Earth)...

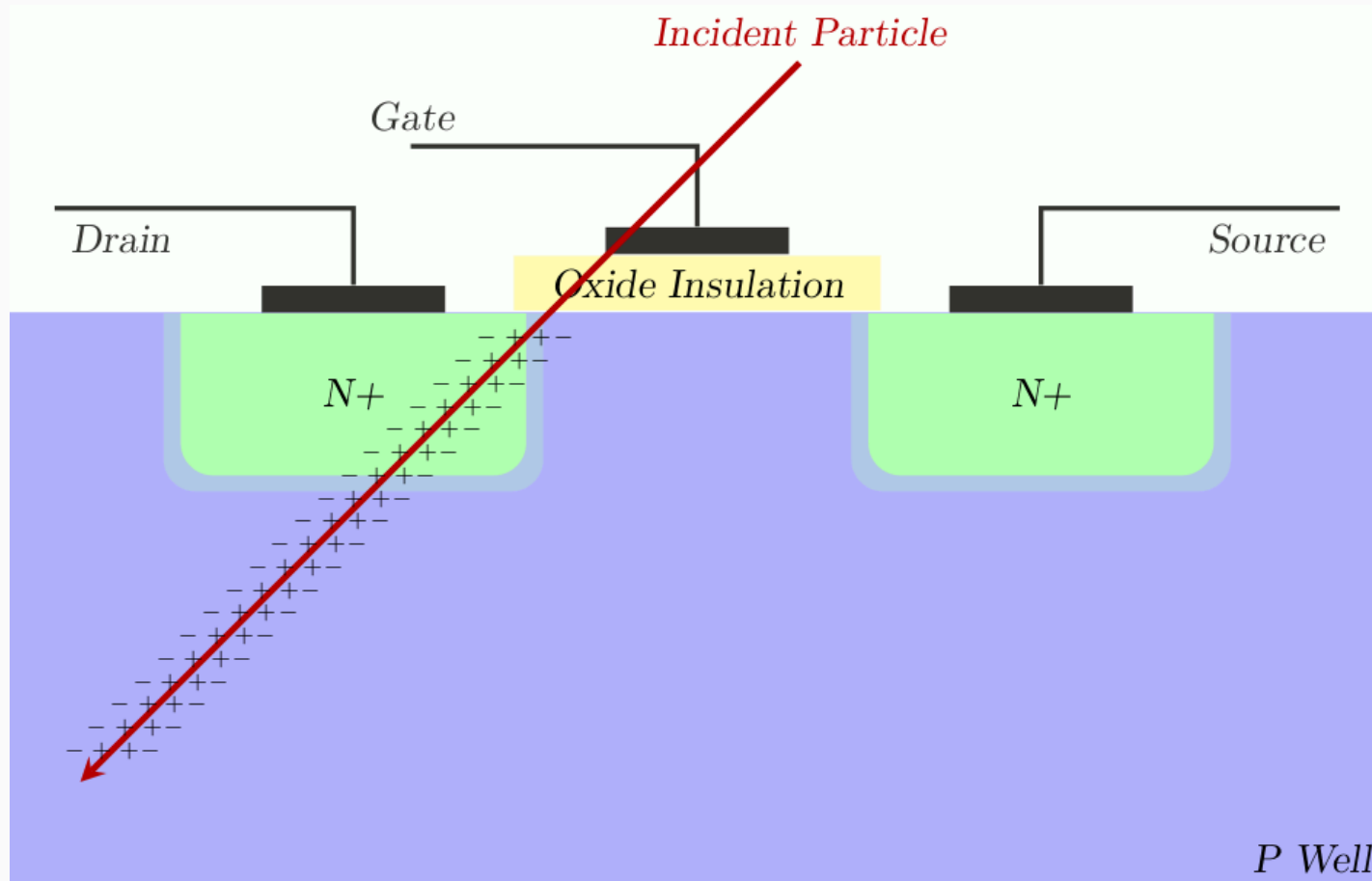Source: https://zeptobars.com/en/read/tt04-tinytapeout-silicon-inside-gds-sky130

Source: Lattice iCE40 UltraPlus Family Data Sheet. © 2021 Lattice Semiconductor Corp.

Single Event Upsets

Source: https://www.cogenda.com/article/SEE
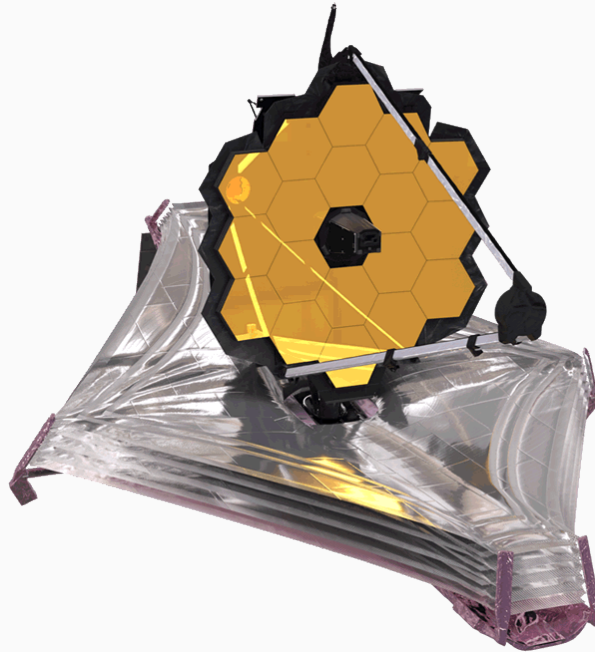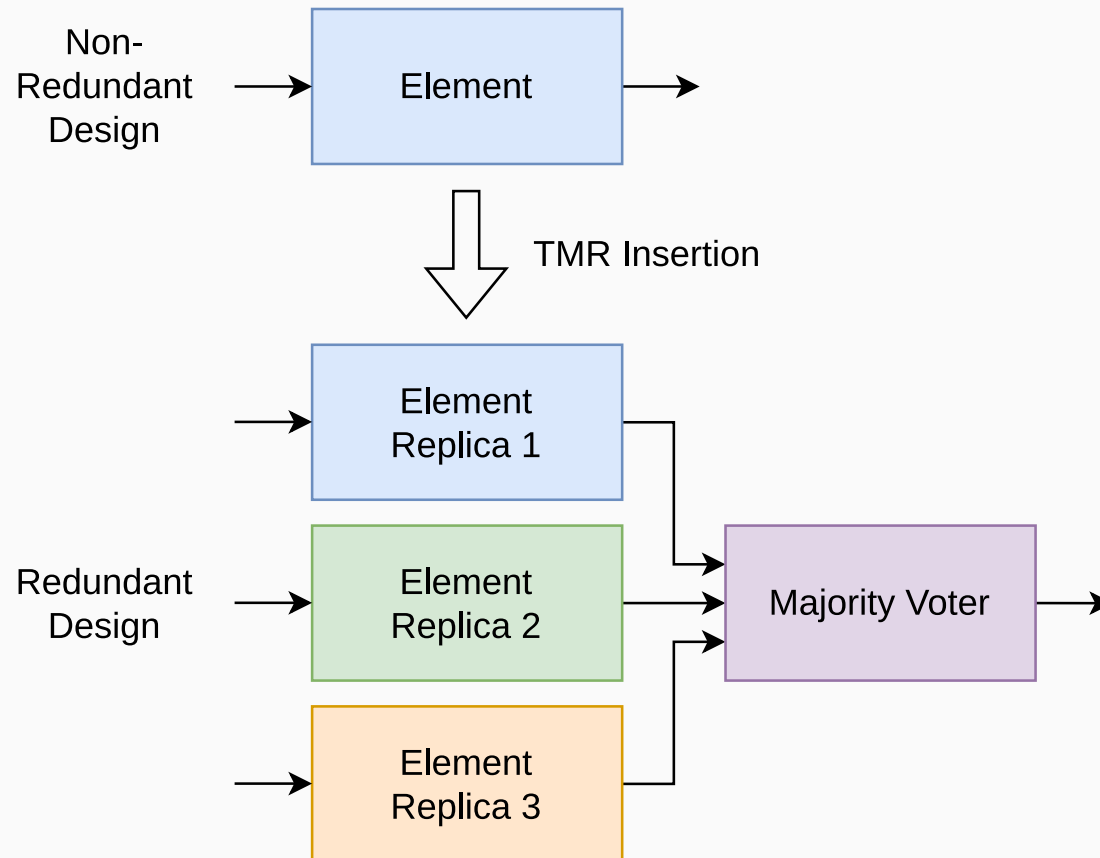
Protection from SEUs remains expensive!

RAD750 CPU [1] (James Webb Space Telescope, Curiosity rover, + many more) is commonly used, but costs **>$200,000 USD** [2]!

Source: https://commons.wikimedia.org/wiki/File:JWST_spacecraft_model_3.png

Triple Modular Redundancy

TMR can be added manually...

but this is **time consuming** and **error prone**.

Can we automate it?

TaMaRa

Implement TMR as a pass in an EDA synthesis tool.

- Integrated with the rest of the flow
- Easy to use
- Fully automated

Concept

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Goal: Pick any design, of any complexity, "press a button" and have it be rad-hardened.

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- Proprietary vendor tools (Synopsys, Cadence, Xilinx, etc) immediately discarded
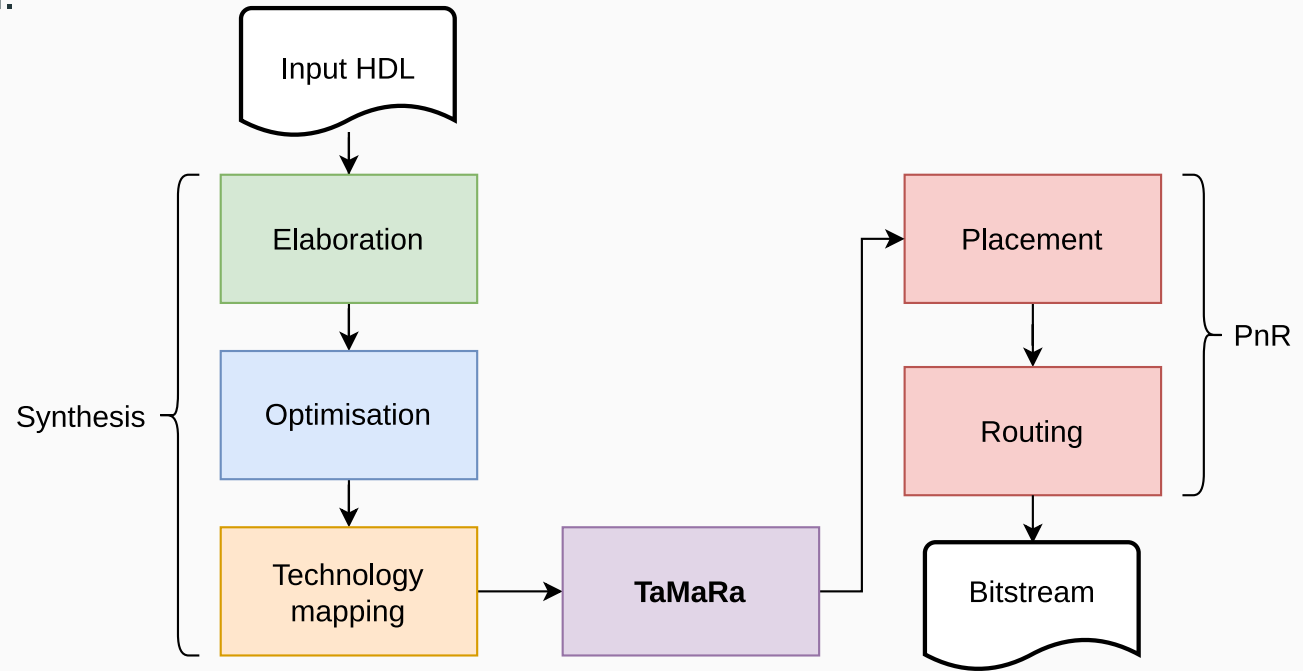- Can't be extended to add custom passes

Two main paradigms:

- **Design-level approaches** ("thinking in terms of HDL")
  - Kulis [4], Lee [5]
- **Netlist-level approaches** ("thinking in terms of circuits")
  - Johnson [6], Benites [7], Skouson [8]

TaMaRa is mainly netlist-driven. Voter insertion is inspired by Benites [7] "logic cones" concept, and parts of Johnson [6].

Also propagate a Verilog annotation to select TMR granularity (like Kulis [4]).

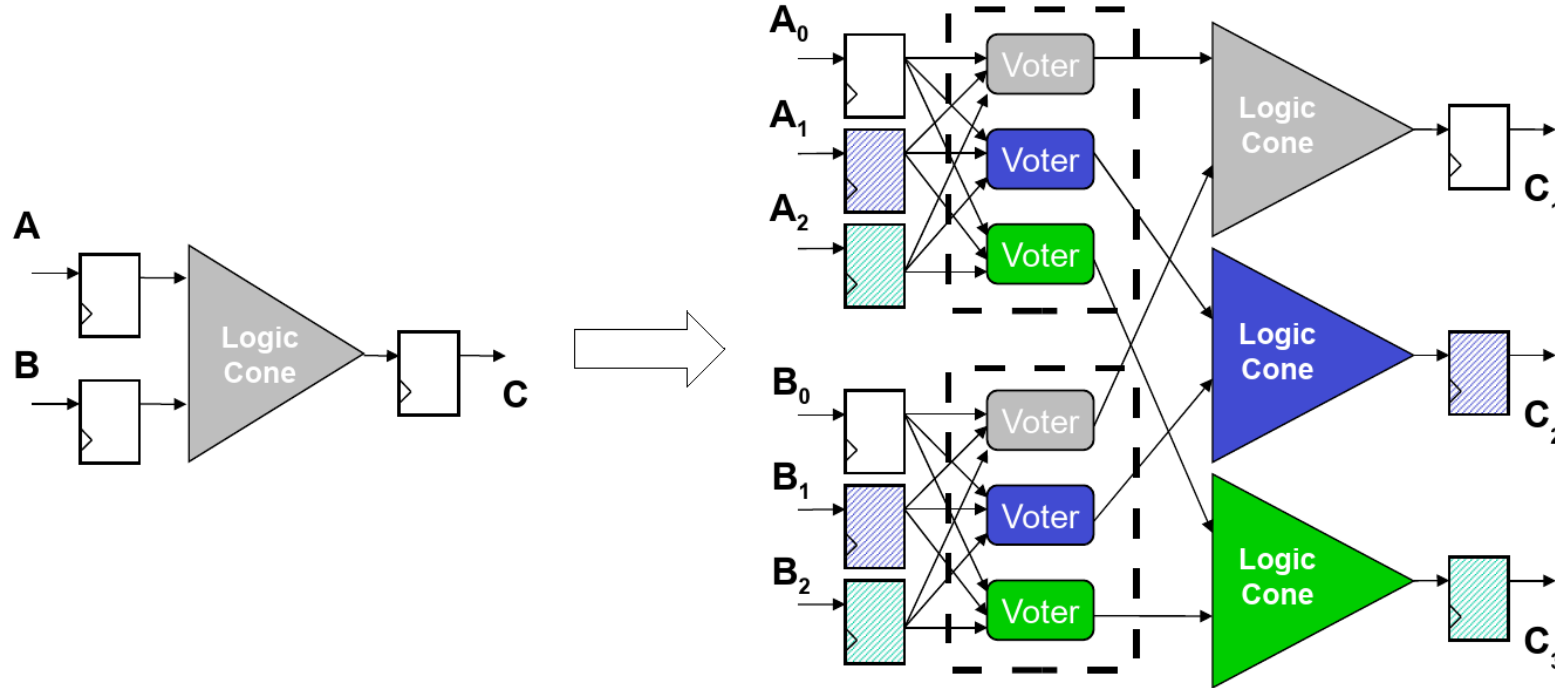Runs after techmapping (i.e. after abc in Yosys)

Source: [9]

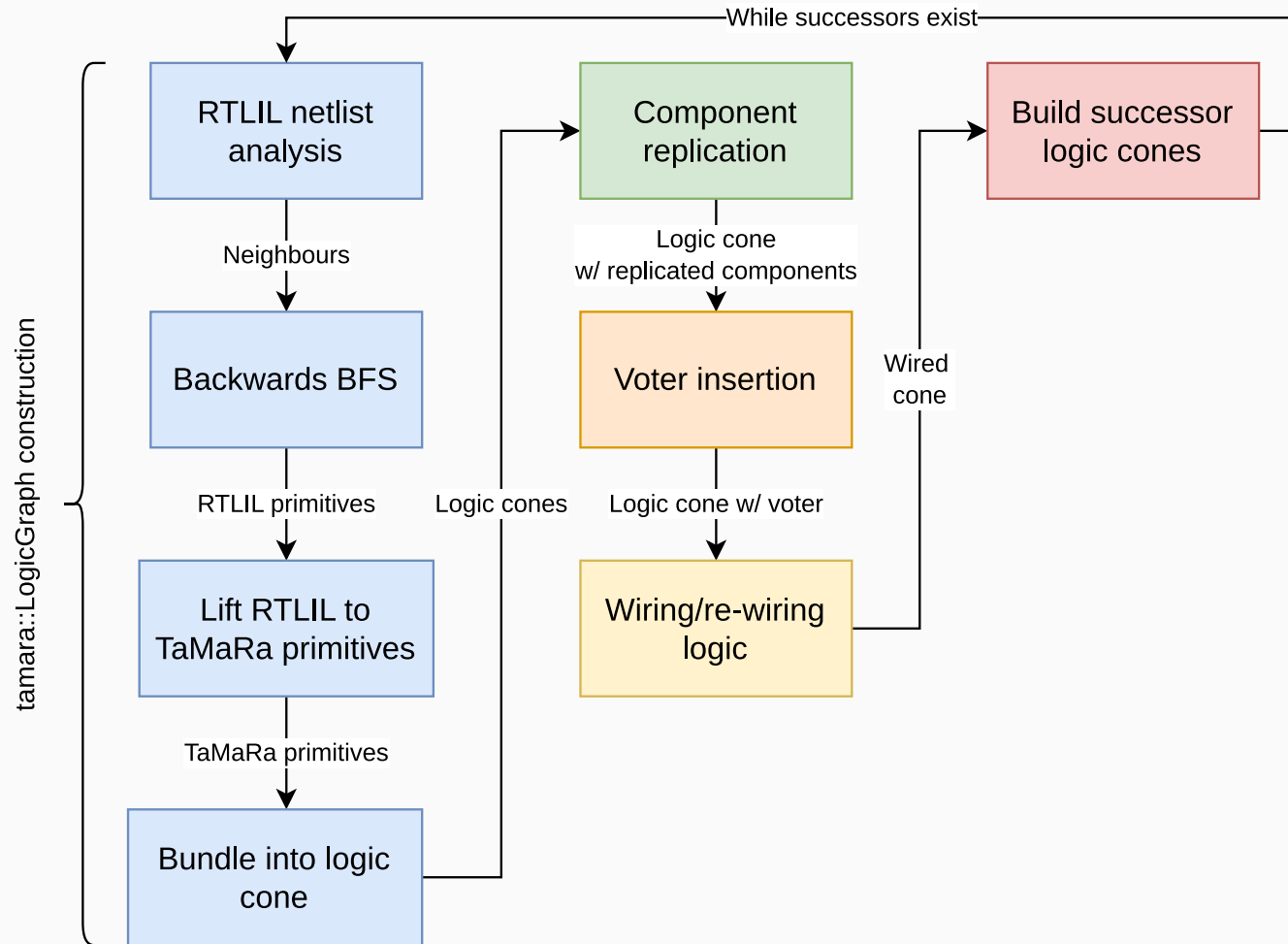**Figure 1** **A logic cone is a set of logic bounded by FFs and I/O.** When TMR is applied, each logic cone contains part of the voting logic.

TaMaRa algorithm: In depth

Verification

Comprehensive verification procedure using formal methods, simulation and fuzzing.

Driven by SymbiYosys tools *eqy* and *mcy*
- In turn driven by Satisfiability Modulo Theorem (SMT) solvers (Yices [10], Boolector [11], etc)

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Equivalence checking: Formally verify that the circuit is functionally equivalent before and after the TaMaRa pass.
- Ensures TaMaRa does not change the underlying behaviour of the circuit.

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Mutation: Formally verify that TaMaRa-processed circuits correct injected faults in a testbench
- Ensures TaMaRa does its job!

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Idea:
1. Use Verismith [12] to generate random Verilog RTL.
2. Run TaMaRa synthesis end-to-end.
3. Use formal equivalence checking to verify the random circuits behave the same before/after TMR.

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Problem: Mutation
- Need valid testbenches for these random circuits
- Requires automatic test pattern generation (ATPG), highly non-trivial
- Future topic of further research

Simulation

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Use one of Verilator or Yosys' own cxxrtl to simulate a full design.

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- Currently considering picorv32 RISC-V CPU as the Device Under Test (DUT)
- Simpler DUTs will be tested as well

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Concept:
- Iterate over the netlist, randomly consider flipping a bit every cycle
  ‣ May be non-trivial depending on simulator
- Self-checking testbench that ensures the DUT responds correctly (e.g. RISC-V CoreMark)

Current status & future

Algorithm design and planning essentially complete. Yosys internals (particularly RTLIL) understood to a satisfactory level (still learning as I go).

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Programming hopefully finished *around* February 2025, verification by April 2025.

Original circuit:

not_triplicate
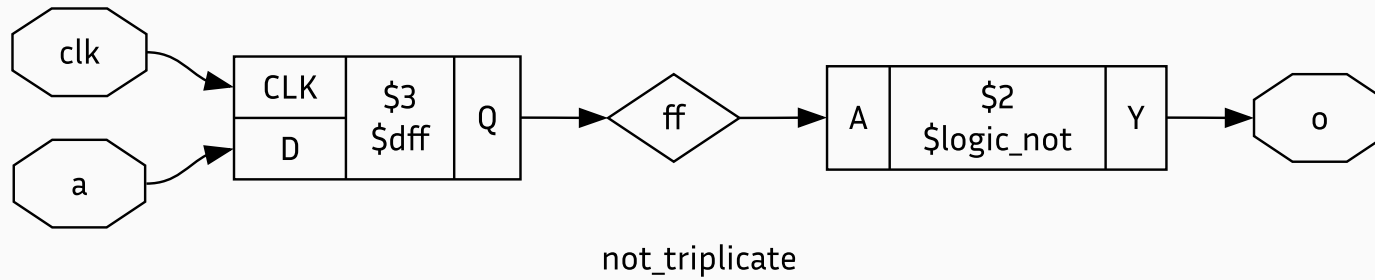
```systemverilog
(* tamara_triplicate *)
module not_triplicate(
    input logic a,
    input logic clk,
    output logic o
);

logic ff;

always_ff @(posedge clk) begin
    ff <= a;
end

assign o = !ff;

endmodule
```

After `tamara_debug replicateNot`:
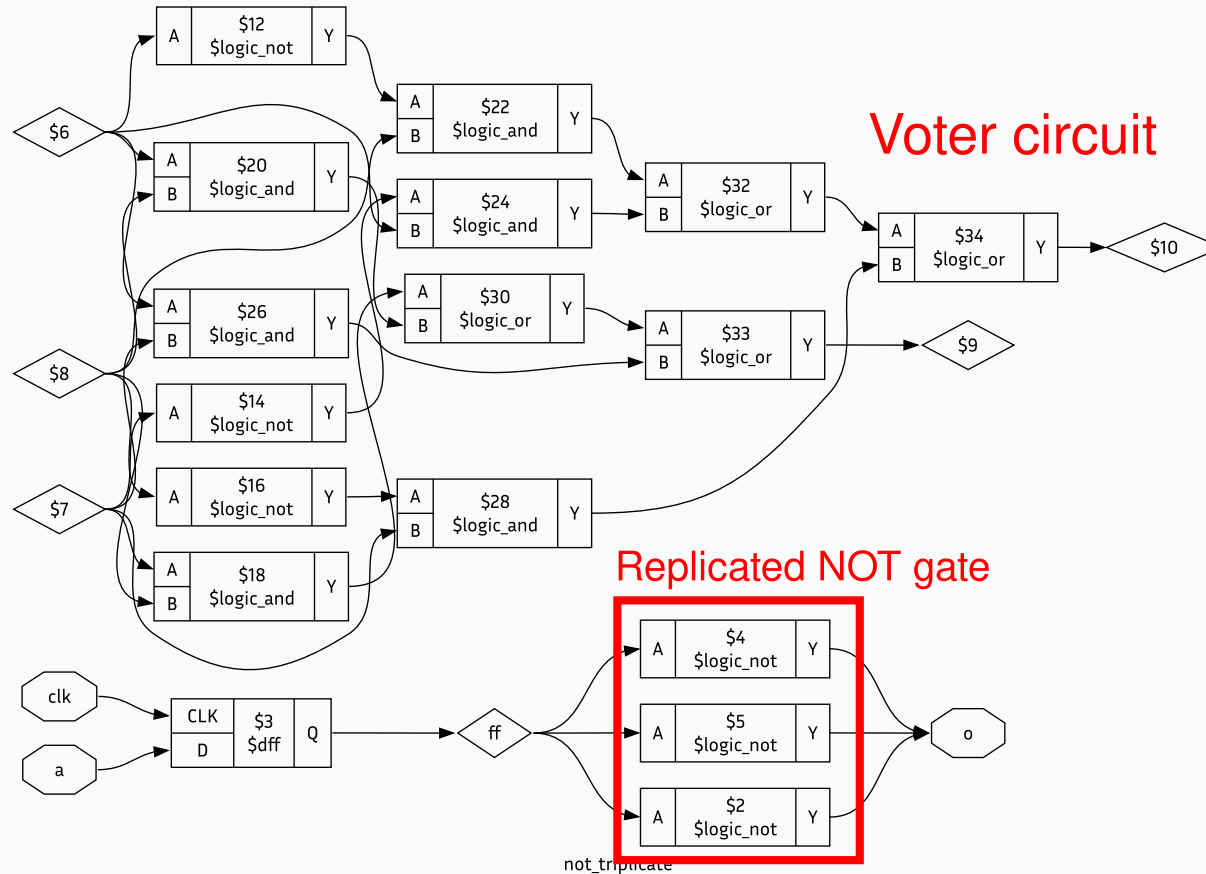
Voter circuit:

a	b	c	out	err
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

```systemverilog
module voter(
    input logic a,
    input logic b,
    input logic c,
    output logic out,
    output logic err
);
    assign out = (a && b) || (b && c) || (a && c);
    assign err = (!a && c) || (a && !b) || (b && !c);
endmodule
```

Manual design in Logisim:
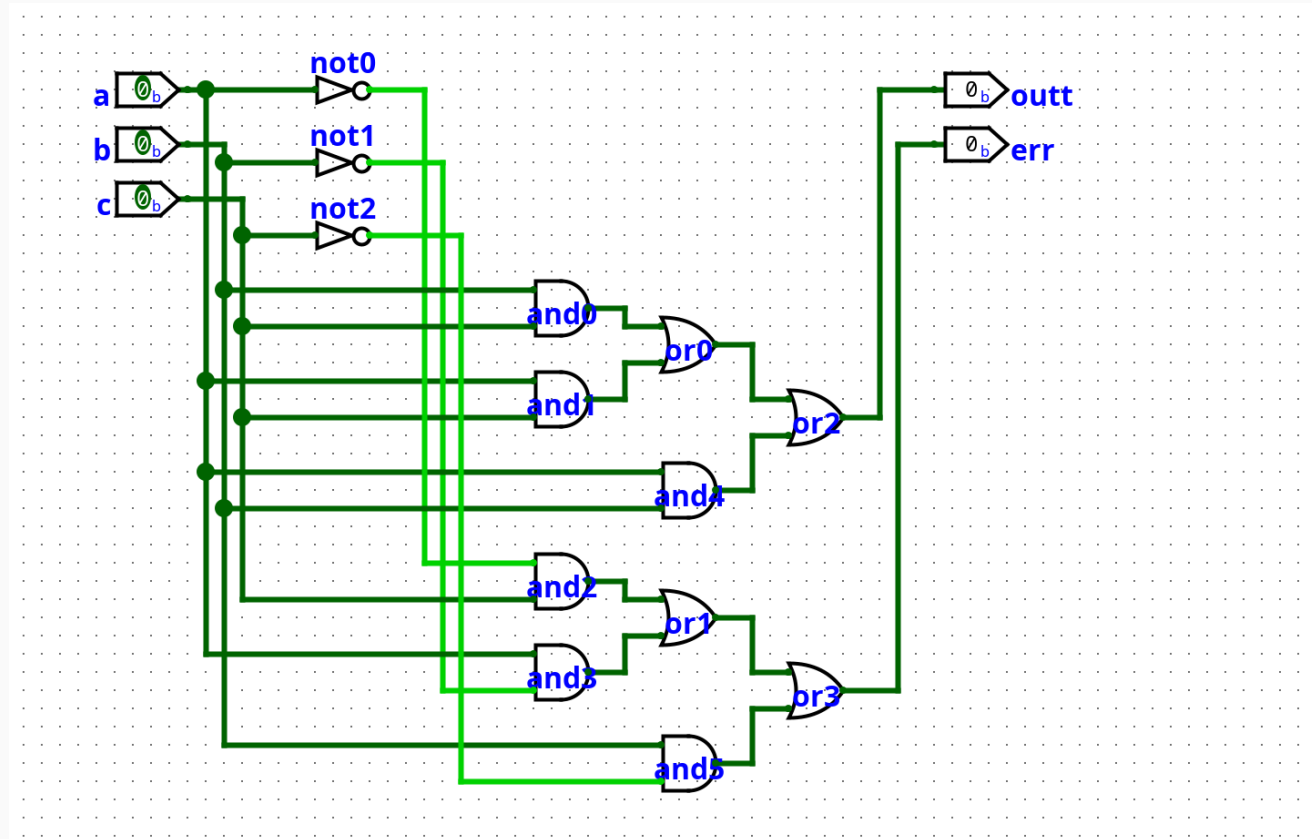
```
      Voter
tamara::VoterBuilder::build(RTLIL::Module
*module) {
        // NOT
        // a -> not0 -> and2
        WIRE(not0, and2);
        NOT(0, a, not0_and2_wire);

        ...

        // AND
        // b, c -> and0 -> or0
        WIRE(and0, or0);
        AND(0, b, c, and0_or0_wire);

        ...

        // OR
        // and0, and1 -> or0 -> or2
        WIRE(or0, or2);
        OR(0, and0_or0_wire,
and1_or0_wire, or0_or2_wire);

        ...

        return ...;
    }
```
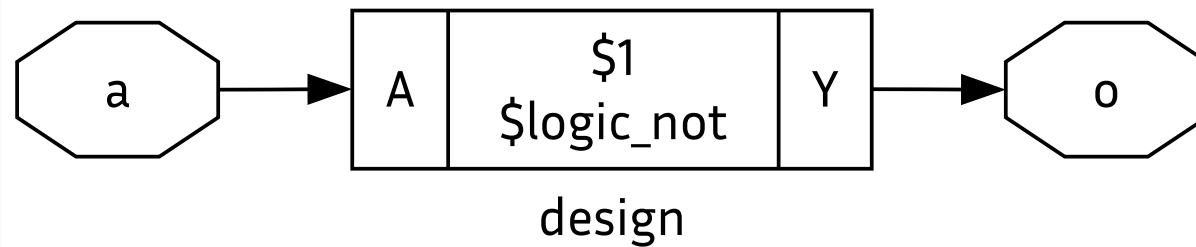

$auto$tamara_debug.cpp:57:execute$1
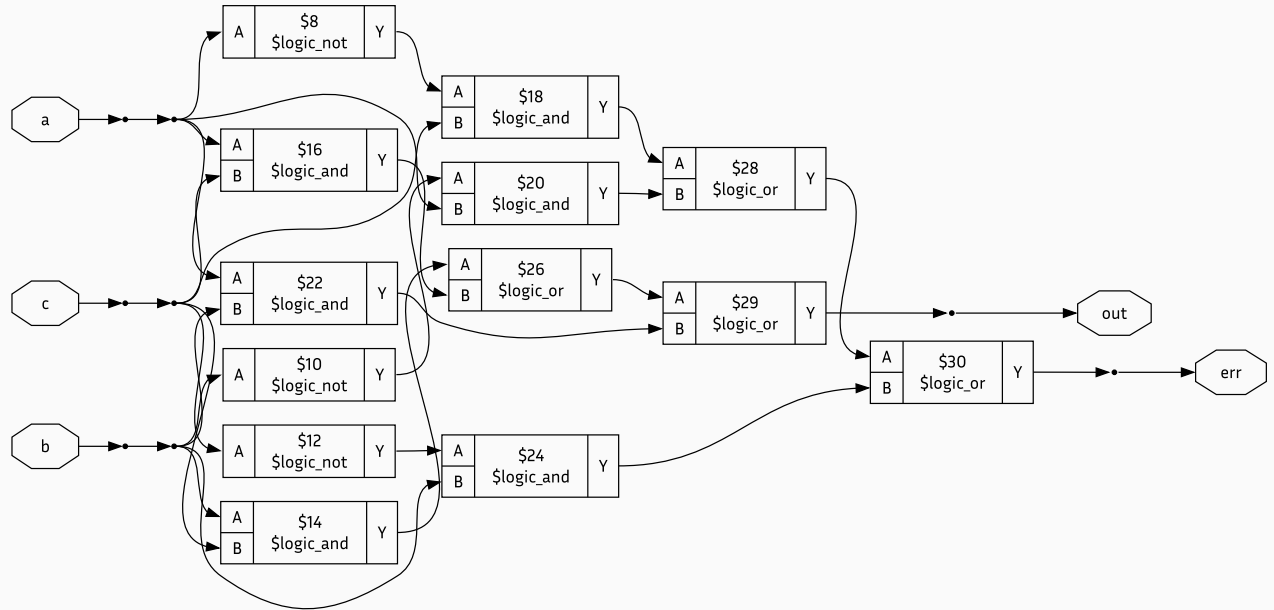
Progress: Equivalence checking

Marked equivalent by eqy in conjunction with Yices!

Original, very simple circuit:

After manual voter insertion (using SystemVerilog):

Voter circuit

Replicated NOT gates

Progress: Equivalence checking (Voter insertion)

Are they equivalent? Yes! (Thankfully)

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```
~/w/t/build (master) [n] »> eqy -f ../tests/formal/equivalence/not_voter.eqy
EQY 22:10:20 [not_voter] read_gold: starting process "yosys -ql not_voter/gold.log not_voter/gold.ys"
EQY 22:10:20 [not_voter] read_gold: finished (returncode=0)
EQY 22:10:20 [not_voter] read_gate: starting process "yosys -ql not_voter/gate.log not_voter/gate.ys"
EQY 22:10:20 [not_voter] read_gate: finished (returncode=0)
EQY 22:10:20 [not_voter] combine: starting process "yosys -ql not_voter/combine.log not_voter/combine.ys"
EQY 22:10:20 [not_voter] combine: finished (returncode=0)
EQY 22:10:20 [not_voter] partition: starting process "cd not_voter; yosys -ql partition.log partition.ys"
EQY 22:10:20 [not_voter] partition: finished (returncode=0)
EQY 22:10:20 [not_voter] run: starting process "make -C not_voter -f strategies.mk"
EQY 22:10:20 [not_voter] run: make: Entering directory '/home/matt/workspace/tamara/build/not_voter'
EQY 22:10:20 [not_voter] run: Running strategy 'sby' on 'design.o'..
EQY 22:10:20 [not_voter] run: Proved equivalence of partition 'design.o' using strategy 'sby'
EQY 22:10:20 [not_voter] run: make -f strategies.mk summary
EQY 22:10:20 [not_voter] run: make[1]: Entering directory '/home/matt/workspace/tamara/build/not_voter'
EQY 22:10:20 [not_voter] run: make[1]: Leaving directory '/home/matt/workspace/tamara/build/not_voter'
EQY 22:10:20 [not_voter] run: make: Leaving directory '/home/matt/workspace/tamara/build/not_voter'
EQY 22:10:20 [not_voter] run: finished (returncode=0)
EQY 22:10:20 [not_voter] Successfully proved equivalence of partition design.o
EQY 22:10:20 [not_voter] Successfully proved designs equivalent
EQY 22:10:20 [not_voter] summary: Elapsed clock time [H:MM:SS (secs)]: 0:00:00 (0)
EQY 22:10:20 [not_voter] summary: Elapsed process time [H:MM:SS (secs)]: 0:00:00 (0)
EQY 22:10:20 [not_voter] DONE (PASS, rc=0)
```
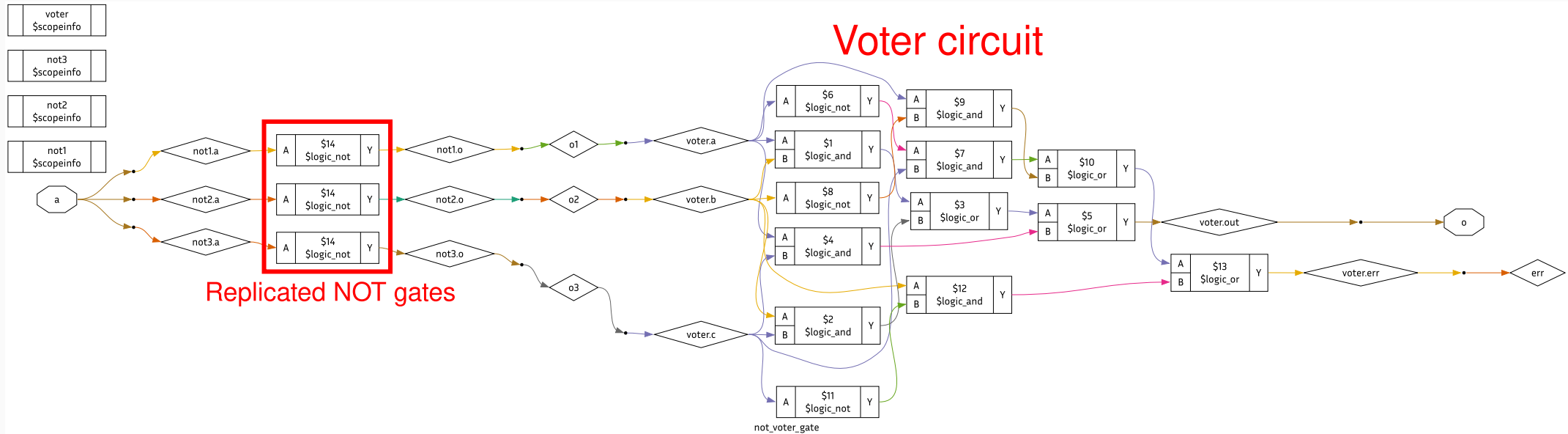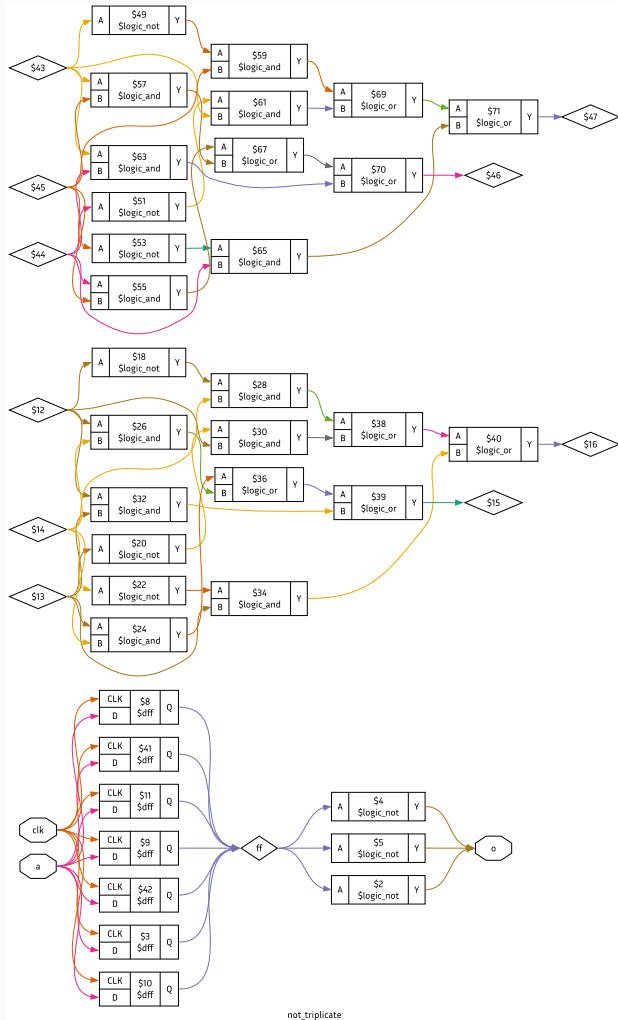
Caveat: Still need to verify circuits with more complex logic (i.e. DFFs).

Current problem: Duplicate DFFs

not_triplicate

```
7.2. Computing logic graph
Module has 1 output ports, 2 selected cells

Searching from output port o
Starting search for cone 0
     ... [snip] ...
Search complete for cone 0, have 3 items

Replicating 3 collected items for logic cone 0
     Replicating ElementCellNode $logic_not$../tests/verilog/
not_triplicate.sv:16$2
     Replicating ElementWireNode ff
     Replicating FFNode $procdff$3
Checking terminals
Input node $procdff$3 is not IONode, replicating it
     Replicating FFNode $procdff$3
Warning: When replicating FFNode $procdff$3 in cone 0: Already
replicated in logic cone 0
Input node o is IONode, it will NOT be replicated

Inserting voter into logic cone 0

... [snip] ...
```

The future

Tasks that remain (more or less):

- Fixing duplicate logic elements when replicating RTLIL primitives
- Wiring voter to logic elements, and wiring replicated logic elements to the rest of the circuit
- Considering wiring for feedback circuits *(expected to be complex/massive time sink!)*
- Global routing of error signal to a net
- Processing complex circuits like picorv32
- Writing a cycle-accurate fault-injection simulator, and associated testbenches
- Formal equivalence checking for complex circuits
- Formal mutation coverage
- Fuzzing *(if time permits)*

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- If TaMaRa works, its hybrid algorithm addresses a number of limitations in previous literature
- May be useful for research labs (CubeSats) and industry

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TaMaRa plugin code and tests will be released open-source under the MPL 2.0 (used by Firefox, Eigen, etc). Papers will hopefully be available under CC-BY.

TaMaRa will be freely available for anyone to use and build on. Combination of academic publication + open source for widest possible reach.

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I have also spoken with the team at YosysHQ GmbH and Sandia National Laboratories, who are very interested in the results of this project and its applications.

Conclusion

Summary

- TaMaRa: Automated triple modular redundancy EDA flow for Yosys
- Fully integrated into Yosys suite
- Takes any circuit, helps to prevent it from experiencing SEUs by adding TMR
- Synthesises netlist-driven approaches [9], [6] with design-level approaches [4]
- **Key goal:** "Click a button" and have any circuit run in space/in high reliability environments!

I'd like to extend my gratitude to N. Engelhardt of YosysHQ, the team at Sandia National Laboratories, and my supervisor Assoc. Prof. John Williams for their support and interest during this thesis so far.

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Thank you! Any questions?