TaMaRa:
An automated triple modular redundancy EDA flow for Yosys

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Prepared for YosysHQ and Sandia National Laboratories

Table of contents

Background

About me

TODO photo

Matt Young, 21 years old from Brisbane, Australia.

Graduated Bachelor of Computer Science earlier in 2024 from the University of Queensland.

Currently studying Bachelor of Computer Science (Honours) at UQ, which includes a one year research thesis.

Passionate about digital hardware design, embedded systems, high performance/low-level software/hardware. Looking to in future take up a PhD, and eventually research/work in the area of CPU/GPU/ASIC design, or FPGAs, or similar.

Motivation

Fault tolerant computing is important for safety critical sectors (aerospace, defence, medicine, etc.)

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ASICs and FPGAs commonly deployed in space (and on Earth)… but protection from SEUs remains expensive!

Triple Modular Redundancy

TODO describe TMR

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Let's automate it!

TaMaRa methodology

Concept

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- Proprietary vendor tools (Synopsys, Cadence, Xilinx, etc) immediately ignored as they can’t be extended

Existing works

Very important prior work done by J. M. Johnson and M. J. Wirthlin [2] at BYU.

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TODO algorithm

The TaMaRa algorithm

TODO

Verification

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I plan to have a comprehensive verification procedure using formal methods, simulation and fuzzing.

All driven by SymbiYosys tools *eqy* and *mcy* (in turn driven by theorem provers/SAT solvers)

Formal verification

Equivalence checking: Formally verify that the circuit is functionally equivalent before and after the TaMaRa pass.

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- Ensures TaMaRa does not change the underlying behaviour of the circuit.

Mutation: Formally verify that TaMaRa-processed circuits correct SEUs (single bit only)

- Ensures TaMaRa does its job!

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Idea:

1. Use Verismith [3] to generate random Verilog RTL.
2. Run TaMaRa synthesis end-to-end.
3. Use formal equivalence checking to verify the random circuits behave the same before/after TMR.

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Problem: Mutation

- We need valid testbenches for these random circuits, how would we generate that?
- Under active research in academia (may not be possible at the moment)

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Concept:

- Iterate over the netlist, randomly consider flipping a bit every cycle.
- Write a self-checking testbench and ensure that the DUT responds correctly

Technical implementation

Currently implemented in C++20, using CMake.

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Run `tmr` after synthesis, but before techmapping.

Run `tmr_finalise` just before techmapping (ensuring no more optimisation passes will run).

Current status & future

Current status

TODO

Mostly focused around literature reviews, scoping out the problem, formulating requirements, etc.

That being said, I also have a skeleton Yosys plugin loading.

The future

This will be implemented for my Honours thesis over the next 1 year.

- Honours is kind of of like mini masters, it's an Australia-specific thing.
- Supervised by Assoc. Prof. John Williams (former PetaLogix, Xilinx)

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Ideally, TaMaRa will be released open-source under the MPL 2.0.

- Pending university IP shenanigans, but there is a good chance of being allowed to open-source it.

Conclusion

Summary

TODO

Bibliography

[1] D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist, and M. Milanovic, "Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs," *CoRR*, 2019, [Online]. Available: http://arxiv.org/abs/1903.10407

[2] J. M. Johnson and M. J. Wirthlin, "Voter insertion algorithms for FPGA designs using triple modular redundancy," in *Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays*, in FPGA '10. ACM, Feb. 2010. doi: 10.1145/1723112.1723154.

[3] Y. Herklotz and J. Wickerson, "Finding and Understanding Bugs in FPGA Synthesis Tools," in *ACM/SIGDA Int. Symp. on Field-Programmable Gate Arrays*, in FPGA '20. Seaside, CA, USA: ACM, 2020. doi: 10.1145/3373087.3375310.

Thank you!

Any questions?