An Automated Triple Modular Redundancy EDA Flow for Yosys

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Introduction

Safety-critical sectors require Application Specific Integrated Circuit (ASIC) designs and Field Programmable Gate Array (FPGA) gateware to be fault-tolerant. In particular, high-reliability spaceflight computer systems need to mitigate the effects of Single Event Upsets (SEUs) caused by ionising radiation. One common fault-tolerant design technique is Triple Modular Redundancy (TMR), which mitigates SEUs by triplicating key parts of the design and using voter circuits. Leveraging the open-source Yosys Electronic Design Automation (EDA) tool, in this work, I present **TaMaRa**: a novel fully automated TMR flow, implemented as a Yosys plugin.

Single Event Upsets

SEUs are caused by ionising radiation striking a CMOS transistor on an integrated circuit, and inducing a small charge which can flip bits (Figure 3). This is dangerous, as it can invalidate the results of important calculations, potentially causing loss of life and/or property in safety-critical scenarios.

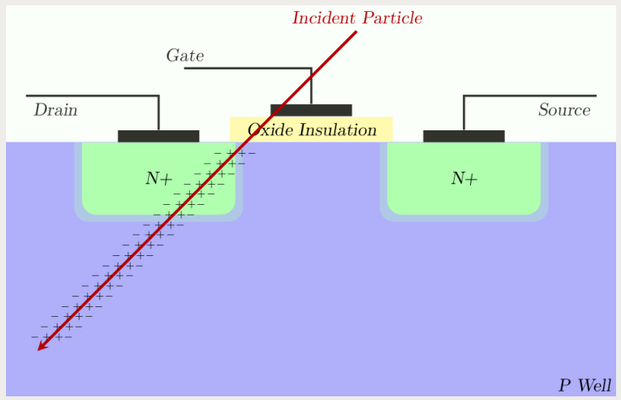

Figure 3: Mechanism of SEUs affecting CMOS transistors

Triple Modular Redundancy

Triple Modular Redundancy (TMR) mitigates SEUs by triplicating key parts of the design and using voter circuits to select a non-corrupted result if an SEU occurs (see Figure 1).

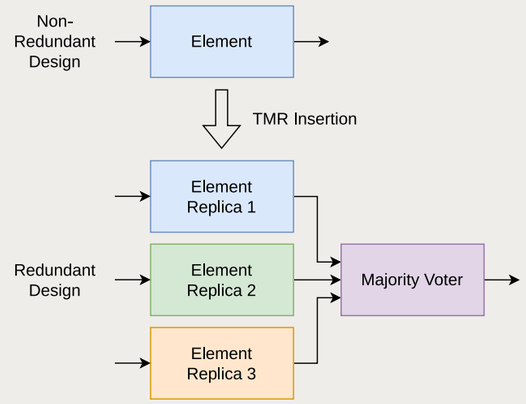

Figure 1: Diagram demonstrating TMR being inserted into an abstract design

Results: Circuits

Figure 4 shows a netlist schematic for a simple 2-bit multiplexer, and Figure 5 shows it after the application of TaMaRa TMR.

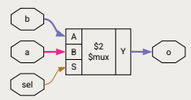

Figure 4: 2-bit multiplexer

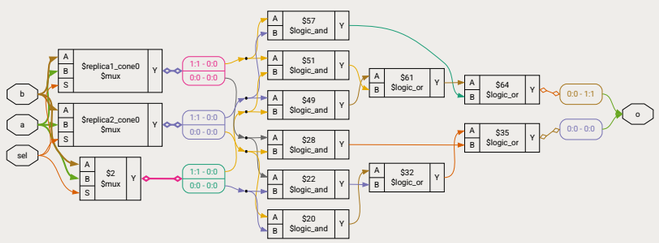

Figure 5: 2-bit multiplexer with TaMaRa TMR

TaMaRa Methodology

The **TaMaRa** algorithm (Figure 2), introduced in this work, automates the insertion of TMR at the post-synthesis netlist level.

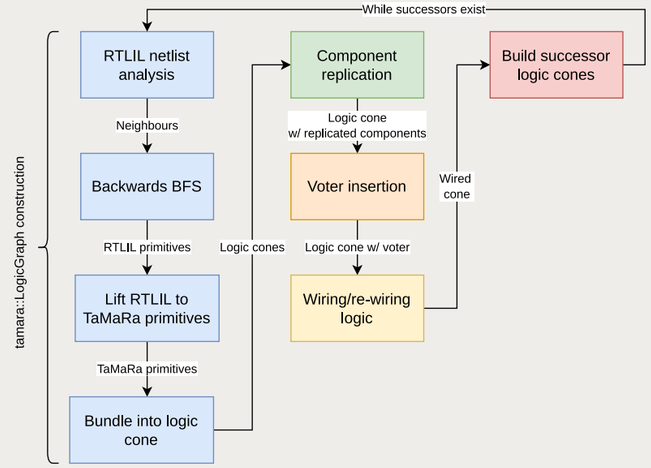

Figure 2: Description of the TaMaRa algorithm

Results: Reliability

TaMaRa demonstrates the capability of mitigating simulated SEU faults in a large-scale formally verified fault-injection campaign. When the voter is itself protected from faults (Figure 6), the algorithm performs well; but in more realistic unprotected scenarios, faults can still occur (Figure 7).

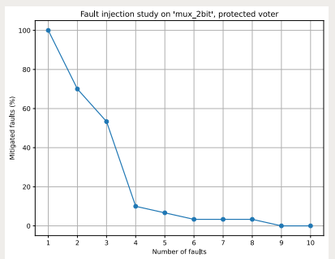

Figure 6: Protected voter

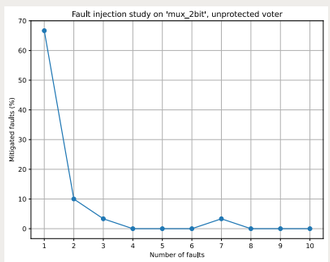

Figure 7: Unprotected voter

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Acknowledgements

N. Engelhardt, George Rennie, Emil J. Tywoniak, Krystine Sherwin, Catherine “whitequark”, Jannis Harder, John Williams, Peter Sutton, and my friends and family.

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