An Automated Triple Modular Redundancy EDA Flow for Yosys

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Introduction

Safety-critical sectors require Application Specific Integrated Circuit (ASIC) designs and Field Programmable Gate Array (FPGA) gateware to be fault-tolerant. Particularly, high-reliability spaceflight computer systems need to mitigate the effects of Single Event Upsets (SEUs) caused by ionising radiation. One common fault-tolerant design technique is Triple Modular Redundancy (TMR), which mitigates SEUs by triplicating key parts of the design and using voter circuits. Leveraging the open-source Yosys Electronic Design Automation (EDA) tool, in this work, I present *TaMaRa*: a novel fully automated TMR flow, implemented as a Yosys plugin.

Peace be with you

Figure 1: ‘Doves [...] are used in many settings as symbols of peace, freedom or love. Doves appear in the symbolism of Judaism, Christianity, Islam and paganism, and of both military and pacifist groups.’

Another one

We are peaceful doves.

Third Column

Methodology

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