TaMaRa:
An automated triple modular redundancy EDA flow for Yosys

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Prepared for YosysHQ and Sandia National Laboratories

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Background

About me

Matt Young, 21 years old from Brisbane, Australia.

Graduated Bachelor of Computer Science earlier in 2024 from the University of Queensland.

Currently studying Bachelor of Computer Science (Honours) at UQ, which includes a one year research thesis.

Passionate about digital hardware design, embedded systems, high performance/low-level software/hardware. Might take up a PhD in future :)

Motivation

Fault tolerant computing is important for safety critical sectors (aerospace, defence, medicine, etc.)

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ASICs and FPGAs commonly deployed in space (and on Earth)... but protection from SEUs remains expensive!

Triple Modular Redundancy

TODO describe TMR

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Let's automate it!

TaMaRa methodology

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- Proprietary vendor tools (Synopsys, Cadence, Xilinx, etc) immediately discarded
- Can’t be extended to add custom passes

Existing works

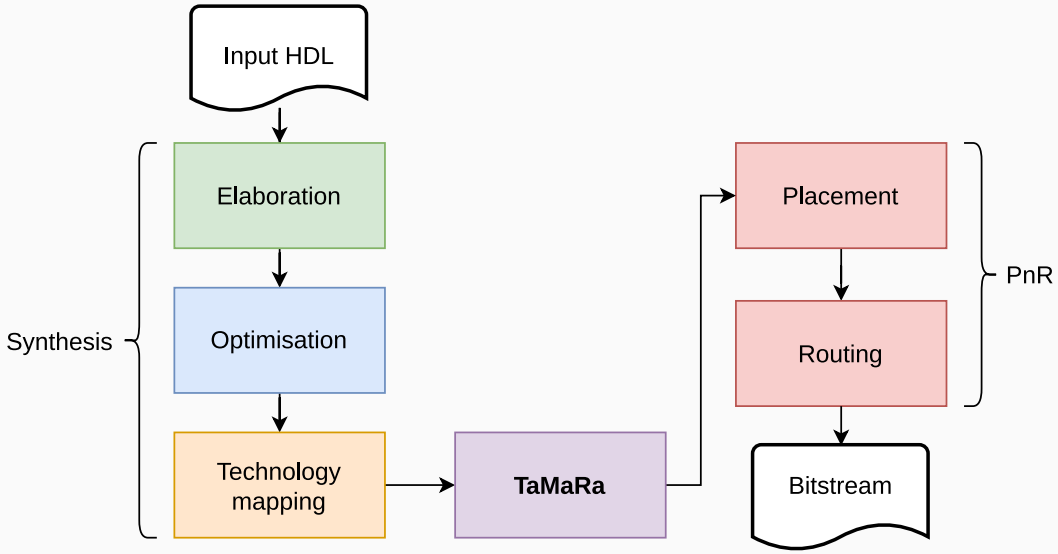
Two main paradigms:

- **Design-level approaches** (“thinking in terms of HDL”)
  - Kulis [2], Lee [3]
- **Netlist-level approaches** (“thinking in terms of circuits”)
  - Johnson [4], Benites [5], Skouson [6]

The TaMaRa algorithm

TaMaRa will mainly be netlist-driven, using Johnson's [4] voter insertion algorithm.

Also aim to propagate a `(* triplicate *)` HDL annotation to select TMR granularity (similar to Kulis [2])



The TaMaRa algorithm

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Why netlist driven with the `(* triplicate *)` annotation?

- Removes the possibility of Yosys optimisation eliminating redundant TMR logic
- Removes the necessity of complex blackboxing logic and trickery to bypass the normal design flow
- Cell type shouldn't matter, TaMaRa targets FPGAs and ASICs
- Still allows selecting TMR granularity - **best of both worlds**

Verification

Comprehensive verification procedure using formal methods, simulation and fuzzing.

Driven by SymbiYosys tools *eqy* and *mcy*

- In turn driven by theorem provers/SAT solvers

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- Ensures TaMaRa does its job!

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Idea:

1. Use Verismith [7] to generate random Verilog RTL.
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Problem: Mutation

- We need valid testbenches for these random circuits, how would we generate that?
- Under active research in academia (may not be possible at the moment)

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We want to simulate an SEU environment.

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Concept:

- Iterate over the netlist, randomly consider flipping a bit every cycle
- Write a self-checking testbench and ensure that the DUT responds correctly

Technical implementation

Currently implemented in C++20, using CMake.

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Run `tamara_propagate` after `read_verilog` to propagate the `(* triplicate *)` annotations.

Run `tamara_tmr` after techmapping to perform triplication and voter insertion (add TMR).

Current status & future

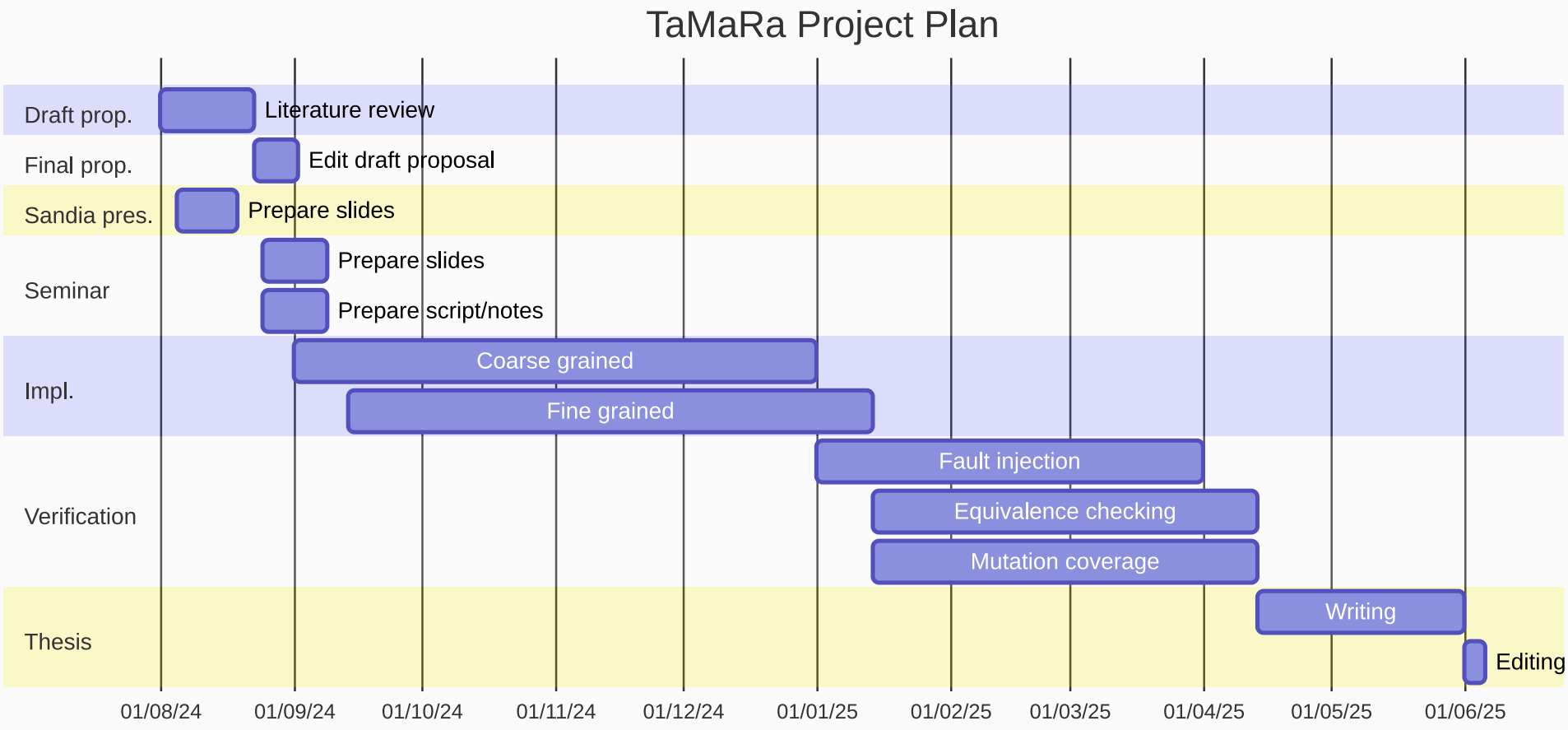
Current status

Mostly focused around literature reviews, scoping out the problem, formulating requirements, etc.

Programming expected to start in the next 1-2 weeks.

Skeleton plugin does exist with CMake/Ninja-based toolchain.

The future


TaMaRa Project Plan
Draft prop.
Literature review
Final prop.
Edit draft proposal
Sandia pres.
Prepare slides
Seminar
Prepare slides
Prepare script/notes
Impl.
Coarse grained
Fine grained
Verification
Fault injection
Equivalence checking
Mutation coverage
Thesis
Writing
Editing
01/08/24
01/09/24
01/10/24
01/11/24
01/12/24
01/01/25
01/02/25
01/03/25
01/04/25
01/05/25
01/06/25

The future

This will be implemented for my Honours thesis over the next 1 year.

- Honours is kind of of like mini masters, it's an Australia-specific thing.
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Programming hopefully finished *around* February 2025, verification by April 2025.

Ideally, TaMaRa will be released open-source under MPL 2.0.

- Pending university IP shenanigans...

Conclusion

Summary

- Automated triple modular redundancy EDA flow for Yosys
- Takes any circuit, helps to prevent it from experiencing SEUs
- Click a button and have any circuit run in space/in high reliability environments!

Summary

[1] D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist, and M. Milanovic, "Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs," *CoRR*, 2019, [Online]. Available: http://arxiv.org/abs/1903.10407

[2] S. Kulis, "Single Event Effects mitigation with TMRG tool," *Journal of Instrumentation*, vol. 12, no. 1, p. C01082–C01082, Jan. 2017, doi: 10.1088/1748-0221/12/01/c01082.

[3] G. Lee, D. Agiakatsikas, T. Wu, E. Cetin, and O. Diessel, "TLegUp: A TMR Code Generation Tool for SRAM-Based FPGA Applications Using HLS," in *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2017, pp. 129–132. doi: 10.1109/FCCM.2017.57.

[4] J. M. Johnson and M. J. Wirthlin, "Voter insertion algorithms for FPGA designs using triple modular redundancy," in *Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays*, in FPGA '10. ACM, Feb. 2010. doi: 10.1145/1723112.1723154.

[5] L. A. C. Benites and F. L. Kastensmidt, "Automated design flow for applying Triple Modular Redundancy (TMR) in complex digital circuits," in *2018 IEEE 19th Latin-American Test Symposium (LATS)*, 2018, pp. 1–4. doi: 10.1109/LATW.2018.8349668.

[6] D. Skouson, A. Keller, and M. Wirthlin, "Netlist Analysis and Transformations Using SpyDrNet," in *Proceedings of the 19th Python in Science Conference*, M. Agarwal, C. Calloway, D. Niederhut, and D. Shupe, Eds., 2020, pp. 40–47. doi: 10.25080/Majora-342d178e-006.

[7] Y. Herklotz and J. Wickerson, "Finding and Understanding Bugs in FPGA Synthesis Tools," in *ACM/SIGDA Int. Symp. on Field-Programmable Gate Arrays*, in FPGA '20. Seaside, CA, USA: ACM, 2020. doi: 10.1145/3373087.3375310.

Thank you!

Any questions?