

	A1	SFC_I2C		SFC_I2C	A2		GND	B1	GND		GND	B2	GND
	A3	SFC_I2C		SFC_I2C	A4		SA1_INA	B3	SA		SA	B4	SA1_INA
	A5	SFC_SPI		SFC_SPI	A6		SA1_INB	B5	SA		SA	B6	SA1_INB
	A7	SFC_SPI		SFC_SPI	A8		SA2_INA	B7	SA		SA	B8	SA2_INA
	A9	SFC_SPI		SFC_IO	A10	RTC_RESET	SA2_INB	B9	SA		SA	B10	SA2_INB
EPS_SDA	A11	EPS_I2C		EPS_I2C	A12	EPS_SCL	SA3_INA	B11	SA		SA	B12	SA3_INA
EPS_IRQ	A13	EPS_I2C		EPS_IO	A14	EPS_RESET	SA3_INB	B13	SA		SA	B14	SA3_INB
WDT_MON	A15	EPS_IO		EPS_IO	A16	PL3_EN	GND	B15	GND		GND	B16	GND
COMM_BIAS	A17	COMM_IO		COMM_IO	A18	COMM_TMON	PL1_REG_5V0	B17	PL1		PL1	B18	PL1_REG_5V0
	A19	COMM_UART		COMM_UART	A20			B19	PL1		PL1	B20	
	A21	PL1_UART		PL1_UART	A22		GND	B21	GND		GND	B22	GND
	A23	PL1_IO		PL1_IO	A24		PL2_REG_5V0	B23	PL2		PL2	B24	PL2_REG_5V0
PL2_TLM	A25	PL1_IO		PL1_IO	A26		PL2_MAG_3V3	B25	PL2		PL2	B26	PL2_MAG_3V3
CSS1A	A27	PL2_UART		PL2_UART	A28		SYS_REG_3V3	B27	SYS		SYS	B28	SYS_REG_3V3
CSS2A	A29	PL2_AN		PL2_AN	A30	CSS1B	GND	B29	GND		GND	B30	GND
CSS3A	A31	PL2_AN		PL2_AN	A32	CSS2B	GND	B31	GND		GND	B32	GND
	A33	PL2_AN		PL2_AN	A34	CSS3B	PWR_SAFE	B33	FSW		FSW	B34	PWR_SAFE
	A35	PL2_SPI		PL2_SPI	A36		PWR_UNSF	B35	FSW		FSW	B36	PWR_UNSF
	A37	PL2_SPI		PL2_SPI	A38		BAT_SAFE	B37	FSW		FSW	B38	BAT_SAFE
	A39	PL2_SPI		PL2_SPI	A40		BAT_UNSF	B39	FSW		FSW	B40	BAT_UNSF
GSE_TLM	A41	GSE_UART		GSE_UART	A42	GSE_CMD	GND	B41	GND		GND	B42	GND
GSE_PGED	A43	GSE_PROG		GSE_PROG	A44	GSE_PGEC	DEP_UNREG	B43	SYS		SYS	B44	DEP_UNREG
GSE_RESET	A45	GSE_IO		GSE_IO	A46	GSE_DISARM	SYS_UNREG	B45	SYS		SYS	B46	SYS_UNREG
GSE_SEL0	A47	GSE_IO		GSE_IO	A48	GSE_SEL1	SW_UNREG	B47	SYS		SYS	B48	SW_UNREG
GSE_SEL2	A49	GSE_IO		GSE_IO	A50	GSE_SEL3	RTC_REG_3V3	B49	RTC		RTC	B50	RTC_REG_3V3
RSW_INHIBIT	A51	GSE_IO		GSE_IO	A52	BAT_INHIBIT	GND	B51	GND		GND	B52	GND