

AN EVOLUTION OF CUBESAT SUBSYSTEM DESIGN METHODS FOR...

by

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A thesis submitted in partial fulfillment
of the requirements for the degree

of

Master of Science

in

Electrical Engineering

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ACKNOWLEDGEMENTS

I would like acknowledge Acknowledgments must be double spaced and is limited to one page.

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ABSTRACT

The abstract must be single spaced and no more than 350 words, indent first line five spaces. The abstract must contain the following elements: (1) statement of the problem, (2) procedure or methods, (3) results, and (4) conclusions. Mathematical formulas, abbreviations, diagrams, and other illustrative materials should not be included. It should be written to be understood by a person who does not have expertise in the field.

INTRODUCTION

Welcome to the Montana State University electronic Thesis/Dissertation (ETD) L^AT_EX template. In this chapter various sections, subsections, and subsubsections are created and filled with random text). In Ch. ?? methods to write equations and how to include figures and tables are explored. Conclusions are drawn in Ch. 7.

Section

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Subsection With a Very Very Very Very
Very Very Very Very Very Very Long Title

For long subsection titles use the command `\longsubsection{#1}{#2}`, where `#1` is the first line of the long title, and `#2` is the second line of the long title. You can also pass an optional argument to this command that puts a shorter title in the table of contents as shown by the subsection below.

Another Subsection With a Very Very Very
Very Very Very Very Very Very Long Title

The are **not** similar commands for sections and subsections as these are not specified in the MSU style guide.

BACKGROUND

CubeSats are a growing industry and are becoming increasingly more capable and affordable space mission options. Off-the-shelf components can be used to develop complex missions....

DESIGN STUDY - SOLAR CELL EXPERIMENT

This subsystem design was part of the FIREBIRD-II mission, and was an electronic load used to measure the performance of a spacecraft's solar cells on orbit. By working with an industry partner, the SSEL was able to utilize cutting edge solar cell technology in exchange for providing the customer with low-cost flight heritage and useful environmental data. This chapter will focus on the design method used to fulfill the requirements as defined by the collaboration between the SSEL team and the customer. After discussing the subsystem requirements, the concept design can take shape, followed by the analyses and calculations performed to verify circuit functionality.

At this time, the SSEL relied on the Mentor Graphics PADS Suite for electrical computer aided design (ECAD), and integrated SPICE simulation was not a feature that was readily available. Therefore, simulations of the critical circuits and subcircuits was performed using LTSpice developed by Linear Technology. Then, a full schematic was captured in PADS for creating the PCB layout files and bill-of-materials needed for fabrication and assembly of the subsystem.

Requirements and Conceptual Design

Circuit Simulations and Calculations

PCB Layout and Mechanical Design

Calibration and Results

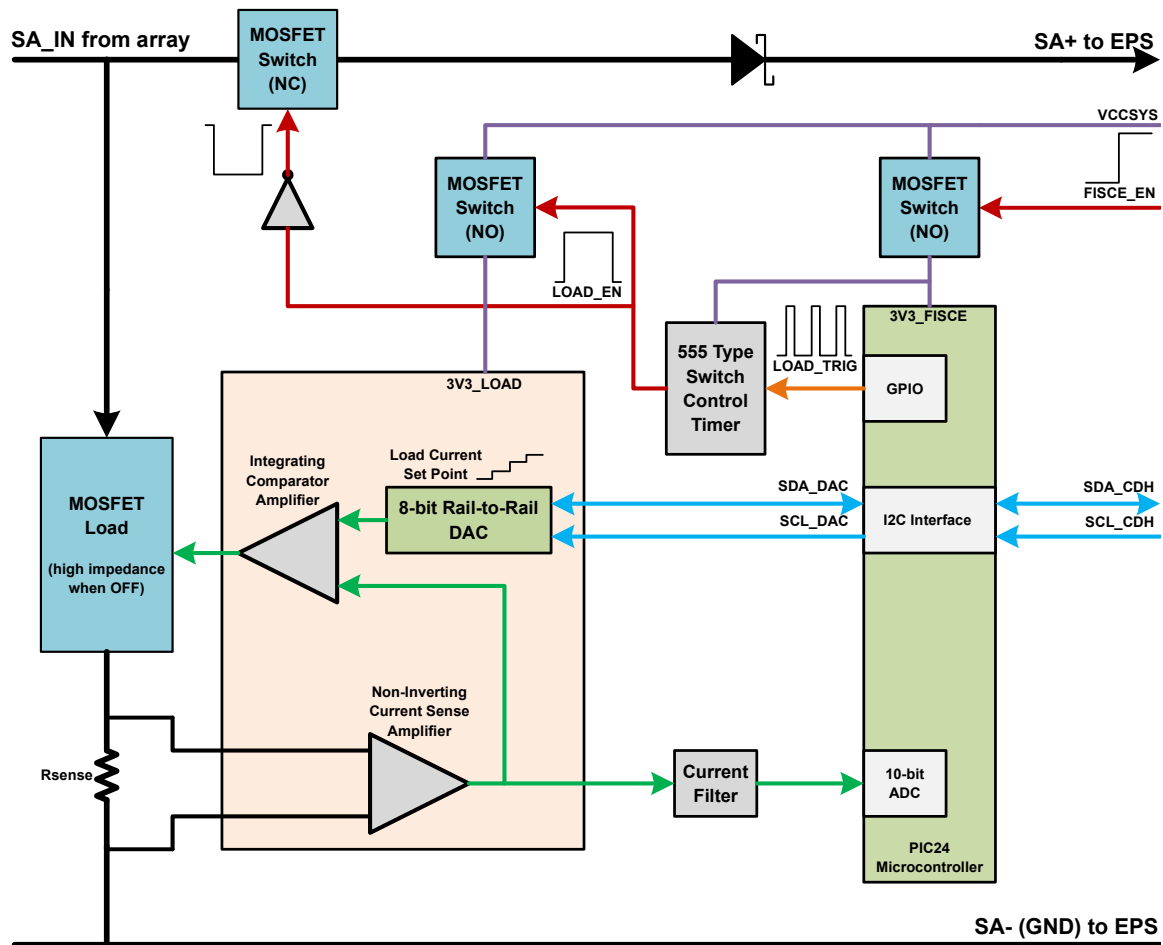


Figure 3.1: This block diagram represents the components of the FISCE load circuit and their functions.

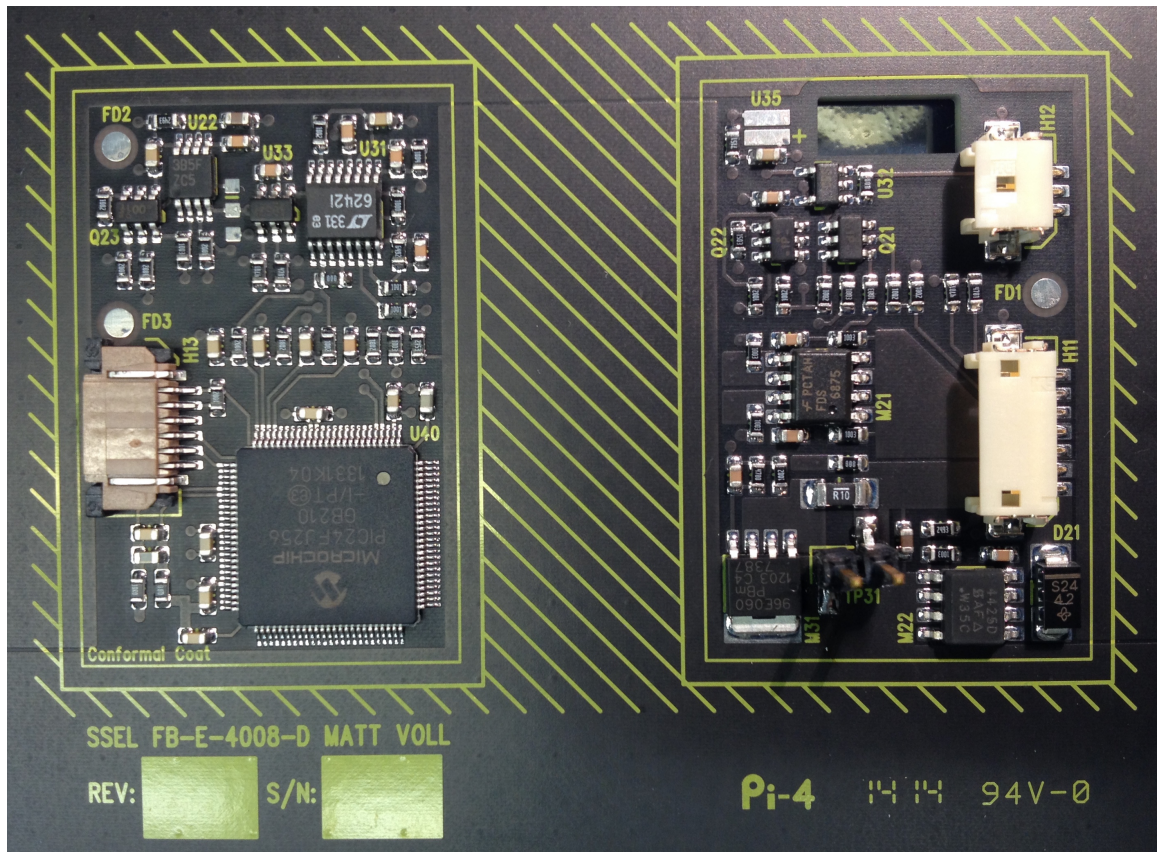


Figure 3.2: The assembled FISCE load circuit on the backside of the solar panel substrate.

DESIGN METHOD EXAMPLE: ELECTRICAL POWER SUBSYSTEM

This subsystem was designed to facilitate expanded capabilities of the IT-SPINS mission. Building on successes of the electrical power subsystem (EPS) used for the FIREBIRD-II mission, the design of an updated version of the Phoenix EPS began in the Spring of 2016. The original design came out of necessity, and began a trend of using SSEL developed subsystems for CubeSat missions rather than purchasing and integrating off-the-shelf solutions.

This chapter provides an investigation of how IT-SPINS mission requirements made a significant overhaul of the Phoenix EPS mandatory. Then, a conceptual design that incorporates those requirements is presented. With a block diagram in place, several circuit simulations and calculations were performed to verify that components of the design would operate as intended once built. The method used in this example effectively used a hierarchical schematic structure to reuse several “blocks” and make the schematic less cluttered. However, simulations were not well integrated into the design flow and were difficult to track as the design matured; if a simulation was modified or updated the corresponding schematic changes had to be done manually. Similarly, support documents such as connector pin reference tables were in a constant state of flux as the design progressed.

Figure 4.1 is an overview of the processes involved in designing the Phoenix EPS. Ideally, these steps would be linked in only a linear progression, i.e. each step would need to be completed and approved before moving onto the next. The arrows show that during the simulation and schematic entry phases there was a need to revise the subsystems requirements and conceptual design material. Also, there was essentially only one formal approval step, made when the PCB was fully laid out and ready for fabrication.

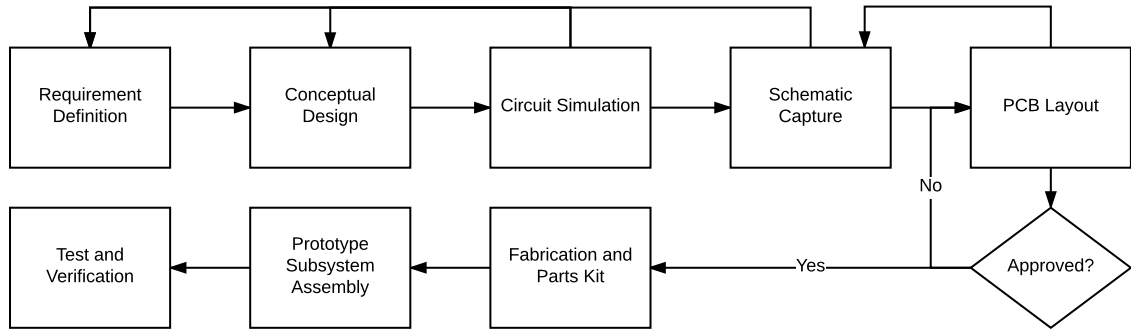


Figure 4.1: A simplified representation of the design method used in this chapter.

Requirements and Conceptual Design

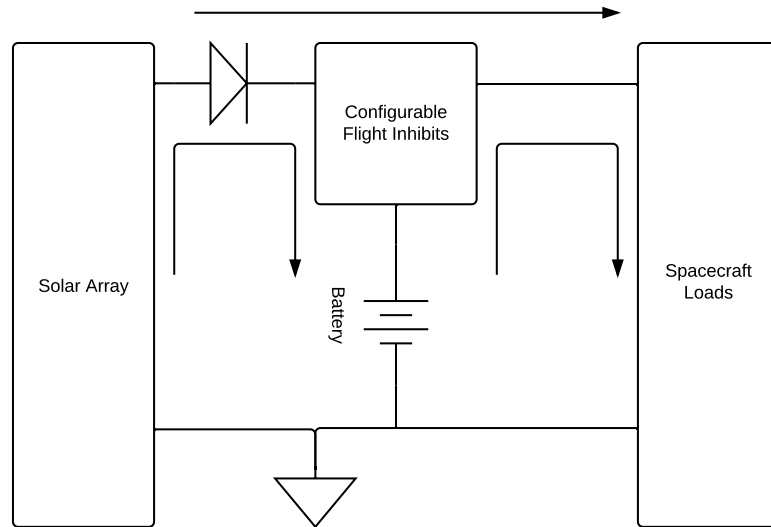


Figure 4.2: Basic configuration of a direct energy transfer (DET) power subsystem, with primary current paths shown by arrows.

Each resistor shown indicates a critical current sense location that is used to monitor the subsystem’s status and performance. The inhibit switches shown indicate the locations at which the power path is broken for “safing” the satellite during test and launch; the physical switches are not located on the

	A1	SFC_I2C			SFC_I2C	A2			GND	B1	GND			GND	B2	GND
	A3	SFC_I2C			SFC_I2C	A4			SA1_INA	B3	SA			SA	B4	SA1_INA
	A5	SFC_SPI			SFC_SPI	A6			SA1_INB	B5	SA			SA	B6	SA1_INB
	A7	SFC_SPI			SFC_SPI	A8			SA2_INA	B7	SA			SA	B8	SA2_INA
	A9	SFC_SPI			SFC_IO	A10		RTC_RESET	SA2_INB	B9	SA			SA	B10	SA2_INB
EPS_SDA	A11	EPS_I2C			EPS_I2C	A12	EPS_SCL		SA3_INA	B11	SA			SA	B12	SA3_INA
EPS_IRQ	A13	EPS_I2C			EPS_IO	A14	EPS_RESET		SA3_INB	B13	SA			SA	B14	SA3_INB
WDT_MON	A15	EPS_IO			EPS_IO	A16	PL3_EN		GND	B15	GND			GND	B16	GND
COMM_BIAS	A17	COMM_IO			COMM_IO	A18	COMM_TMON		PL1_REG_5V0	B17	PL1			PL1	B18	PL1_REG_5V0
	A19	COMM_UART			COMM_UART	A20				B19	PL1			PL1	B20	
	A21	PL1_UART			PL1_UART	A22			GND	B17	GND			GND	B22	GND
	A23	PL1_IO			PL1_IO	A24			PL2_REG_5V0	B23	PL2			PL2	B24	PL2_REG_5V0
	A25	PL1_IO			PL1_IO	A26			PL2_MAG_3V3	B25	PL2			PL2	B26	PL2_MAG_3V3
PL2_TLM	A27	PL2_UART			PL2_UART	A28			SYS_REG_3V3	B27	SYS			SYS	B28	SYS_REG_3V3
CSS1A	A29	PL2_AN			PL2_AN	A30	CSS1B		GND	B29	GND			GND	B30	GND
CSS2A	A31	PL2_AN			PL2_AN	A32	CSS2B		GND	B31	GND			GND	B32	GND
CSS3A	A33	PL2_AN			PL2_AN	A34	CSS3B		PWR_SAFE	B33	FSW			FSW	B34	PWR_SAFE
	A35	PL2_SPI			PL2_SPI	A36			PWR_UNSF	B35	FSW			FSW	B36	PWR_UNSF
	A37	PL2_SPI			PL2_SPI	A38			BAT_SAFE	B37	FSW			FSW	B38	BAT_SAFE
	A39	PL2_SPI			PL2_SPI	A40			BAT_UNSF	B39	FSW			FSW	B40	BAT_UNSF
	A41	GSE_UART			GSE_UART	A42	GSE_CMD		GND	B41	GND			GND	B42	GND
GSE_PGED	A43	GSE_PROG			GSE_PROG	A44	GSE_PGEC		DEP_UNREG	B43	SYS			SYS	B44	DEP_UNREG
GSE_RESET	A45	GSE_IO			GSE_IO	A46	GSE_DISARM		SYS_UNREG	B45	SYS			SYS	B46	SYS_UNREG
GSE_SEL0	A47	GSE_IO			GSE_IO	A48	GSE_SEL1		SW_UNREG	B47	SYS			SYS	B48	SW_UNREG
GSE_SEL2	A49	GSE_IO			GSE_IO	A50	GSE_SEL3		RTC_REG_3V3	B49	RTC			RTC	B50	RTC_REG_3V3
RSW_INHIBIT	A51	GSE_IO			GSE_IO	A52	BAT_INHIBIT		GND	B51	GND			GND	B52	GND

Figure 4.4: New connector pinouts.

Circuit Simulations and CalculationsPCB Layout and Mechanical DesignLessons Learned and Future Work

In this case, there were several times when the requirements, conceptual design, schematic, and PCB layout were all being updated and altered in parallel. As the IT-SPINS mission and the operation of its subsystems became more fully defined, the critically important EPS design had to be altered to maintain compatibility. In hindsight, these changes made the design method seem somewhat chaotic when

DESIGN STUDY - ELECTRICAL GROUND SUPPORT EQUIPMENT

This is the VOID EGSE design example.

Requirements and Conceptual Design

Circuit Simulations and Calculations

PCB Layout and Mechanical Design

Lessons Learned and Future Work

FUTURE METHODS

Investigating the possible methods for future use.

CONCLUSION

\LaTeX produces documents that look great, automatically handles references and citations, and easily incorporates figures and tables. This is not a guide to \LaTeX but rather an introduction to the MSU style. If you want more information about \LaTeX many introductory guides can be found online.

REFERENCES CITED

APPENDICES

APPENDIX A

EXAMPLE CODE

% MATLAB code to say 'hello world'

disp('Hello world')

APPENDIX B

EXAMPLE SCHEMATIC