

AN EVOLUTION OF CUBESAT SUBSYSTEM DESIGN METHODS FOR...

by

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A thesis submitted in partial fulfillment
of the requirements for the degree

of

Master of Science

in

Electrical Engineering

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ACKNOWLEDGEMENTS

I would like acknowledge Acknowledgments must be double spaced and is limited to one page.

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ABSTRACT

The abstract must be single spaced and no more than 350 words, indent first line five spaces. The abstract must contain the following elements: (1) statement of the problem, (2) procedure or methods, (3) results, and (4) conclusions. Mathematical formulas, abbreviations, diagrams, and other illustrative materials should not be included. It should be written to be understood by a person who does not have expertise in the field.

INTRODUCTION

Welcome to the Montana State University electronic Thesis/Dissertation (ETD) L^AT_EX template. In this chapter various sections, subsections, and subsubsections are created and filled with random text). In Ch. ?? methods to write equations and how to include figures and tables are explored. Conclusions are drawn in Ch. 7.

Section

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Subsection With a Very Very Very Very
Very Very Very Very Very Very Long Title

For long subsection titles use the command `\longsubsection{#1}{#2}`, where `#1` is the first line of the long title, and `#2` is the second line of the long title. You can also pass an optional argument to this command that puts a shorter title in the table of contents as shown by the subsection below.

Another Subsection With a Very Very Very
Very Very Very Very Very Very Long Title

The are **not** similar commands for sections and subsubsections as these are not specified in the MSU style guide.

BACKGROUND

CubeSats are a growing industry and are becoming increasingly more capable and affordable space mission options. Off-the-shelf components can be used to develop complex missions....

DESIGN STUDY - SOLAR CELL EXPERIMENT

This subsystem design was part of the FIREBIRD-II mission, and was an electronic load used to measure the performance of a spacecraft's solar cells on orbit. By working with an industry partner, the SSEL was able to utilize cutting edge solar cell technology in exchange for providing the customer with low-cost flight heritage and useful environmental data. This chapter will focus on the design method used to fulfill the requirements as defined by the collaboration between the SSEL team and the customer. After discussing the subsystem requirements, the concept design can take shape, followed by the analyses and calculations performed to verify circuit functionality.

At this time, the SSEL relied on the Mentor Graphics PADS Suite for electrical computer aided design (ECAD), and integrated SPICE simulation was not a feature that was readily available. Therefore, simulations of the critical circuits and subcircuits was performed using LTSpice developed by Linear Technology. Then, a full schematic was captured in PADS for creating the PCB layout files and bill-of-materials needed for fabrication and assembly of the subsystem.

Requirements and Conceptual Design

Circuit Simulations and Calculations

PCB Layout and Mechanical Design

Calibration and Results

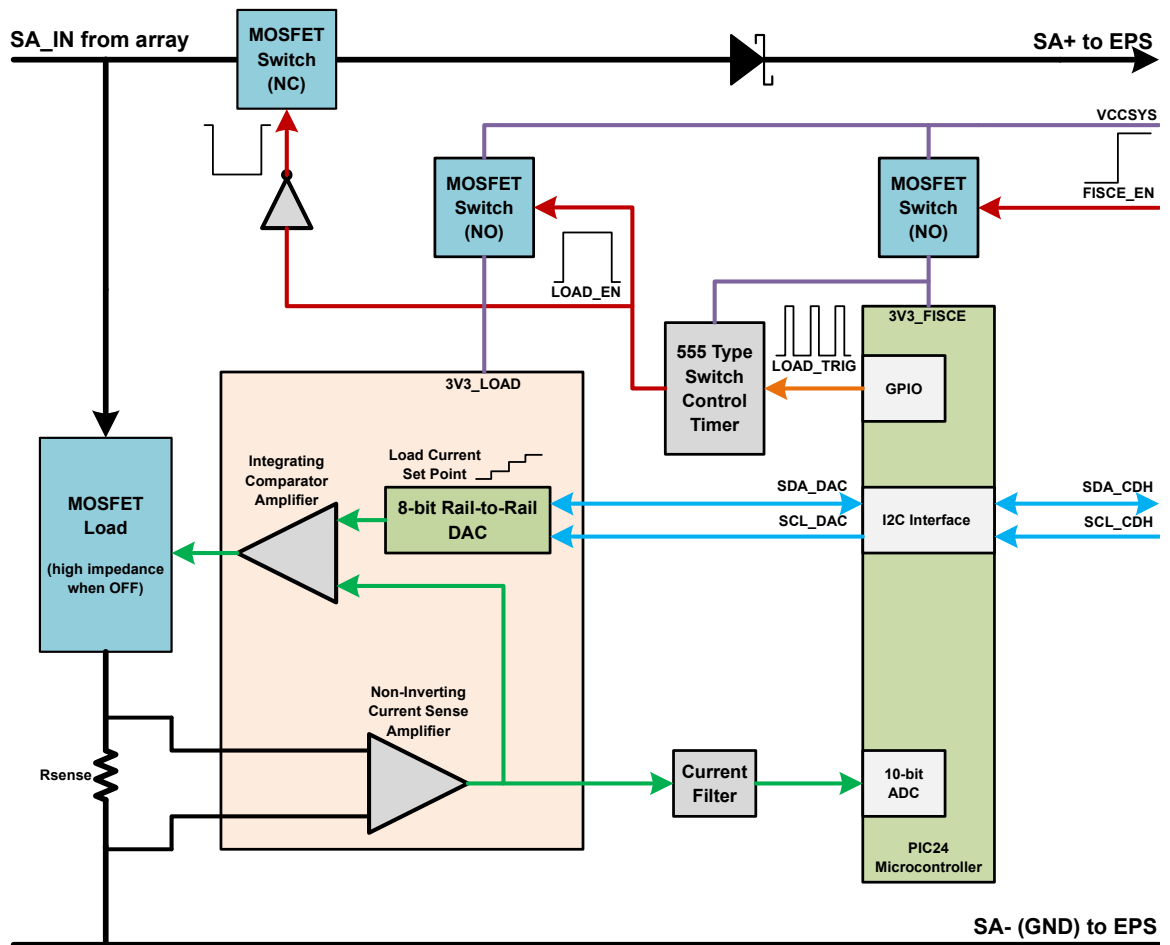


Figure 3.1: This block diagram represents the components of the FISCE load circuit and their functions.

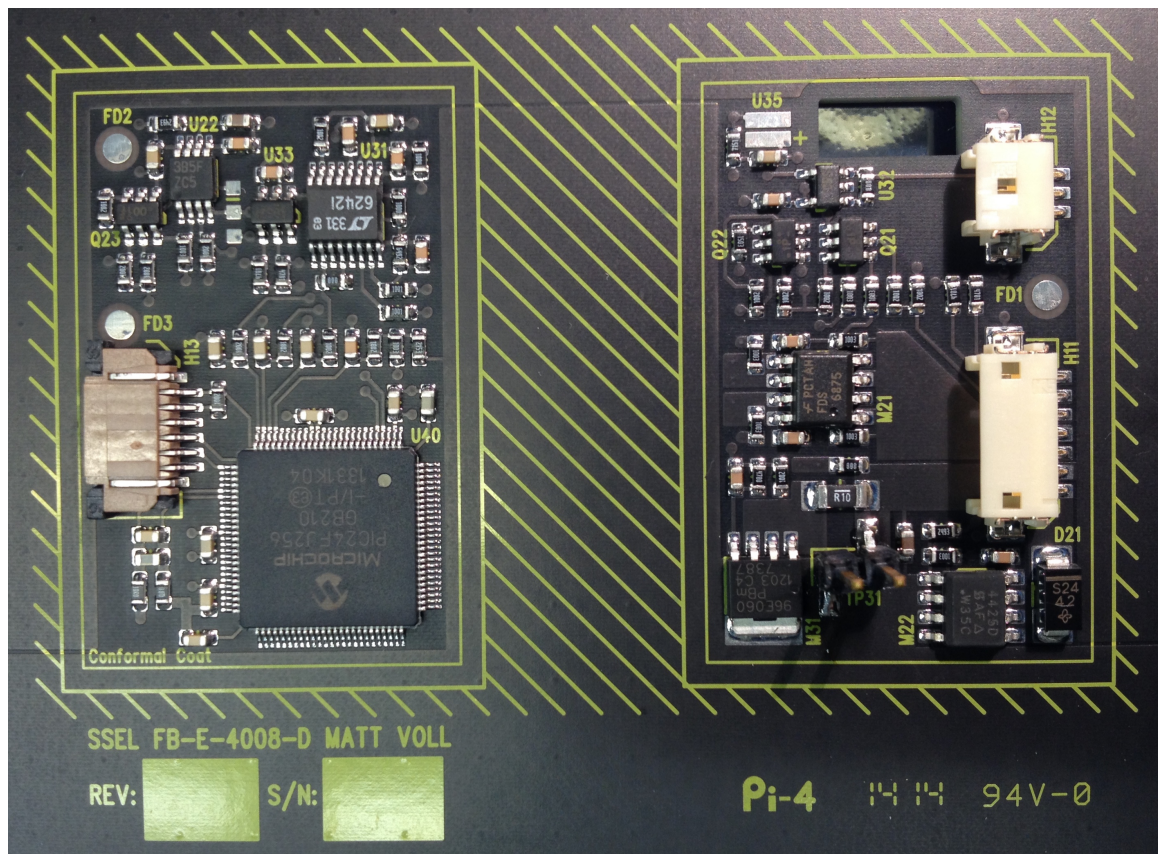


Figure 3.2: The assembled FISCE load circuit on the backside of the solar panel substrate.

DESIGN METHOD EXAMPLE: ELECTRICAL POWER SUBSYSTEM

This subsystem was designed to facilitate expanded capabilities of the IT-SPINS mission. Building on successes of the electrical power subsystem (EPS) used for the FIREBIRD-II mission, the design of an updated version of the Phoenix EPS began in the Spring of 2016. The original design came out of necessity, and began a trend of using SSEL developed subsystems for CubeSat missions rather than purchasing and integrating off-the-shelf solutions.

This chapter provides an investigation of how IT-SPINS mission requirements made a significant overhaul of the Phoenix EPS mandatory. Then, a conceptual design that incorporates those requirements is presented. With a block diagram in place, several circuit simulations and calculations were performed to verify that components of the design would operate as intended once built. The method used in this example effectively used a hierarchical schematic structure to reuse several “blocks” and make the schematic less cluttered. However, simulations were not well integrated into the design flow and were difficult to track as the design matured; if a simulation was modified or updated the corresponding schematic changes had to be done manually. Similarly, support documents such as connector pin reference tables were in a constant state of flux as the design progressed.

Figure 4.1 is an overview of the processes involved in designing the Phoenix EPS. Ideally, these steps would be linked in only a linear progression, i.e. each step would need to be completed and approved before moving onto the next. The arrows show that during the simulation and schematic entry phases there was a need to revise the subsystems requirements and conceptual design material. Also, there was essentially only one formal approval step, made when the PCB was fully laid out and ready for fabrication.

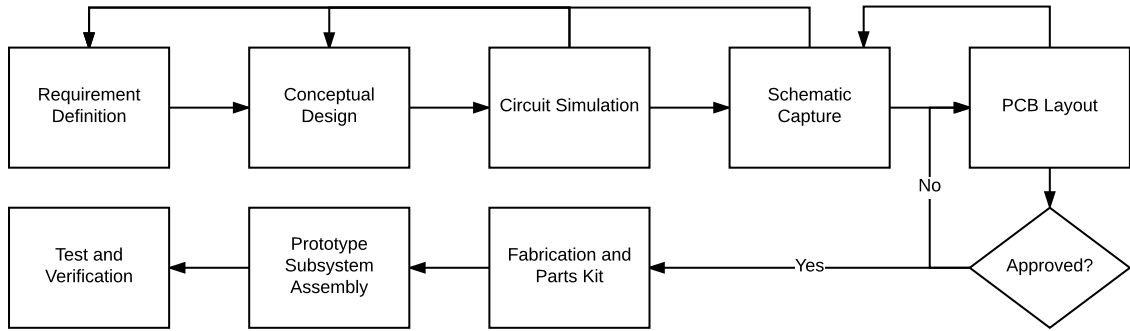


Figure 4.1: A simplified representation of the design method used in this chapter.

Requirements and Conceptual Design

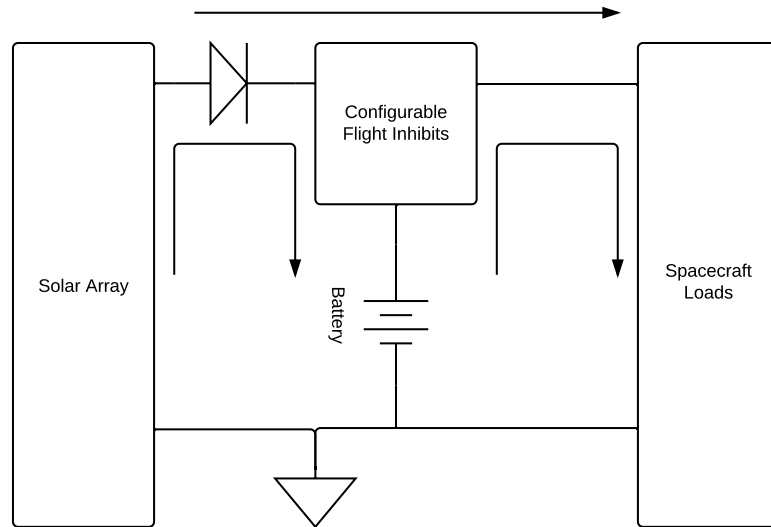


Figure 4.2: Basic configuration of a direct energy transfer (DET) power subsystem, with primary current paths shown by arrows.

Each resistor shown indicates a critical current sense location that is used to monitor the subsystem’s status and performance. The inhibit switches shown indicate the locations at which the power path is broken for “safing” the satellite during test and launch; the physical switches are not located on the

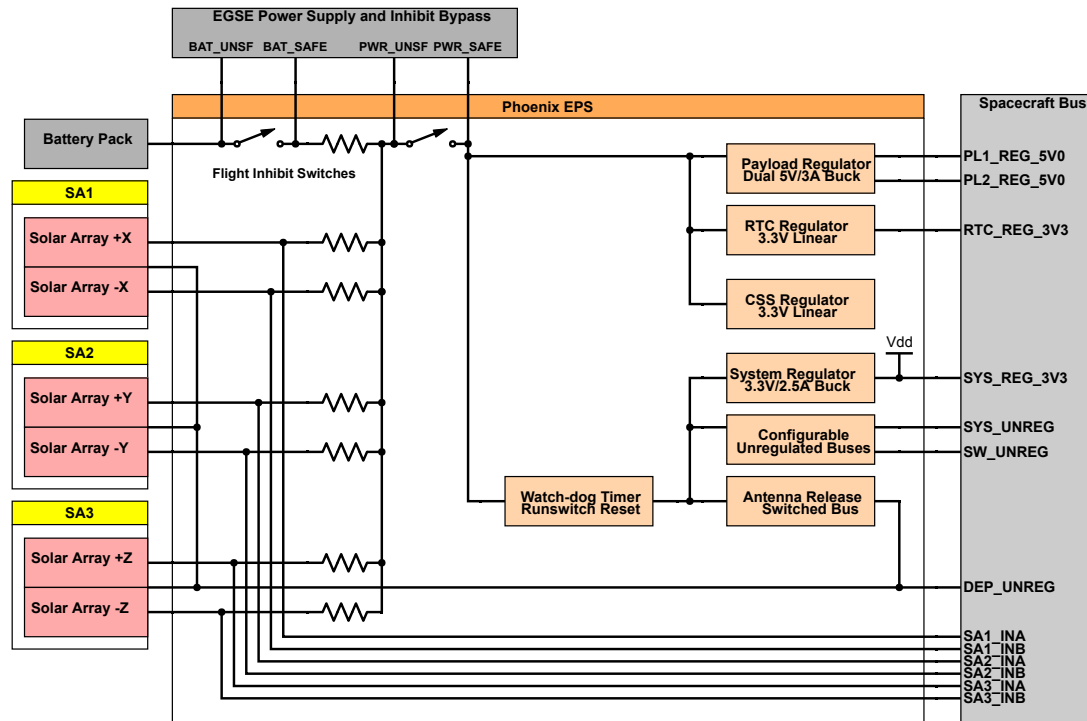


Figure 4.3: Components of the Phoenix EPS and the connections that form the PDN of the spacecraft.

A1 SFC_I2C	SFC_I2C A2	GND B1	GND	GND B2	GND
A3 SFC_I2C	SFC_I2C A4	SA1_INA B3	SA B4	SA B4	SA1_INA
A5 SFC_SPI	SFC_SPI A6	SA1_INB B5	SA B6	SA B6	SA1_INB
A7 SFC_SPI	SFC_SPI A8	SA2_INA B7	SA B8	SA B8	SA2_INA
A9 SFC_SPI	SFC_IO A10	SA2_INB B9	SA B10	SA B10	SA2_INB
EPS_SDA A11	EPS_I2C A12	SA3_INA B11	SA B12	SA B12	SA3_INA
EPS_IRQ A13	EPS_I2C A14	SA3_INB B13	SA B14	SA B14	SA3_INB
WDT_MON A15	EPS_IO A16	GND B15	GND	GND B16	GND
COMM_BIAS A17	COMM_IO A18	PL1_REG_5V0 B17	PL1 B18	PL1 B18	PL1_REG_5V0
A19 COMM_UART	COMM_UART A20	B19 PL1	PL1 B20	PL1 B20	PL1
A21 PL1_UART	PL1_UART A22	GND B21	GND	GND B22	GND
A23 PL1_IO	PL1_IO A24	PL2_REG_5V0 B23	PL2 B24	PL2 B24	PL2_REG_5V0
A25 PL1_IO	PL1_IO A26	PL2_MAG_3V3 B25	PL2 B26	PL2 B26	PL2_MAG_3V3
PL2_TLM A27	PL2_UART A28	SYS_REG_3V3 B27	SYS B28	SYS B28	SYS_REG_3V3
CSS1A A29	PL2_AN A30	GND B29	GND	GND B30	GND
CSS2A A31	PL2_AN A32	GND B31	GND	GND B32	GND
CSS3A A33	PL2_AN A34	PWR_SAFE B33	FSW B34	FSW B34	PWR_SAFE
A35 PL2_SPI	PL2_SPI A36	PWR_UNSF B35	FSW B36	FSW B36	PWR_UNSF
A37 PL2_SPI	PL2_SPI A38	BAT_SAFE B37	FSW B38	FSW B38	BAT_SAFE
A39 PL2_SPI	PL2_SPI A40	BAT_UNSF B39	FSW B40	FSW B40	BAT_UNSF
GSE_TLM A41	GSE_UART A42	GND B41	GND	GND B42	GND
GSE_PGED A43	GSE_PROG A44	DEP_UNREG B43	SYS B44	SYS B44	DEP_UNREG
GSE_RESET A45	GSE_IO A46	SYS_UNREG B45	SYS B46	SYS B46	SYS_UNREG
GSE_SEL0 A47	GSE_IO A48	SW_UNREG B47	SYS B48	SYS B48	SW_UNREG
GSE_SEL2 A49	GSE_IO A50	RTC_REG_3V3 B49	RTC B50	RTC B50	RTC_REG_3V3
RSW_INHIBIT A51	GSE_IO A52	GND B51	GND	GND B52	GND

Figure 4.4: New connector pinouts.

GSE_SEL2	A1	GSE_IO		GSE_IO	B1	GSE_SEL3
GSE_SEL0	A2	GSE_IO		GSE_IO	B2	GSE_SEL1
GSE_RESET	A3	GSE_IO		GSE_IO	B3	GSE_DISARM
GSE_PGED	A4	GSE_PROG		GSE_PROG	B4	GSE_PGEC
GSE_TLM	A5	GSE_UART		GSE_UART	B5	GSE_CMD
PL2_TLM	A6	PL2_UART		EPS_IO	B6	EPS_RESET
GSE_SDA	A7	EPS_I2C		EPS_I2C	B7	GSE_SCL
SYS_REG_3V3	A8	SYS		GND	B8	GND
RSW_INHIBIT	A9	INHIBIT		INHIBIT	B9	BAT_INHIBIT
PWR_SAFE	A10	FSW		GND	B10	GND
PWR_SAFE	A11	FSW		GND	B11	GND
PWR_UNSF	A12	FSW		GND	B12	GND
PWR_UNSF	A13	FSW		GND	B13	GND
BAT_SAFE	A14	FSW		GND	B14	GND
BAT_SAFE	A15	FSW		GND	B15	GND
BAT_UNSF	A16	FSW		GND	B16	GND
BAT_UNSF	A17	FSW		GND	B17	GND

Figure 4.5: New connector pinouts.

BATTERY						
GND	A1	GND		PWR	B1	BAT_UNSF
GND	A2	GND		PWR	B2	BAT_UNSF
BAT_INHIBIT	A3	INHIBIT		TMON	B3	BAT_TMON
GND	A4	GND		UNREG	B4	SYS_UNREG
BAT_SDA	A5	SDA		SCL	B5	BAT_SDA

INHIBITS						
PWR_UNSF	A1	PWR		PWR	B1	PWR_SAFE
PWR_UNSF	A2	PWR		PWR	B2	PWR_SAFE
FSWA_C	A3	MON		MON	B3	FSWB_C
BATT_SAFE	A4	PWR		PWR	B4	BATT_UNSF
BATT_SAFE	A5	PWR		PWR	B5	BATT_UNSF

SOLAR ARRAYS[1..3]						
GND	A1	GND		PWRA	B1	SA_INA
GND	A2	GND		PWRA	B2	SA_INA
GND	A3	GND		CSSA	B3	CSSA_IN
GND	A4	GND		DEP	B4	DEP_UNREG
GND	A5	GND		CSSB	B5	CSSB_IN
GND	A6	GND		PWRB	B6	SA_INB
GND	A7	GND		PWRB	B7	SA_INB

Figure 4.6: New connector pinouts.

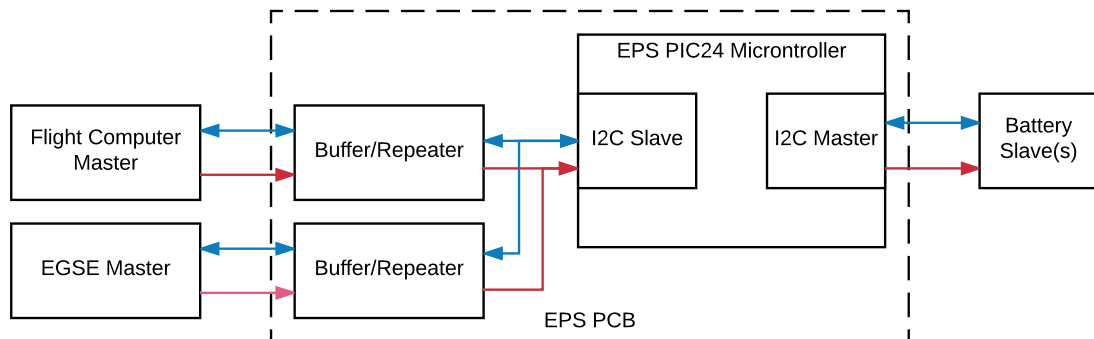


Figure 4.7: New connector pinouts.

Circuit Simulations and CalculationsPCB Layout and Mechanical DesignLessons Learned and Future Work

In this case, there were several times when the requirements, conceptual design, schematic, and PCB layout were all being updated and altered in parallel. As the IT-SPINS mission and the operation of its subsystems became more fully defined, the critically important EPS design had to be altered to maintain compatibility. In hindsight, these changes made the design method seem somewhat chaotic when

DESIGN STUDY - ELECTRICAL GROUND SUPPORT EQUIPMENT

This is the VOID EGSE design example.

Requirements and Conceptual Design

Circuit Simulations and Calculations

PCB Layout and Mechanical Design

Lessons Learned and Future Work

FUTURE METHODS

Investigating the possible methods for future use.

CONCLUSION

\LaTeX produces documents that look great, automatically handles references and citations, and easily incorporates figures and tables. This is not a guide to \LaTeX but rather an introduction to the MSU style. If you want more information about \LaTeX many introductory guides can be found online.

REFERENCES CITED

APPENDICES

APPENDIX A

EXAMPLE CODE

% MATLAB code to say 'hello world'

disp('Hello world')

APPENDIX B

EXAMPLE SCHEMATIC