Nonconformance Report

Incident Date:	04/22/2014
NCR Number	

Subsystem	Part/Document Name	No. of NCR Sheets
EPS	FISCE Solar Panel Schematic and Layout	

Brief Description

During initial EDU testing on the FISCE solar panel, odd behavior was observed on the Q23 transistor. This transistor is a dual NPN/PNP type FMB2227A BJT. The NPN gate of Q23 is used to pull the TRIG pin of the 555 timer LOW with a series of pulses from the MCU. It was observed that the TRIG remained in its default HIGH state even though the correct pulse signal from the MCU was driving the gate. Because of this, the load never turned on.

MPS Number	MPS OP Number	Hardware Type
		☐ Flight ☐ Flight Qualification ☐ Non-Flight ☑ ETU
Quantity	**Procedure Number**	**Found During**
		FISCE Test Plan

Reference Documents

FB-E-4007-D, FB-E-4008-D (see FISCE_Documentation.zip on Knowledge Tree pending releases)

Analysis (Attach additional pages if necessary)

The NPN gate of Q23 is used to pull the TRIG pin of the 555 timer LOW with a series of pulses from the MCU. It was observed that the TRIG remained in its default HIGH state even though the correct pulse signal from the MCU was driving the gate. When working correctly, the 555 timer output should go HIGH and stay there until the series of pulses from the MCU stops, at which point the 555 timer expires and the output goes LOW. The 555 output signal controls the 3V3_LOAD and SA+ power switches.

First, the orientation of the 6-pin SOT package of Q23 was checked and found to be correct. Then, the pin sequence of the schematic was compared to the FMB2227A datasheet. It was found that pins 1 and 5, the base and emitter of the NPN gate (Q23-A) respectively, had been reversed. The same issue was also found on the other two dual transistors, both of which are dual NPN type FMB2222A BJT's.

After looking at the part type and schematic decals in the PADS design file, it was found that the naming scheme for the part gates had caused PADS to automatically change the pin numbering sequence of the part when saved. This meant that even though the pin numbers were entered correctly at first, the final schematic netlist used for the FISCE layout had incorrect pin numbers (pins 1 and 5 switched) for all 3 of the board's dual BJT parts: Q21, Q22, and Q23.

Proposed Corrective Action

There is a total of 6 pins on the FISCE board that are connected incorrectly in the layout of the circuit. These are all low-current control signals located on SOT23-6 packages. The proposed action is to attempt to cut the 6 traces in the PCB and solder small gauge fly-wires between each of the pins and their correct connection point. Conveniently, each pin has a resistor nearby that may act as viable solder point for the fly-wires. See the attached schematic sheet and FMB2222A/2227A datasheets for details on the pin discrepancies.

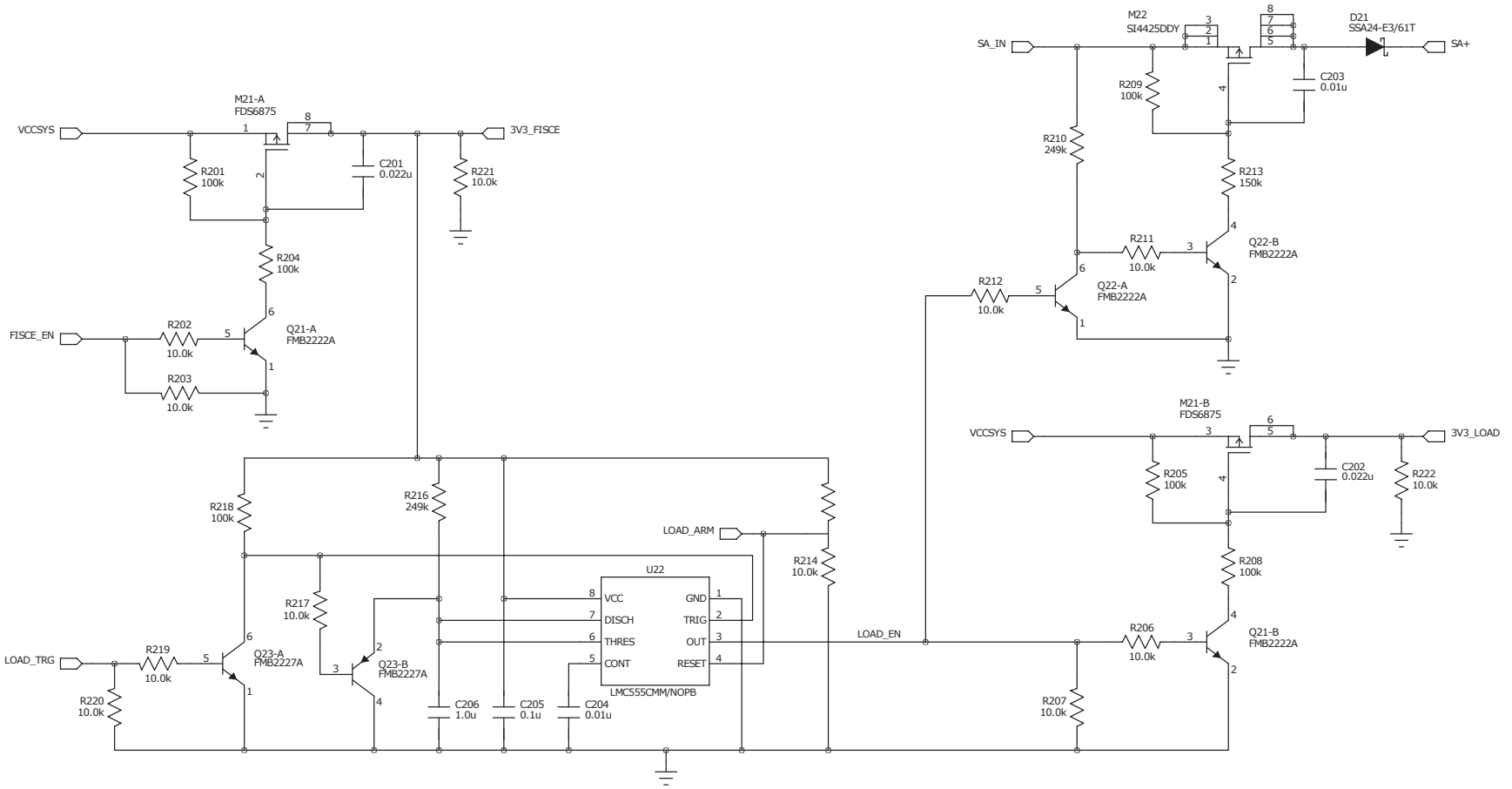
The alternative action would be to make the changes in the layout and spin a new set of 4 FISCE PCB's. This may delay our shipment to Vanguard of the completed/tested boards by at least a week.

RE Discipline Date	PM Date

Corrective Action Taken

QA Date	PM Date

Additional comments to be attached on a separate sheet



<Author/RE> Matt Voll <Sig>	DATED: 02/20/2014	COMPANY: Space Science & Engineering Lab
<Reviewed By 1> <Sig>	DATED:	TITLE: FISCE Instrument Solar Panel Schematic
<Reviewed By 2> <Sig>	DATED:	DOCUMENT NO: FB-E-4007-D / REV: 1.0
<Approved By> <Sig>	DATED:	SHEET NAME: POWER_SWITCH / SIZE: B SHEET: 2 OF 4

FAIRCHILD SEMICONDUCTOR®

August 2013

FFB2227A / FMB2227A
NPN & PNP General-Purpose Amplifier

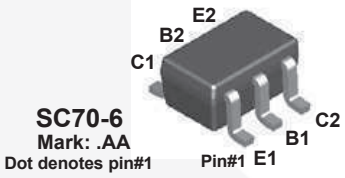
Description

This complementary device is a medium-power amplifier and switch, requiring collector currents up to 500 mA. Sourced from Process 19 and 63. See FFB2222A (NPN) and FFB2907A (PNP) for characteristics.

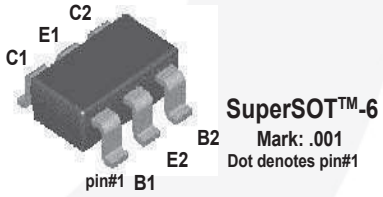
Ordering Information

Part Number	Top Mark	Package	Packing Method
FFB2227A	AA	SC70 6L	Tape and Reel
FMB2227A	001	SSOT 6L	Tape and Reel

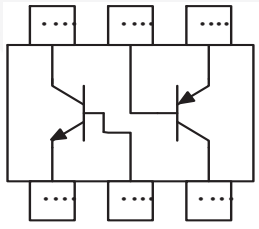
Block Diagram



FFB2227A Device Package

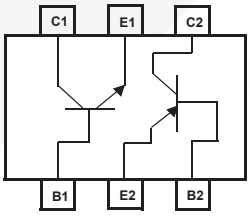


FMB2227A Device Package



FFB2227A Internal Connection

TRANSISTOR TYPE	
C1 B1 E1	NPN
C2 B2 E2	PNP

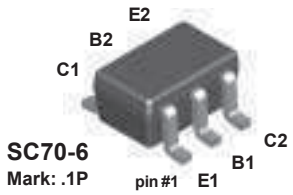


FMB2227A Internal Connection

Figure 1. Block Diagram

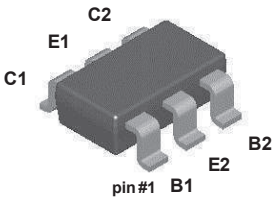
FAIRCHILD
SEMICONDUCTOR™

FFB2222A FMB2222A MMPQ2222A

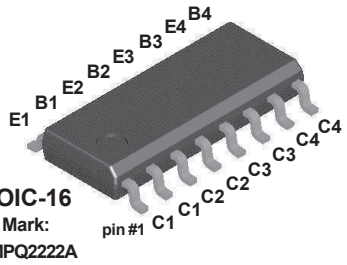


SC70-6
Mark: .1P

NOTE: The pinouts are symmetrical; pin 1 and pin 4 are interchangeable. Units inside the carrier can be of either orientation and will not affect the functionality of the device.



SuperSOT™-6
Mark: .1P
Dot denotes pin #1



SOIC-16
Mark:
MMPQ2222A

NPN Multi-Chip General Purpose Amplifier

This device is for use as a medium power amplifier and switch requiring collector currents up to 500 mA. Sourced from Process 19.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	75	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	500	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		FFB2222A	FMB2222A	MMPQ2222A	
P_D	Total Device Dissipation Derate above 25°C	300 2.4	700 5.6	1,000 8.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Effective 4 Die Each Die	415	180	 125 240	°C/W °C/W °C/W

Proposed FISCE board modifications. RED lines indicate cut traces, GREEN lines indicate suggested fly-wire attachments.