On-Orbit Annealing of Satellite Solar Panels

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ABSTRACT

An approach to extend the life of orbiting satellites is presented. Since output power of spacecraft solar panels plays a major role in determining the end of life of the satellite, any attempt to recover any of this lost power would be very attractive. The goal of this research was to investigate the possibility of annealing radiation damaged solar panels under conditions that would be feasible to apply in orbiting spacecraft. Preliminary data of a technique called forward biased current annealing of GaAs cells is presented and shows promising results at a moderate temperature.

An autonomous microprocessor controlled experiment to carry out these tasks is also presented. The experiment is currently capable of monitoring and accurately recording different cell performance including their IV characteristics. With simple modifications to this circuit the system can be designed to perform current annealing of different array cells.

INTRODUCTION

Solar energy has been and will continue to be the primary source of power on nearly all earth orbiting spacecrafts. Photovoltaic devices, primarily solar cells, have proven to be a simple and reliable mechanism for the conversion of the suns radiant energy to usable electrical energy.

Typical solar array subsystems are designed to provide adequate power to the spacecraft through the End-of-Life (EOL), which can be as long as ten years. Due to the harsh space environment on orbiting satellites, they are continuously subjected to radiation from geomagnetically trapped protons and electrons and from solar flare protons. These radiant particles damage the solar cells resulting in decreased cell efficiencies with an overall reduction in available output power. This has always presented a problem for designers of space power systems. The traditional solution to this problem has been to combine the use of radiation absorbing cover glasses with a degree of overdesign for EOL derating. That is to say, to meet the EOL power requirements, solar arrays are designed to provide more power than necessary to account for radiation degradation and other degrading effects. Thus, Beginning-of-Life (BOL) generated power is normally more than needed and usually is wasted. New requirements for higher power systems make this approach very expensive in both launch weight and component cost.

Attempts to minimize the quantity of solar cells required at BOL have been primarily concentrated in the areas of radiation hardening of the cells or their cover material, in the development of more efficient cells and to some extent the annealing of cell arrays.

Gallium Arsenide (GaAs) cell were found to be an attractive alternative to currently used silicon cells due to their higher efficiencies, their radiation resistance and their ability to be easily annealed.

Currently, the Naval Postgraduate School is conducting research in the areas of testing and annealing of solar arrays. Research has developed to the stage that a serious on-orbit annealing experiment is being prepared.

GALLIUM ARSENIDE CELLS

Radiation degraded silicon solar cells, experience significant thermal annealing at temperatures ranging from 450 to 550 degrees C. (1) This high temperature would be extremely difficult to generate on orbit and it tends to damage the contacts and cover material of the cells.

Gallium arsenide cells, on the other hand, thermally anneal in the vicinity of 200 degrees C. (Stages of recovery have been

reported by Yamaguchi, et al, (2) to be 150-200, 250-300 and 400 to 500.) Nonetheless, 200 degrees is still a difficult barrier to reach on-orbit.

Continuing research at NPS has shown that by forward biasing a GaAs cell with .75 amperes of current and maintaining temperature at 90 to 100 degrees C for between 6 and 42 hours, cell that have been irradiated with 1-Mev electrons to fluence levels of 3e15 electrons/cm2 and have originally lost 40% of their original efficiency, recover approximately 33% of that lost efficiency. (Figures 1,2). (3,4)

The promising aspect of these results is that the required temperature is easily achieved on-orbit and the current required will not place a major burden on the satellite power supply. In fact, since .7 amperes is the equivalent output of about 7 cells, part of an arrays power can easily be shunted to anneal another portion of the same array.

SOLAR ARRAY IV TESTER

The requirement to test solar cells on-orbit led to the development of a novel circuit which is both fast and extremely accurate. This circuitry is based on the fact that a bipolar junction transistor models an ideal current source. Therefore, the idea to use it to control the output current of a solar cell will allow the user to measure accurately the short-circuit current (Isc) of the cell. Also measuring different currents and their corresponding voltage would be easy by changing the current using the transistor base as the control.

A description of this circuit in its simplest form has 5 volts placed on the anode of the solar cell which has its cathode tied to the collector of a 2N3405 transistor. The emitter of the transistor is connected to ground through a 10 ohm resistor. The base is stepped through voltages to bias the transistor from cutoff through the active region. By simultaneously measuring the voltage across the solar cell and the voltage across the emitter resistor, the corresponding values of the cell VI characteristics can be recorded. This is true since using a high beta 2N3405 transistor (~400) would allow us to ignore the base current. Thus we can use the measured values of the current in the emitter resistance as the collector current or the solar cell current.
Proof of concept has been completed with the design of a Motorola 6803 microcomputer based IV curve generator. (Figures 3,4,5,6,7) The 6803 drives a digital to analog converter which provides the current to the base of each transistor through an analog multiplexer which selects the cell to be tested. As the transistors base is stepped, a differential amplifier senses the voltage across cell which is converted to digital using an 8-bit analog to digital converter. Simultaneously, the voltage is measured at the emitter by another A to D converter. These results are stored in RAM until all cells are tested and then the

serial port on-board the 6803 transmits the points for each curve to an IBM PC. The hexadecimal dump is converted to decimal, the current is calculated and the curve is plotted. (Figure 8) Note in this figure that the IV curve generated using this method enjoys a much sharper knee in the area of the maximum power point of the cell. This indicates clearly that this IV measuring technique contributes a smaller series resistance and a large parallel leakage resistance than the typical measuring setup. point of the cell. This circuit is calculated to be accurate to within 5 millivolts and 1 milliamp of actual values using 8 bit A to D's and D to A's.

The determination of the maximum power point will be used in the algorithm for energizing anneal circuitry in the on-orbit experiment.

RE-ANNEALING OF GALLIUM ARSENIDE SOLAR CELLS

Past experience has shown that if a GaAs cell is irradiated to a high level of degradation without annealing, the percentage of possible recovery when annealed is limited. The research currently in progress at NPS is centered around a single assumption. That is, we believe that if a cell is only permitted to receive light degradation prior to an anneal cycle, the cell will continually anneal to within 90 percent of its previous value. The idea is that if the array is annealed at each solar maximum, (every 3 months or so), we can expect a stair step effect on the Pmax of the cell.

CONSTRUCTION OF EXPERIMENT

The NPS solar experiment is being designed for accuracy and compactness. The computer controller used .25 amperes during IV testing cycles and 25% less while in "wait state". Its size when not in a hardened case is 3x4.5x1.5 inches. The test array will consist of 8 cells. With a simple modification to the test circuit, it can be designed to steer annealing currents to proper cells as well as recording their response.

CONCLUSIONS

The research required to produce an on-orbit annealing experiment has led to some interesting results.

1) Forward biasing of a gallium arsenide solar cell with .75 amp of current allows significant annealing to occur at a temperature of approximately 90 degrees C.

2) An extremely portable, low power IV tester has been developed for determining the complete IV curve of a single cell or array of cells.

3) Research in progress is expected to prove the assumption that if a cell is not permitted heavy degradation it can continually be annealed to within 90 percent of its previous efficiency.

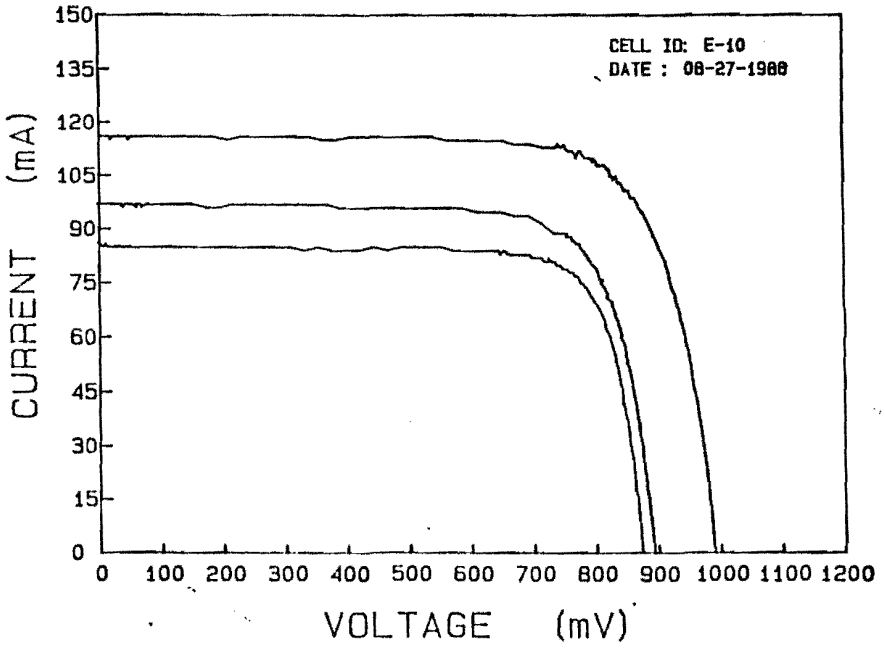
REFERENCES

1. W.E. Horne, A.C. Day and M.A. Thompson, "Burst Annealing of Proton Damage In Silicon Solar Cells," in Seventeenth IEEE Photovoltaic Specialists Conference, pp. 1097-1102, 1984.

2. Masufumi Yamaguchi and Chikara Amano, "Cobalt 60 gamma-ray and Electron Irradiation Damage of GaAs Single Crystals and Solar Cells", Journal of Applied Physics, Vol 54, No.9, pp. 5021-5029, September 1983.

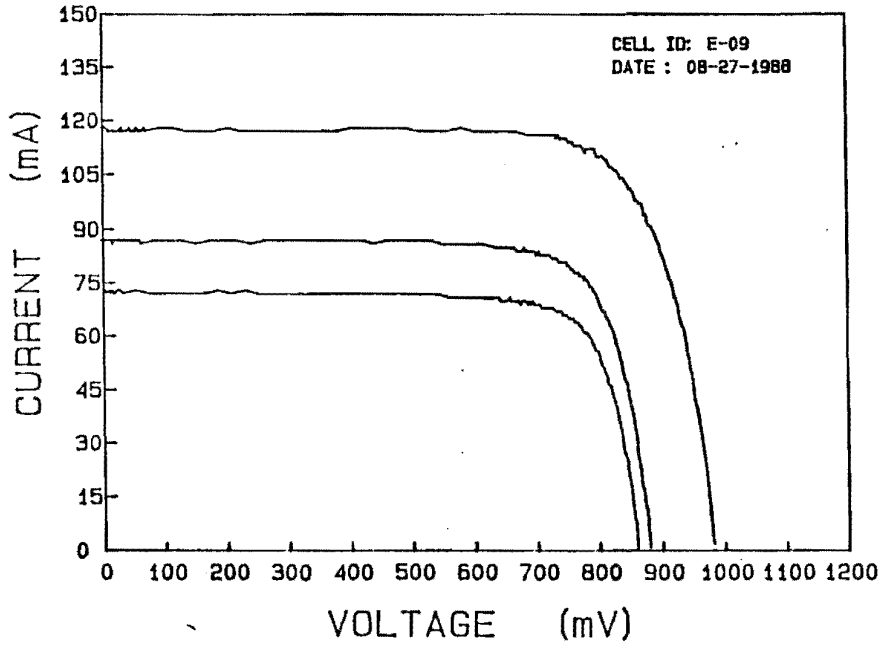
3. Staats, Richard L., "Forward-Biased Current Annealing of Radiation Damaged Gallium Arsenide and Silicon Solar Cells," Masters Thesis, Naval Postgraduate School, Monterey, California, March 1986.

4. Clark, T.F., "An Experimental Test of Minority Carrier Annealing On Gallium Arsenide Solar Cells Using Forward-Biased Current," Masters Thesis, Naval Postgraduate School, Monterey, California, September 1986.



IV Curves for GaAs Solar Cell Showing
Pre and Post Irradiation and Post Anneal Values

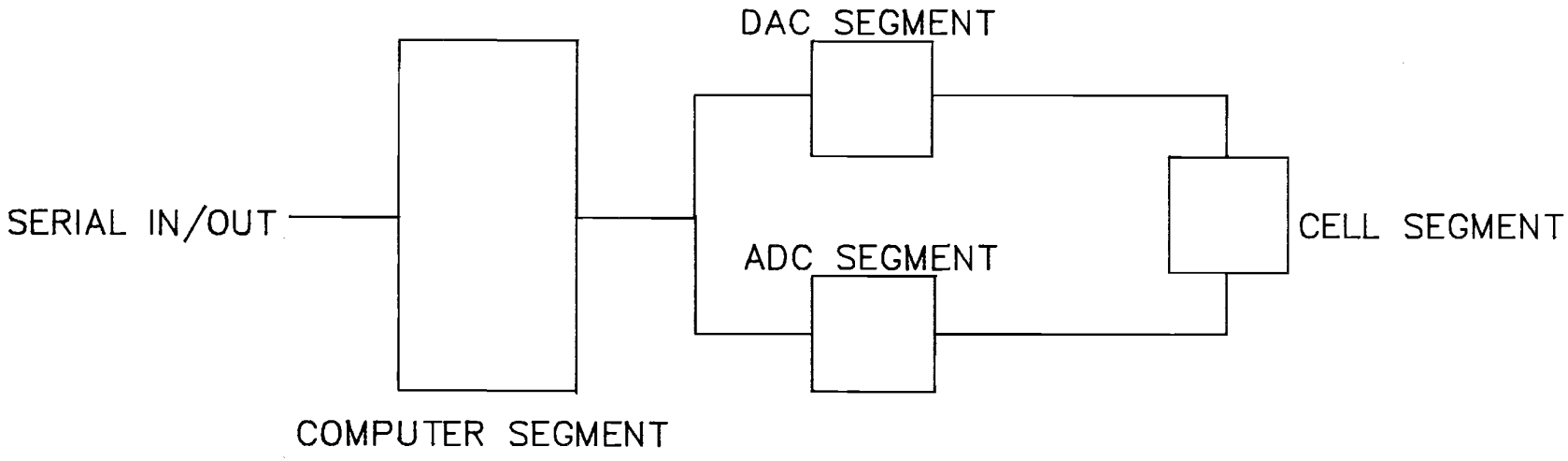
(Figure 2)



IV Curves for GaAs Solar Cell Showing
Pre and Post Irradiation and Post Anneal Values

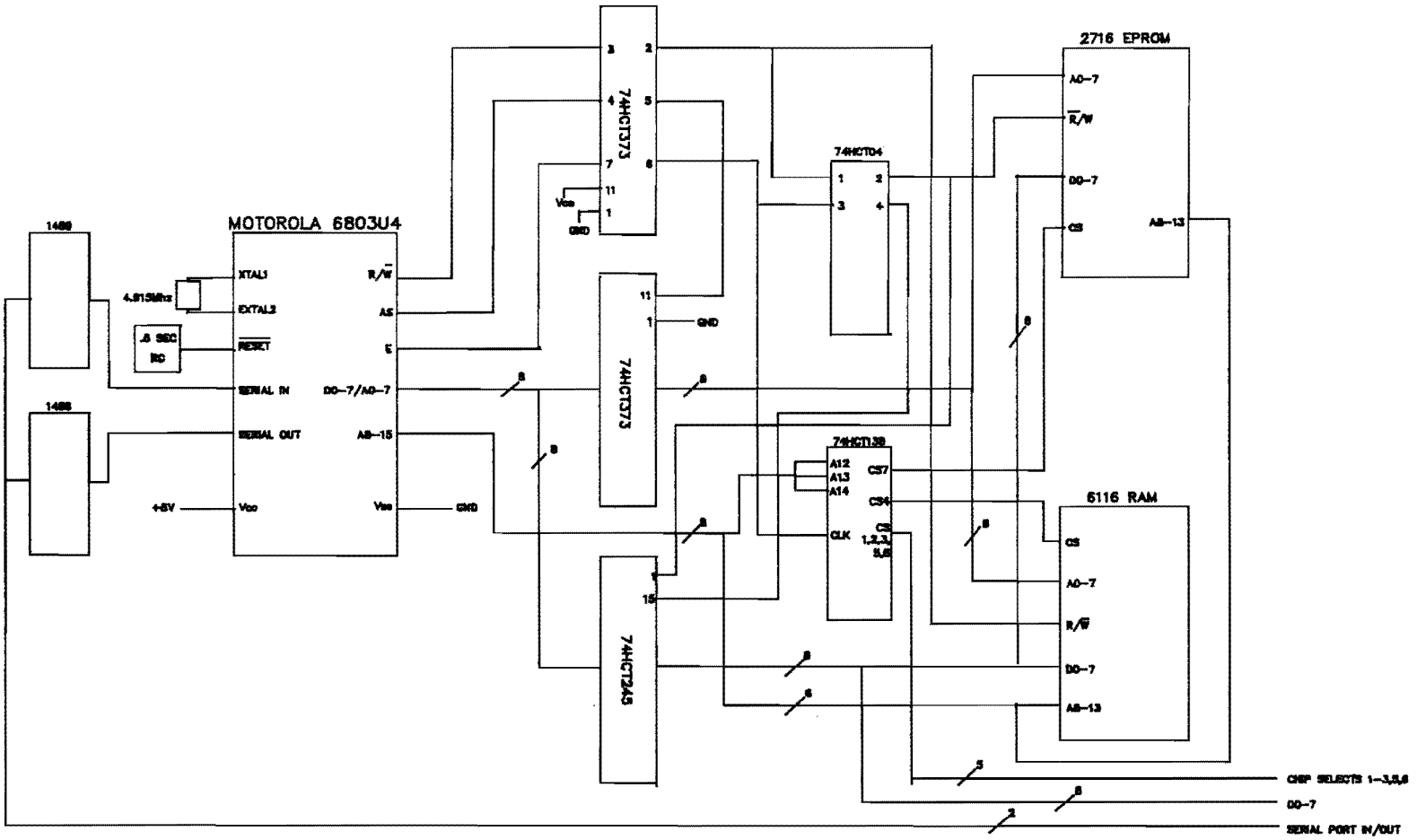
(Figure 1)

SOLAR CELL IV TESTER (BLOCK DIAGRAM)

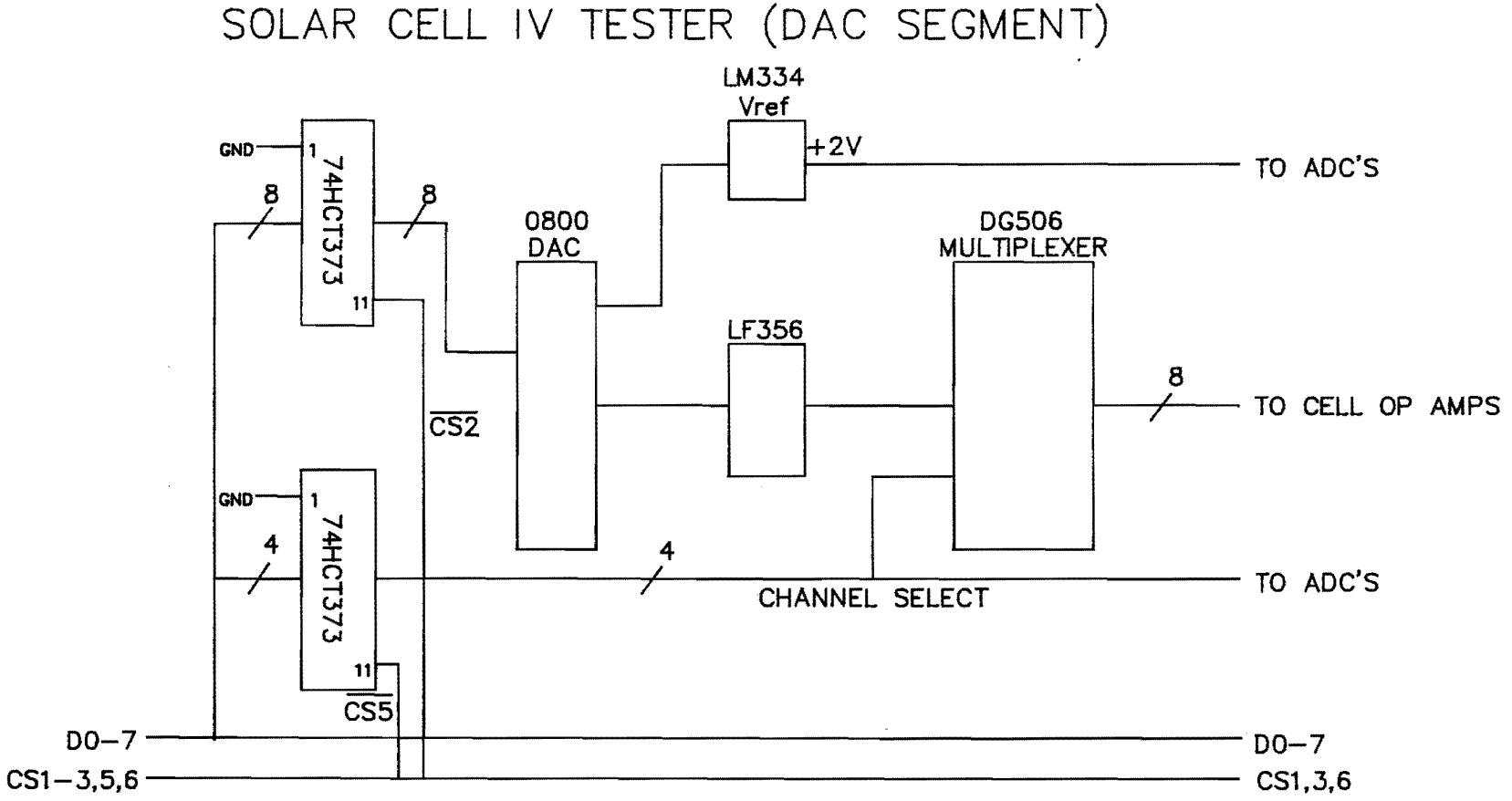


(Figure 3)

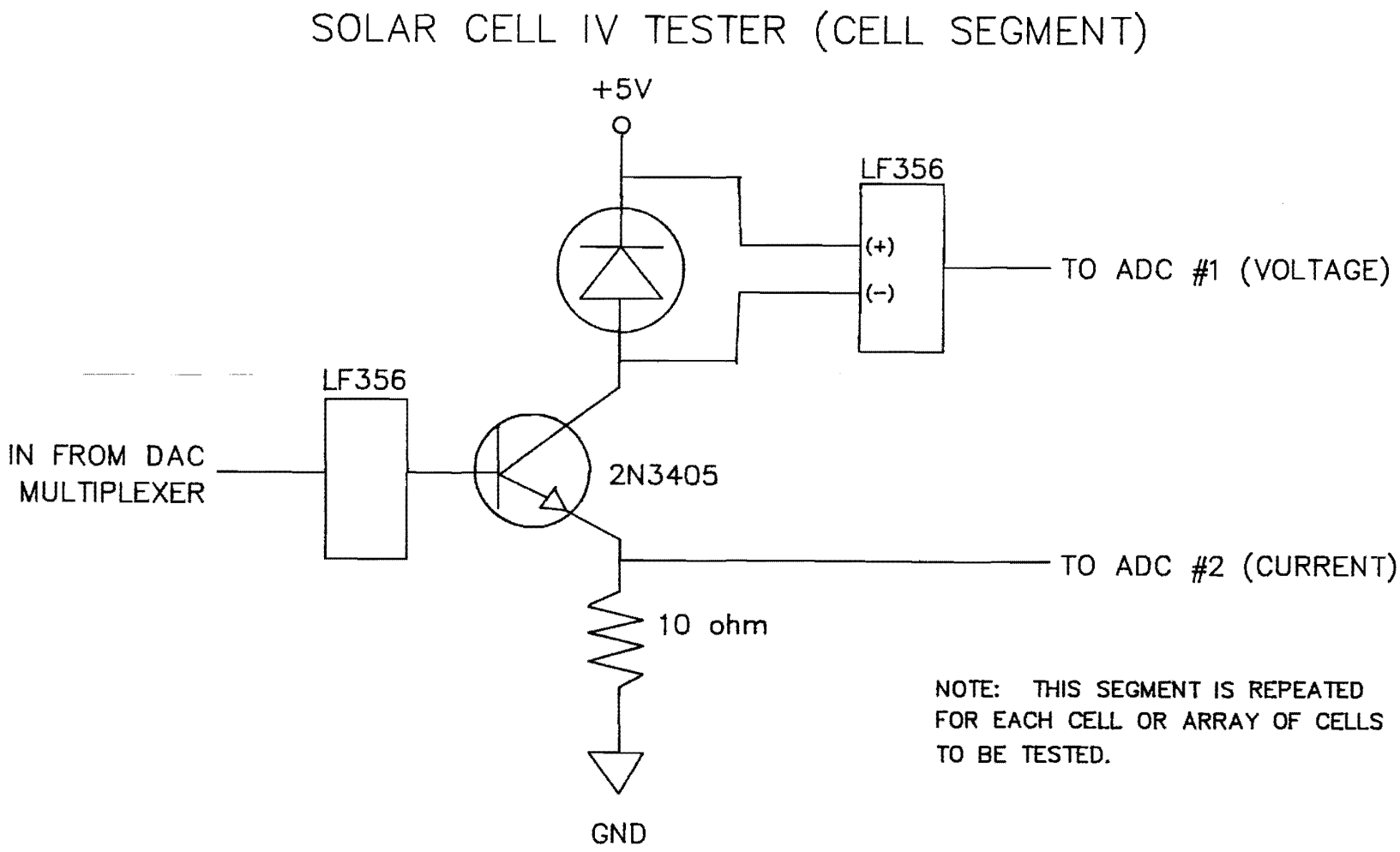
SOLAR CELL IV TESTER (COMPUTER SEGMENT)



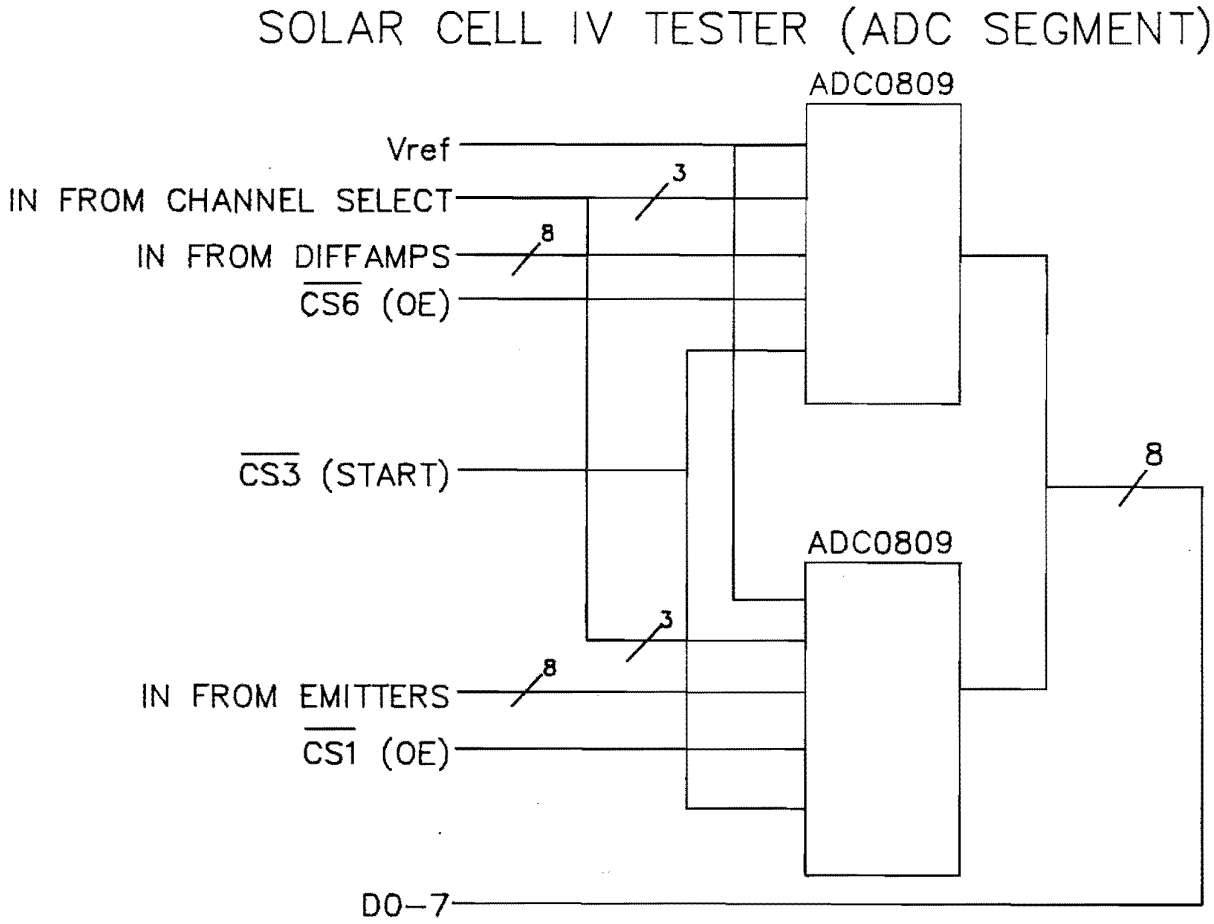
(Figure 4)


SOLAR CELL IV TESTER (DAC SEGMENT)
LM334
Vref
+2V
TO ADC'S
GND
1
74HCT373
11
8
8
0800
DAC
DG506
MULTIPLEXER
LF356
8
TO CELL OP AMPS
CS2
GND
1
74HCT373
11
4
4
TO ADC'S
CHANNEL SELECT
CS5
D0–7
D0–7
CS1–3,5,6
CS1,3,6

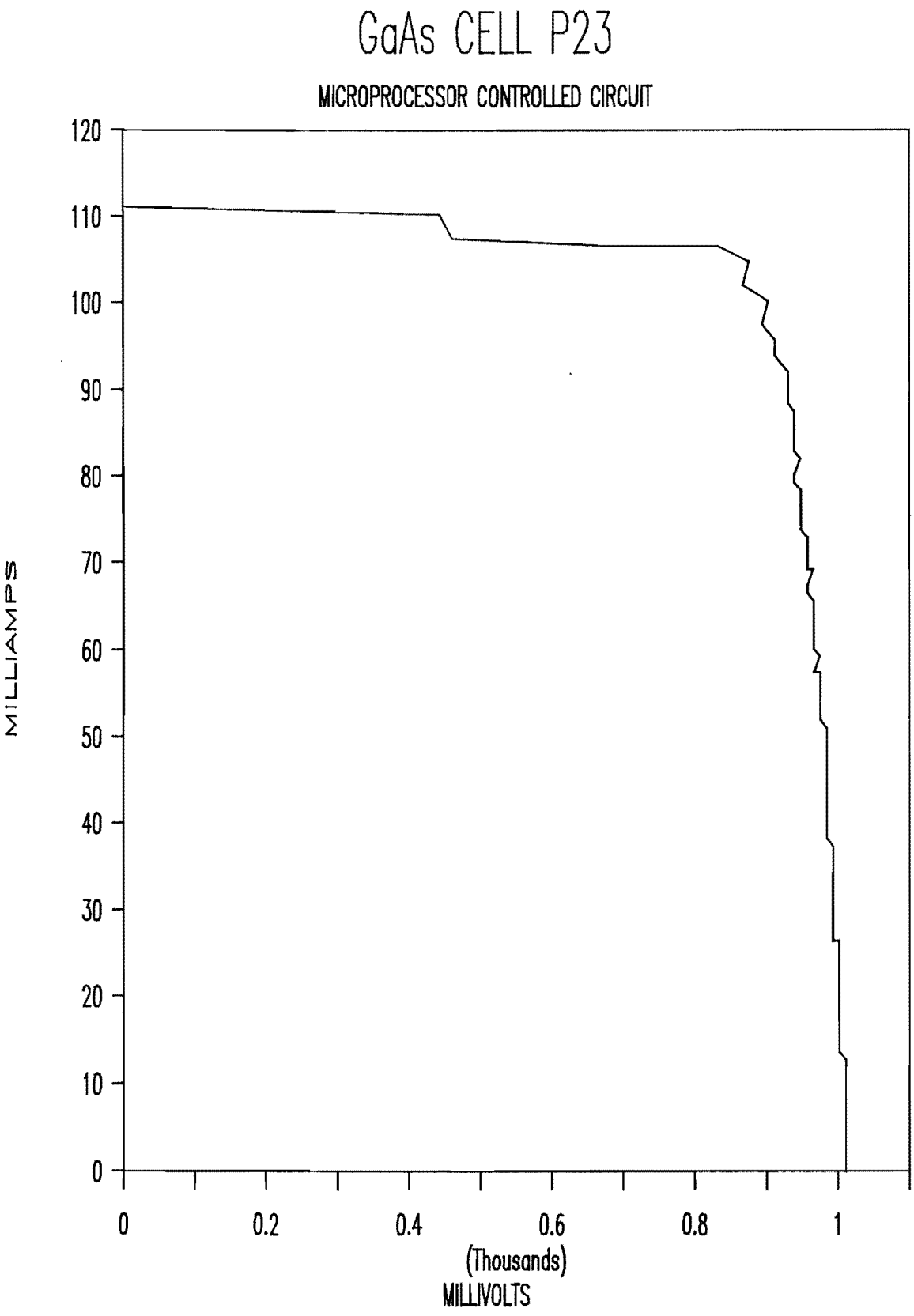
(Figure 5)


SOLAR CELL IV TESTER (CELL SEGMENT)
+5V
LF356
(+)
(-)
TO ADC #1 (VOLTAGE)
LF356
IN FROM DAC
MULTIPLEXER
2N3405
TO ADC #2 (CURRENT)
10 ohm
GND
NOTE: THIS SEGMENT IS REPEATED
FOR EACH CELL OR ARRAY OF CELLS
TO BE TESTED.

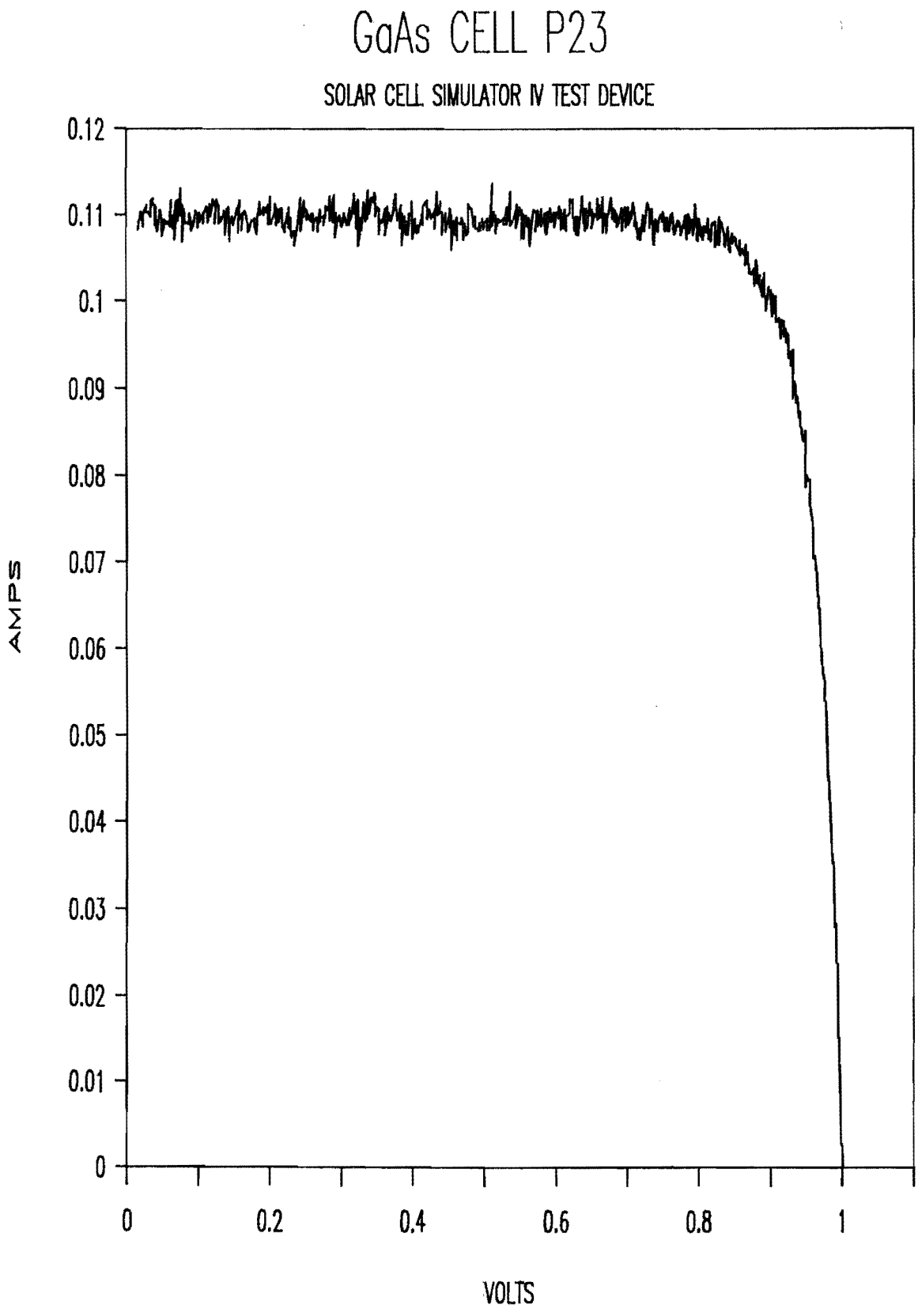
(Figure 6)


SOLAR CELL IV TESTER (ADC SEGMENT)
ADC0809
Vref
IN FROM CHANNEL SELECT
3
IN FROM DIFFAMPS
8
CS6 (OE)
CS3 (START)
8
ADC0809
3
IN FROM EMITTERS
8
CS1 (OE)
D0–7

(Figure 7)


GaAs CELL P23
MICROPROCESSOR CONTROLLED CIRCUIT
MILLIAMPS
120
110
100
90
80
70
60
50
40
30
20
10
0
0
0.2
0.4
0.6
0.8
1
(Thousands)
MILLIVOLTS

(Figure 8)


GaAs CELL P23
SOLAR CELL SIMULATOR IV TEST DEVICE
AMPS
0.12
0.11
0.1
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.2
0.4
0.6
0.8
1
VOLTS

(Figure 9)