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FREEDOM KW41Z
Bluetooth Smart/802.15.4/Generic FSK

Revisions & Change Log

Rev	Description	Date	Approved
X1	Initial Draft	10/22/15	A. QUIROZ
X2	Update connection/labels	11/30/15	A. QUIROZ
X3	BOM update	12/09/15	A. QUIROZ
A	RF BOM update, ADC selector added, VDD update U9 1-14, VDD update on U1 27-28	10/03/16	A. QUIROZ
A1	Update U9 1 and LED, add capacitor to V_EXT	06/20/16	SHAWN
A2	BOM update for C75, R85, R52	07/06/16	SHAWN
A3	BOM update for J1,J3 etc	07/21/16	SHAWN
B	1) Removed BATT_MONITOR net and R78 and replaced J35 with 1x2. 2) Made default power configuration buck mode. 3) Added transistors Q1, Q5, Q6, Q7 and respective resistors for LEDs to operate at 1.8V. 4) Removed resistors R71 and R76 5) Added J36 for processor supply options; replaced J23 with 1x2, replaced J18 with 1x3; changed J22 pins 1 and 2 connection to DCDC_IN; deleted V_MCU net, SH504 and TP13; added J37. 6) Updated J1-J4 pinout according to FRDM_KW40_512_Pinouts_V0_9. 7) Replaced the following connectors: J16,J17,J22 Changed to 210-81149 J23, J24, J35 Changed to 210-81176 8) Removed J27. 9) DNPed R7. 10) Split J22 into 3 1x2 headers and rearranged connections.	11/25/16	Jorge Ramirez
B1	1) Swapped PTC17 and PTC18 connections in U4.	01/10/17	Jorge Ramirez
C	1) R90 as DNP. 2) J12 pin 1 and pin 2 signal swapped. 3) J28,J29, J30 & J31changed for cut-trace options. 4) Zero ohm resistors added on PTC1~7 5) Layout improvements	03/24/17	Antonio Quiroz
C1	1) Change the decoupling capacitor on VDD_RF power pins from 12pF to 3pF for 2*LO leakage improvement. 2) Add 3pF capacitors on PTC1~PTC5 pins for 2*LO leakage improvement. 3) DNP J38, J39 4) DNP J17 and J16 with shorting traces connecting pins 3-4. 5) Change L1 to 5.6nH 6) use short tail connector for J1, J2, J3, J4	08/08/17	Jimmy Cheng
C2	Change the decoupling capacitor on VDD_RF power pins back to 12pF for RF performance consideration	11/06/17	Jimmy Cheng

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ICAP Classification: CP: IUO: X PUBI:

Designer: A. QUIROZ	Drawing Title: FRDM-KW41Z		
Drawn by: A. QUIROZ	Page Title: TITLE PAGE		
Approved: C. BROWN	Size C	Document Number SCH-29102 PDF: SPF-29102	Rev C2
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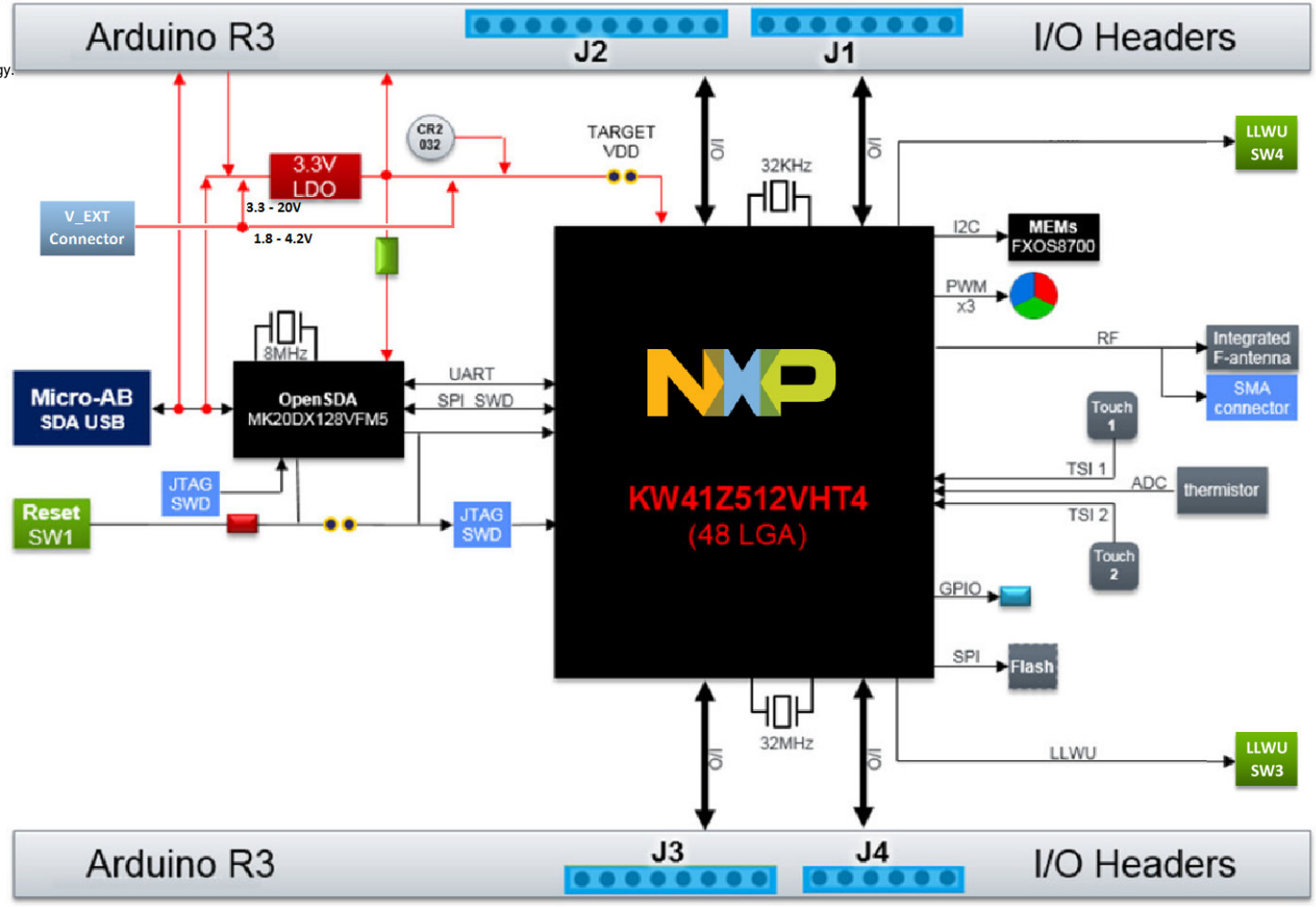
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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Drawing Title: **FRDM-KW41Z**

Page Title: **BLOCK DIAGRAM**

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DCDC_CFG

Neither V_EXT nor V_BATT should exceed 4.2V.

CAD notes: SHORTING J17 pin 3-4 ON BOTTOM LAYER

PSW_CFG

Default: on.

CAD Notes: SHORTING J16 pin 3-4 ON BOTTOM LAYER

REG_CFG

SHORTING HEADER ON BOTTOM LAYER

Power Configuration

Default: Buck Mode (auto start).

	PSW_CFG J16	DCDC_CFG J17	REG_CFG J38, J39
Bypass Mode (auto start) VDCDC_IN (1.71 to 3.6V) Operation 1.8V - 3.6 V	1-2	3-4	J38-on J39-on
Boost Mode (auto start) VDCDC_IN (0.9V to 1.8V) Single Battery Operation	3-4	1-2 5-6	J38-off J39-off
Buck Mode (manual start) VDCDC_IN (1.8V to 4.2V) Coin Cell Battery Operation	5-6 press SW6 to start	3-4	J38-off J39-off
Buck Mode (auto start) VDCDC_IN (1.8V to 4.2V) Coin Cell Battery Operation	3-4	3-4	J38-off J39-off

Place caps close to VDD0/VDD1 pins

Place caps close to VDD_RF pins

Use star config. for VDD_RF1 and VDD_RF2 cap

2*LO leakage decoupling capacitors. Should place the capacitors near PTCx pins as possible.

Place cap close to VDCDC_IN

Place components close to DUT

Place ind close to DUT

MKW41Z512VHT4 MCU

50 ohm controlled impedence line

RF

CAD NOTE: SMA - F-Antenna: Place both capacitor sharing pin 1

CAD NOTE: Open Solder Mask Bottom below F-Antenna on "feedpoint" via

SWD CONNECTOR

SHORTING HEADER ON BOTTOM LAYER.

OpenSDA can be used as a stand-alone debugger by cutting the trace under J12, which isolates the SWD_CLK from the on-board MCU.

POWER MANAGMENT

J23 jumper only if V_EXT is above DCDC limits:
Buck Mode - 4.2V
Bypass - 3.6V

LED_PWR_CFG

Default 1-2.

COIN CELL HOLDER

EXTERNAL PS

* For External PS, If 3.6V - 20V shunt J23 1-2, else if PS 1.8 - 3.6V open J23 and shunt J36 5-6.

32MHz XTAL

32kHz XTAL

IN CIRCUIT TEST GND PROBING

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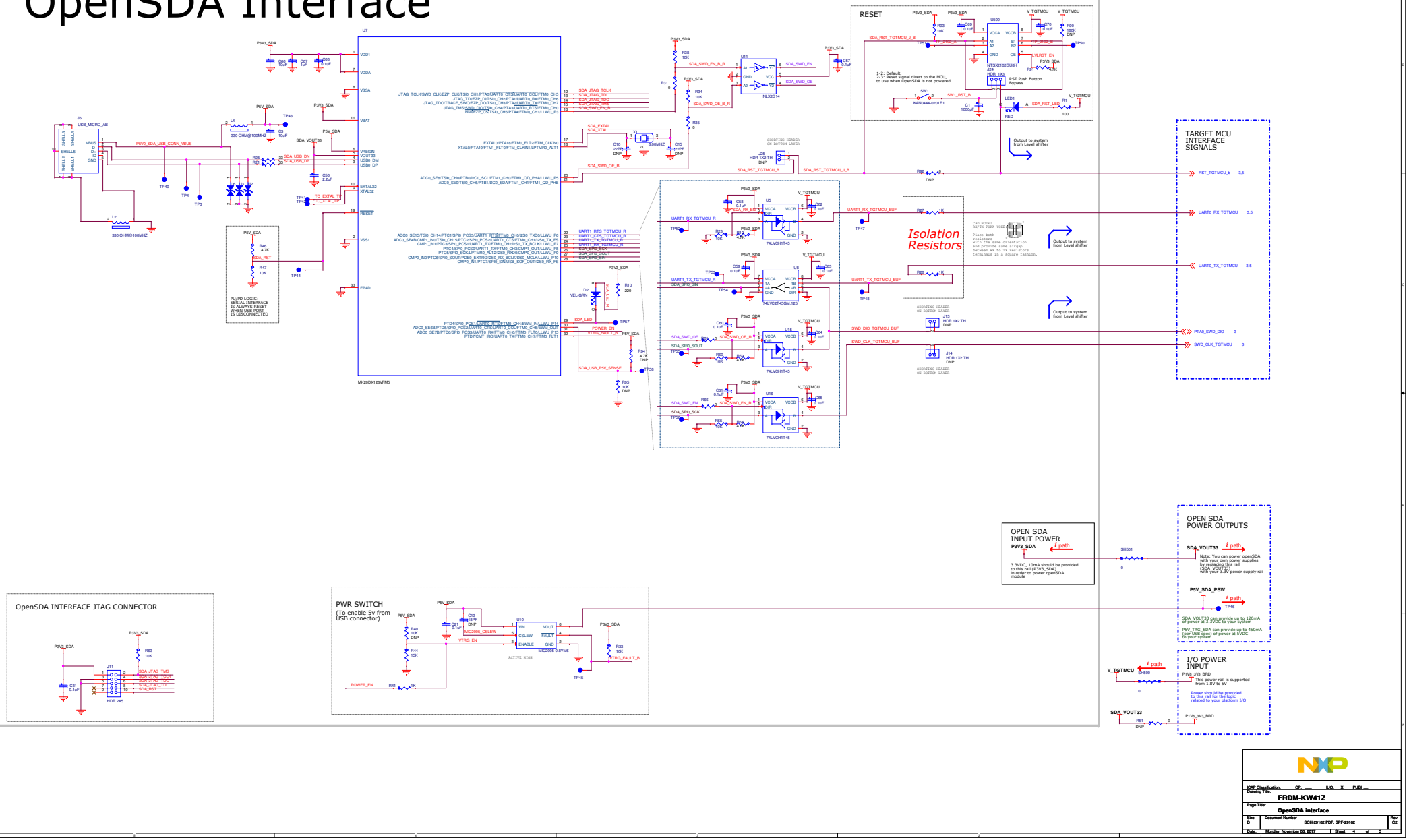
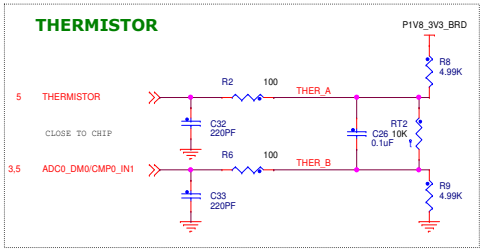
OpenSDA Interface

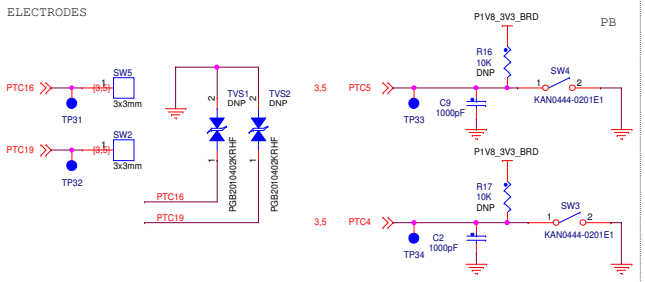


THERMISTOR



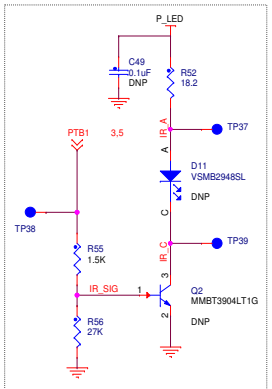
ADC SELECTOR

ELECTRODES

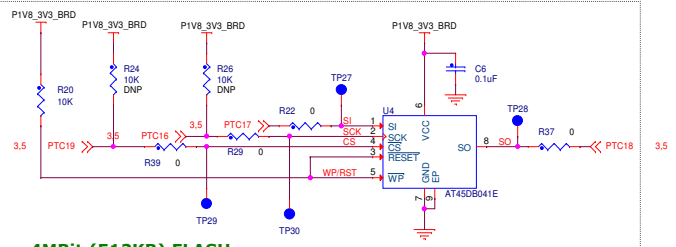


INTERRUPT PUSH BUTTONS

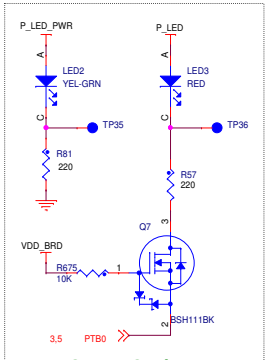
INFRARED LED



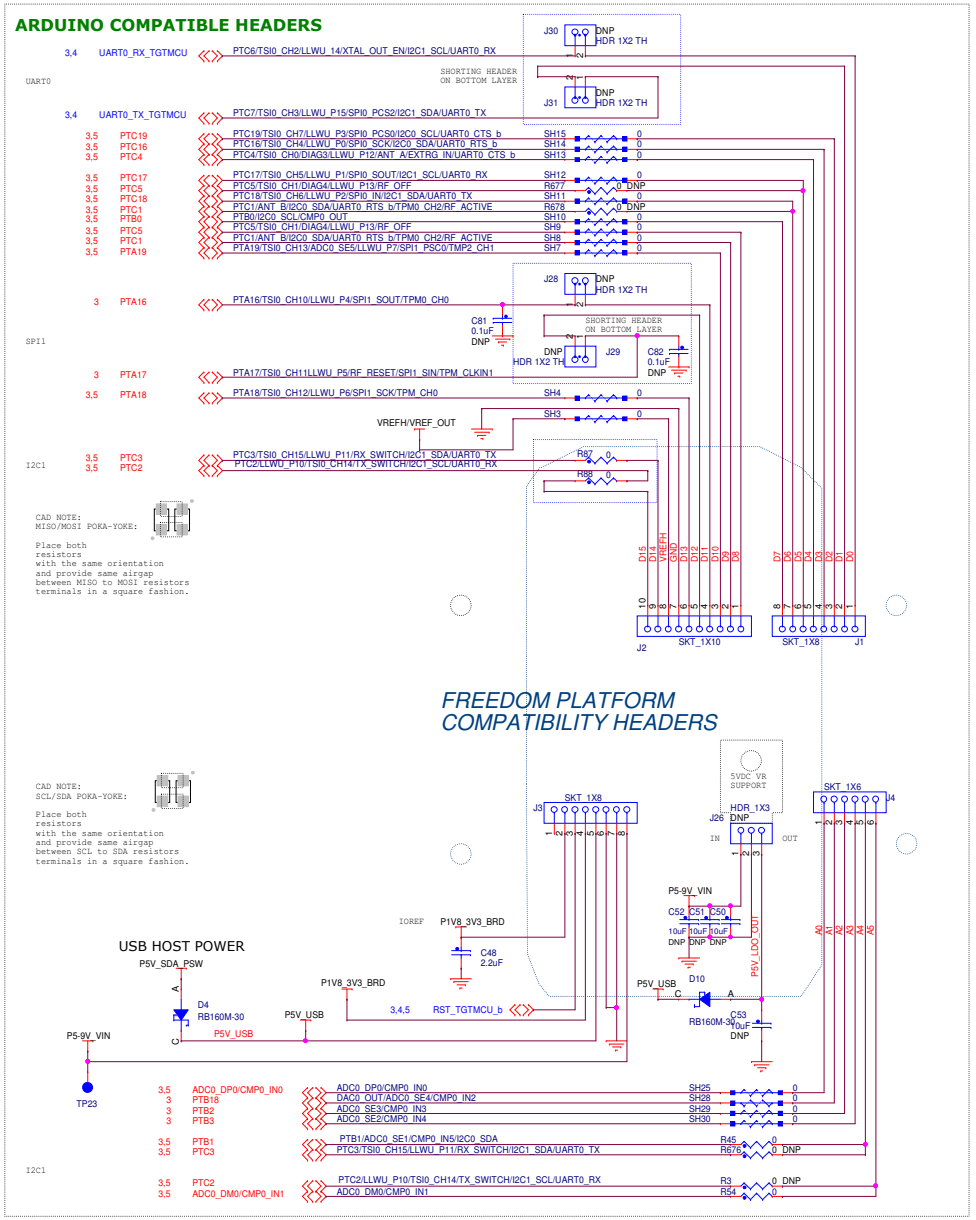
4MBit (512KB) FLASH



POWER ON/ COMMUNICATING



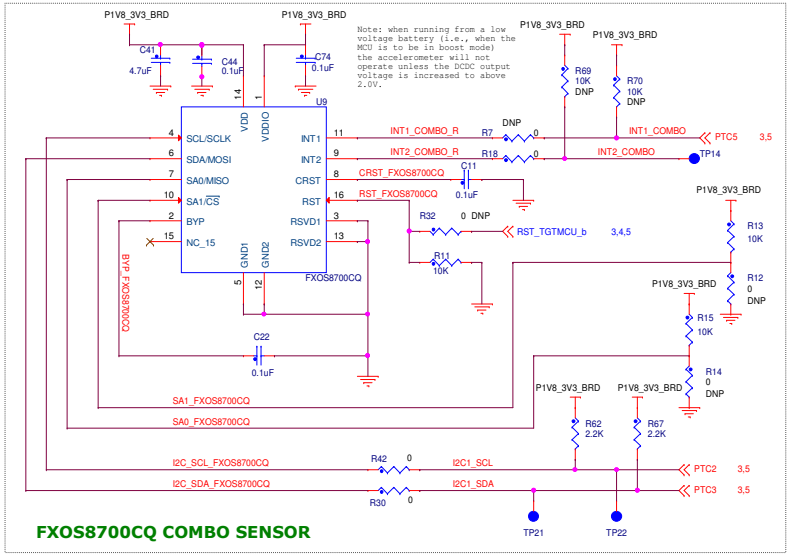
ARDUINO COMPATIBLE HEADERS



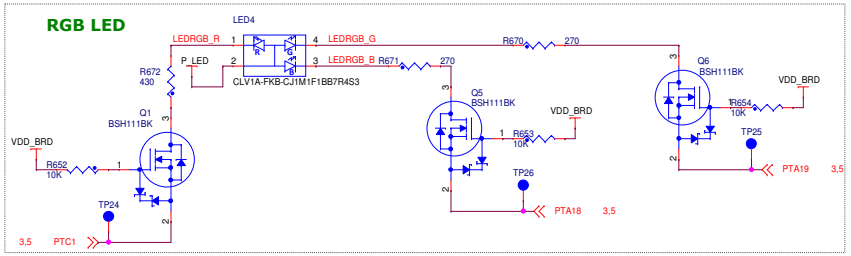
FREEDOM PLATFORM COMPATIBILITY HEADERS

USB HOST POWER

FXOS8700CQ COMBO SENSOR



RGB LED



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