Absolute Maximum Ratings

Parameter	Symbol	Terminals	Rating	Unit
Filament Voltage	Ef	F+,F-	2.58	V_{DC}
Logic Supply Voltage	VDD	VDD	-0.3 ~ 6.5	V_{DC}
Charge Pump Supply	VIN	VIN	-0.3 ~ +20	V_{DC}
Driver Supply Voltage	VDISP.	VDISP	-0.3 ~ +44	V_{DC}
Logic Input Voltage	VI	DA,CS,CP,RESET	-0.3 ~ VDD +0.3	V_{DC}
Storage Temperature	T_{STG}		-55~+85	℃

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Filament Voltage	Ef	-	1.94	2.15	2.37	V_{DC}
Logic Supply Voltage	VDD	-	3.0	3.3	3.6	V_{DC}
Driver Supply Voltage	VDISP.	-	21	23	25	V_{DC}
High Level Input Voltage	VIH	DA,CS,CP,RESET	0.8 VDD		VDD	V_{DC}
Low Level Input Voltage	VIL	DA,CS,CP,RESET	0		0.2 VDD	V_{DC}
Cut-off Voltage	Ek	-	1.15	-	-	V_{DC}
Oscillation Frequency	f_{OSC}	R_{OSC}=47KΩ,when VDD=5.0V; R_{OSC}=33KΩ,when VDD=3.3V;	-	1202	-	KHz
Frame Frequency	f_{FR}		-	783	-	Hz
Operating Temperature	T_{OPR}	-	- 20	-	70	℃

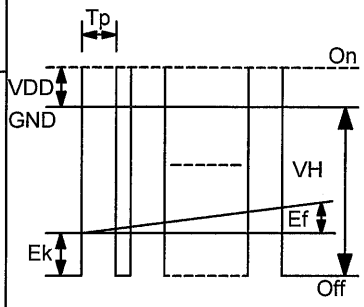
DC Electrical Characteristics (in typical condition)

Parameter	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Filament Current	If	F+,F-	Ef=typ VDD=VDISP=0	111	123	135	mA
Logic Supply Current	IDD	VDD	Display off	-	-	5.0	mA
Driver Supply Current	IEE(AVE)	VDISP	All light up	-	7.0	17.0	mA
	IEE(PEAK)	VDISP	All light up	-	7.0	19.0	mA
Input current	IIN	DA,CS,CP	VIN=VDD or VSS	- 1.0	-	1.0	μA

Pin Description

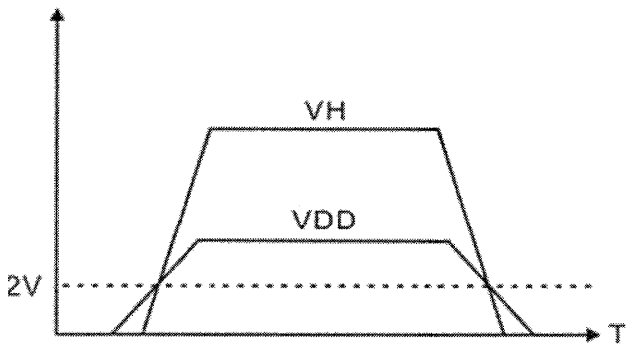
Pin Name	I/O	Description
F+,F-	I	Filament Voltage pin.
VDD	I	Logic Power Supply
VDISP	I	High-Voltage Power Supply
LGND	I	Logic Ground Pin
PGND	I	Ground Pin for High-Voltage
RESET	I	When this pin is "Low" level, the chip is reset.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.
CS	I	Serial Interface Strobe Pin The data input after the CS has fallen is processed as a command. When this pin is "High", CP is ignored.
CP	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.
DA	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock. (starting from the lower bit)

Optical Characteristics

ITEMS	Test Conditions	Color	Min.	Typ.	Max.	Unit
Brightness	Ef = 2.15 Vdc VDD = 3.3 Vdc VH = 23.0 Vdc EK = 2.0 Vdc f_{osc} = 1202 KHz Dimming = 240 /255	GREEN	1800 (365)	2500 (729)	— —	cd/m^2 (fl)
Brightness Ratio Between Digits		$\frac{L(Max)}{L(Min)}$	-	-	2	-
Color Coordinate NOTE 1)		GREEN (G. :x=0.250,y=0.439)				

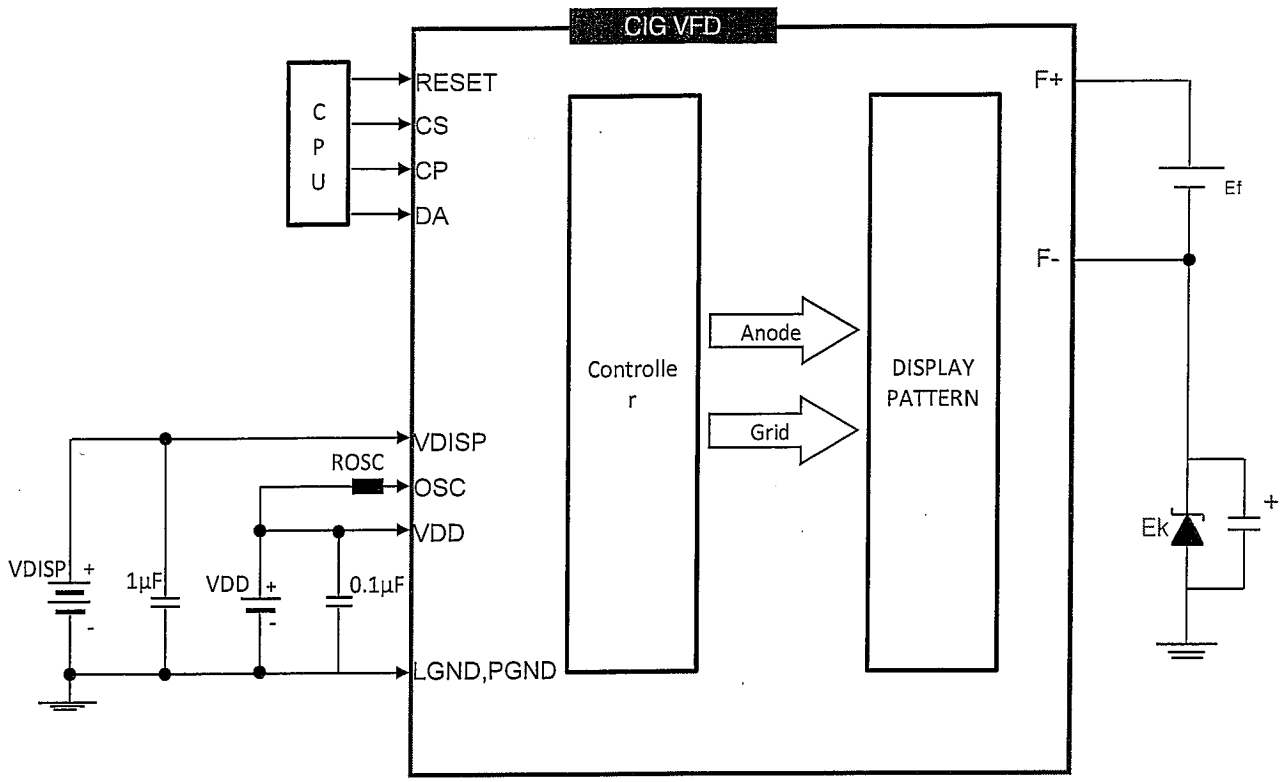
NOTE 1. All phosphor is Cd-free phosphor.

POWER SUPPLY SEQUENCE



4.BLOCK DIAGRAM

REV 1



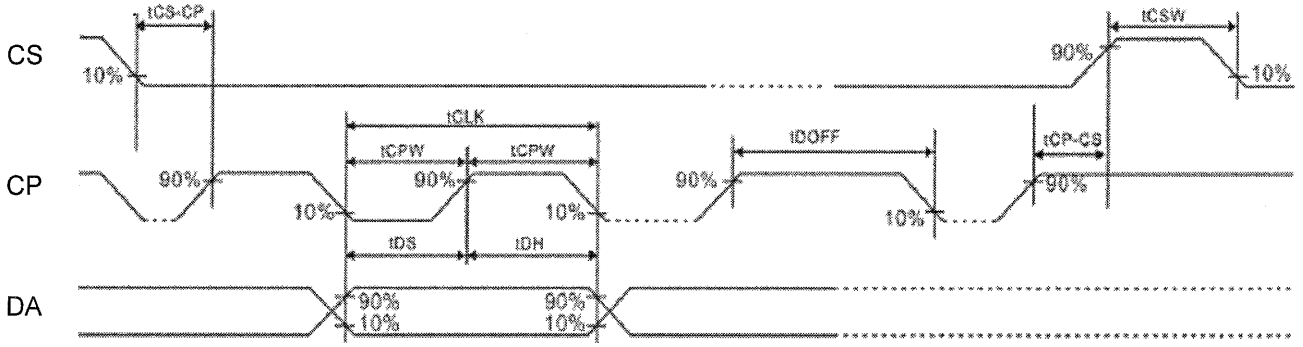
ROSC should be located as near the VFD lead as possible

TIMING CHARACTERISTICS

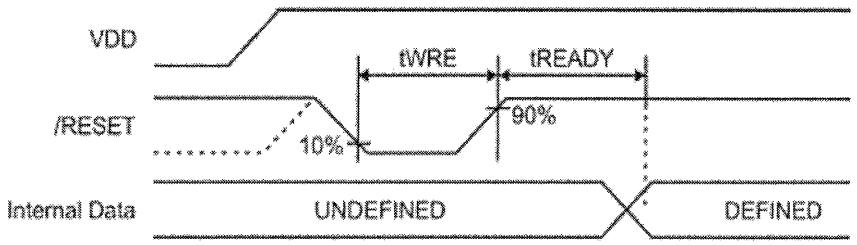
(Unless otherwise stated, VDD=5V/3.3V, GND=0V, VH=30V, Ta=25℃)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Pulse Width	tCPW	VDD=5V VDD=3.3V	400 550	-	-	nS
Clock Hold Time	tCS-CP	VDD=5V VDD=3.3V	250 250	-	-	nS
Data Setup Time	tDS	VDD=5V VDD=3.3V	100 150	-	-	nS
Data Hold Time	tDH	VDD=5V VDD=3.3V	100 150	-	-	nS
Data Processing Time	tDOFF	VDD=5V VDD=3.3V	1 2.5	-	-	µS
CS Hold Time	tCP-CS	VDD=5V VDD=3.3V	500 1000	-	-	nS
CS Pulse Width	tCSW	VDD=5V VDD=3.3V	500 750	-	-	nS
Reset Pulse Width	tRST	VDD=5V VDD=3.3V	15 10	-	-	µS
After Reset Ready Time	tREADY	VDD=5V VDD=3.3V	11	8	7	µS

WAVEFORMS

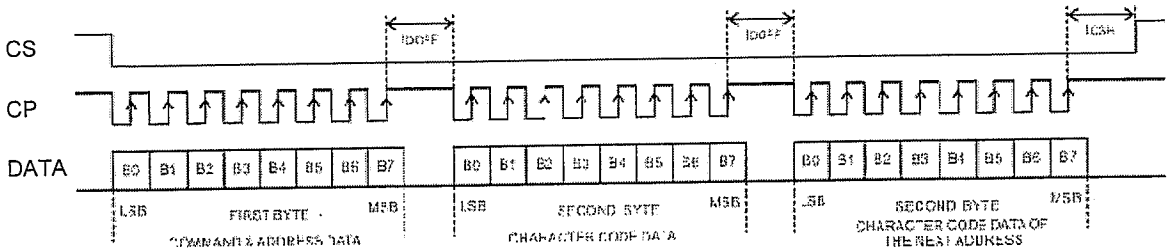


RESET



FUNCTION DESCRIPTION

The Display Control Command and the data are written by an 8-bit serial data transfer. Please refer to the diagram below



Note: When data is written into the RAM (ADRAM, CGRAM, URAM) in a continuous manner, the address are automatically incremented. Therefore it is not necessary to specify the first byte of the 2nd and later bytes when writing the RAM data.

When the CS pin is set to "LOW" Level, data transfer operation is enabled. 8-bit of data are sequentially inputted into the DA Pin (LSB first). The shift register reads the data at the rising edge of the shift clock. The data is then inputted into the CP Pin. The internal load signals are automatically generated and the data is written to each register and RAM. Thus, it is not necessary to input load signals externally.

When the CS Pin is set to "HIGH" Level, the data transfer operation is disabled. The data input when the CS Pin changes from "HIGH" to "LOW" be recognized in 8-bit units.

INSTRUCTIONS TABLE

The following are the list of commands issued by PT6394. When data is written into the RAM in a continuous manner, the addresses are automatically incremented internally. It is therefore not necessary to specify the first byte.

Instruction	MSB		First Byte					LSB	MSB		Second Byte					LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
DCRAM Data Write	0	0	1	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
CGRAM Data Write	0	1	0	*	*	Y2	Y1	Y0	*	D30	D25	D20	D15	D10	D5	D0	2nd Byte
									*	D31	D26	D21	D16	D11	D6	D1	3rd Byte
									*	D32	D27	D22	D17	D12	D7	D2	4th Byte
									*	D33	D28	D23	D18	D13	D8	D3	5th Byte
									*	D34	D29	D24	D19	D14	D9	D4	6th Byte
ADRAM Control Set	0	1	1	X4	X3	X2	X1	X0	*	*	*	*	E3	E2	E1	E0	2nd Byte
URAM Control Set	1	0	0	*	*	U2	U1	U0	8G	7G	6G	5G	4G	3G	2G	1G	2nd Byte
									16G	15G	14G	13G	12G	11G	10G	9G	3rd Byte
Charge pump pre-driver ON/OFF	1	0	1	0	0	1	CH	0	*	*	*	*	*	*	*	*	
Number of Digit Set	1	1	1	0	0	0	*	*	UV	F6	F5	F4	F3	F2	F1	F0	2nd Byte
LED setting	1	0	1	1	LE4	LE3	LE2	LE1	*	*	*	*	*	*	*	*	
Dimming Set	1	1	1	0	0	1	*	*	H7	H6	H5	H4	H3	H2	H1	H0	2nd Byte
Display Light Set	1	1	1	0	1	0	LS	HS	*	*	*	*	*	*	*	*	
Standby Mode	1	1	1	0	1	1	*	ST	*	*	*	*	*	*	*	*	

Notes:

1. *=Not Relevant.
2. Xn=Duty Timing (Digit) Address Set, n=0 to 4.
3. Cn=CGRAM/CGROM Character Code Bit, n=0 to 7.
4. Yn=CGRAM Address Bit, n=0 to 2.
5. Dn=CGRAM Character Code Setting, n=0 to 34.
6. En=Segment Pin Setting, n=0 to 3.
7. Un=URAM Address Set, n=0 to 2.
8. Gn=Grid ON/OFF Setting, n=1 to 16.
9. Fn=Number of Digits Set, n=0 to 6.
10. CH="1": Charge pump pre-driver ON / CH="0": Charge pump pre-driver OFF.
11. UV="1": Universal Function Enable / UV="0": Universal Function Disable.
12. Hn=Dimming Quantity Setting, n=0 to 7.
13. HS="1": All Output (Anode, Segment) Data="H" / HS="0": Normal Mode.
14. LS="1": All Output (Anode, Segment) Data="L" / LS="0": Normal Mode.
15. ST="1": Stand-by Mod / ST="0": Normal Mode.
16. LEn= LED Port ON/OFF, n=1 to 4.
    LEn=1 LED ON
    LEn=0 LED OFF

DATA CONTROL RAM (DCRAM) DATA WRITE COMMAND

The DCRAM Data Write Command is used to specify the address of the DCRAM and writes the character code of the CGROM and CGRAM (C0 to C7 bits). The DCRAM consists of 5 address bits which are used to store the CGRAM & CGROM character codes. The character codes specified by the DCRAM are converted to a 5 x 7 dot matrix character pattern via the CGROM and CGRAM. The DCRAM can each store up to 24 characters. The DCRAM Data Write Command Format is shown below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	DCRAM Data Write Mode is selected and the DCRAM Address is specified. (i.e. DCRAM Address=0H)
	0	0	1	X4	X3	X2	X1	X0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	CGROM & CGRAM Character Codes are specified. (They are written into the DCRAM Address 0H)
	C7	C6	C5	C4	C3	C2	C1	C0	

During a continuous data write operation from one DCRAM Address to the next, it is not necessary to specify the DCRAM address since they are automatically incremented; however, the character code must be specified. Please refer to the information below.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 1H.
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 2H.
	C7	C6	C5	C4	C3	C2	C1	C0	

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	MSB							LSB	
2nd Byte (25th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified an written into the DCRAM Address 17H.
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (26th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified an written into the DCRAM Address 0H.
	C7	C6	C5	C4	C3	C2	C1	C0	

where:

1. X4 (MSB) to X0 (LSB): DCRAM Address Bits (24 Characters).
2. C7 (MSB) to C0 (LSB): CGROM & CGRAM Character Code Bits (256 Characters).

Please refer to the table below for the Duty Timing position and DCRAM Address setting relationship.

X4	X3	X2	X1	X0	Duty Timing Position
0	0	0	0	0	T1 (1G is used)
0	0	0	0	1	T2 (2G is used)
0	0	0	1	0	T3 (3G is used)
0	0	0	1	1	T4 (4G is used)
0	0	1	0	0	T5 (5G is used)
0	0	1	0	1	T6 (6G is used)
0	0	1	1	0	T7 (7G is used)
0	0	1	1	1	T8 (8G is used)
0	1	0	0	0	T9 (9G is used)
0	1	0	0	1	T10 (10G is used)
0	1	0	1	0	T11 (11G is used)
0	1	0	1	1	T12 (12G is used)
0	1	1	0	0	T13 (13G is used)
0	1	1	0	1	T14 (14G is used)
0	1	1	1	0	T15 (15G is used)
0	1	1	1	1	T16 (16G is used)
1	0	0	0	0	T17 (Only Universal is used)
1	0	0	0	1	T18 (Only Universal is used)
1	0	0	1	0	T19 (Only Universal is used)
1	0	0	1	1	T20 (Only Universal is used)
1	0	1	0	0	T21 (Only Universal is used)
1	0	1	0	1	T22 (Only Universal is used)
1	0	1	1	0	T23 (Only Universal is used)
1	0	1	1	1	T24 (Only Universal is used)

CGRAM DATA WRITE COMMAND

The Character Generator RAM (CGRAM) Data Write Command is used to specify the CGRAM address (00H to 07H) and write the character pattern data. It consists of 3 address bits which is used to store the 5 x 7 dot matrix character patterns. The CGRAM can store up to 8 types of character patterns which may be displayed by specifying the Character Code (DCRAM Address). The CGRAM Data Write Command Format is given below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	CGRAM Data Write Mode is selected and the CGRAM Address is specified (i.e. CGRAM Address=00H).
	0	1	0	*	*	Y2	Y1	Y0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	1st Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D30	D25	D20	D15	D10	D5	D0	

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	2nd Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D31	D26	D21	D16	D11	D6	D1	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	3rd Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D32	D27	D22	D17	D12	D7	D2	

	MSB							LSB	
2nd Byte (5th)	B7	B6	B5	B4	B3	B2	B1	B0	4th Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D33	D28	D23	D18	D13	D8	D3	

	MSB							LSB	
2nd Byte (6th)	B7	B6	B5	B4	B3	B2	B1	B0	5th Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D34	D29	D24	D19	D14	D9	D4	

During a continuous data write operation from one CGRAM Address to the next, it is not necessary to specify the CGRAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 6th character pattern data byte are considered as one data item, therefore 1μs is sufficient value for parameter tDOFF between bytes. Please refer to the information below.

	MSB							LSB	
2nd Byte (7th)	B7	B6	B5	B4	B3	B2	B1	B0	1st Column Data is specified and rewritten into the CGRAM Address 01H.
	*	D30	D25	D20	D15	D10	D5	D0	

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	MSB							LSB	
2nd Byte (11th)	B7	B6	B5	B4	B3	B2	B1	B0	5th Column Data is specified and rewritten into the CGRAM Address 01H.
	*	D34	D29	D24	D19	D14	D9	D4	

where:

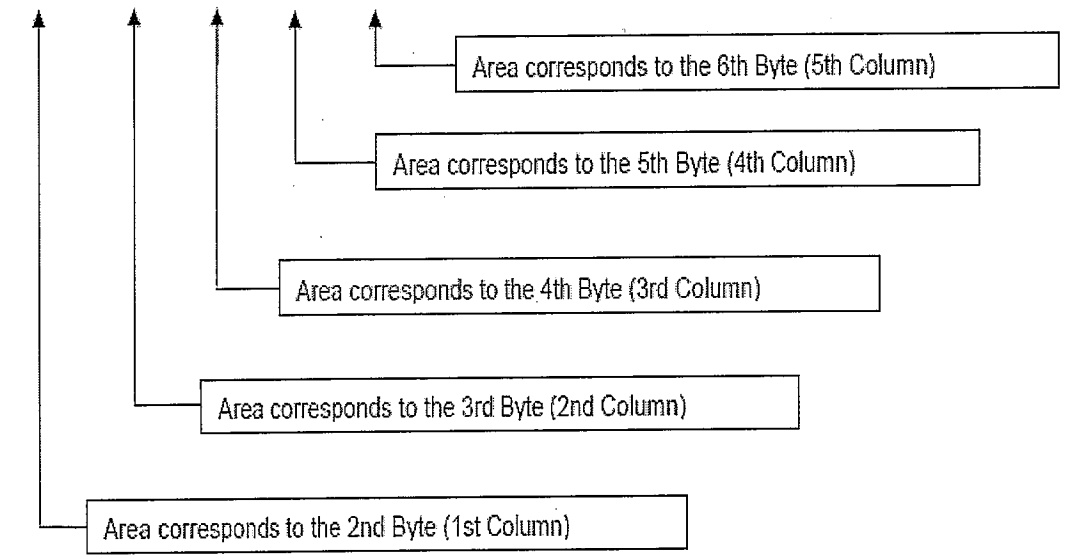
1. Y2 (MSB) to Y0 (LSB): CGRAM Address Bits (8 characters).
2. D34 (MSB) to D0 (LSB): Character Pattern Data Bits (35 outputs).

Please refer below for the CGROM Address and CGRAM Address Setting relationship

Y2	Y1	Y0	CGROM Address
0	0	0	RAM00 (00000000B)
0	0	1	RAM01 (00000001B)
0	1	0	RAM02 (00000010B)
0	1	1	RAM03 (00000011B)
1	0	0	RAM04 (00000100B)
1	0	1	RAM05 (00000101B)
1	1	0	RAM06 (00000110B)
1	1	1	RAM07 (00000111B)

The CGROM and CGRAM output area placement is given in the table below

D0	D1	D2	D3	D4
D5	D6	D7	D8	D9
D10	D11	D12	D13	D14
D15	D16	D17	D18	D19
D20	D21	D22	D23	D24
D25	D26	D27	D28	D29
D30	D31	D32	D33	D34



The Character Generator ROM (CGROM) consists of 8 CGROM Address bits generating 5 x 7 dot matrix character patterns. It can store up to a maximum of 248 types of character patterns.

ADRAM CONTROL SET COMMAND

The Additional Data RAM (ADRAM) consists of 5 address bits used to store the symbol data. It can store up to 4 types of symbol patterns per timing. The symbol data specified by the ADRAM is directly outputted. The terminals to which the ADRAM data are outputted may be used as a cursor. The ADRAM command format is given below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	ADRAM Data Write Mode is selected and the ADRAM address is specified. (i.e. ADRAM Address = 0H)
	0	1	1	X4	X3	X2	X1	X0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 0H.
	*	*	*	*	E3	E2	E1	E0	

During a continuous data write operation from one ADRAM Address to the next, it is not necessary to specify the ADRAM address since they are automatically incremented; however, the symbol data must be specified. Please refer to the information below.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 1H.
	*	*	*	*	E3	E2	E1	E0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 2H.
	*	*	*	*	E3	E2	E1	E0	

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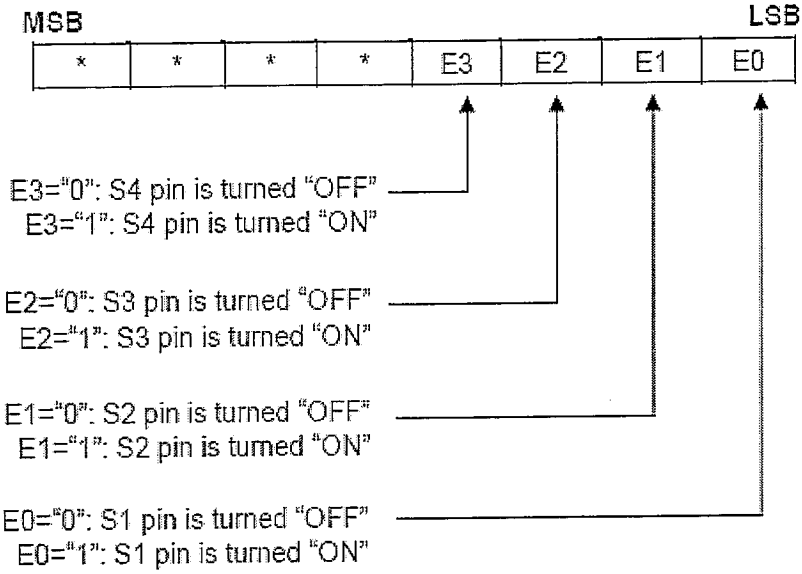
	MSB							LSB	
2nd Byte (25th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 17H.
	*	*	*	*	E3	E2	E1	E0	

	MSB							LSB	
2nd Byte (26th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and rewritten into the ADRA Address 0H.
	*	*	*	*	E3	E2	E1	E0	

where:

1. X4 (MSB) to X0 (LSB): ADRAM Address Bits (24 Characters).
2. E3 (MSB) to E0 (LSB): Symbol Data Bits (Symbol Data per timing).

Please refer to below for the segment position setting relationship.



Please refer to the table below for segment (E0~E3) position and ADRAM (X0~X4) Duty Timing (Digit) Address setting relationship.

Duty Timing (Digit) Address	S4 (E3)	S3 (E2)	S2 (E1)	S1 (E0)
T1 (01100000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T2 (01100001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T3 (01100010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T4 (01100011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T5 (01100100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T6 (01100101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T7 (01100110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T8 (01100111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T9 (01101000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T10 (01101001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T11 (01101010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T12 (01101011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T13 (01101100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T14 (01101101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T15 (01101110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T16 (01101111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T17 (01110000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T18 (01110001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T19 (01110010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T20 (01110011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T21 (01110100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T22 (01110101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T23 (01110110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T24 (01110111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF

URAM CONTROL SET COMMAND

The Universal RAM (URAM) consists of 3 address bits used to store the symbol data. It can store up to 16 types of symbol patterns per timing (T17~T24). The symbol data specified by the URAM is directly outputted. The URAM command format is given below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Universal Control Set Mode is selected and the URAM address is specified. (i.e. URAM Address=00H)
	1	0	0	*	*	U2	U1	U0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	1st Data is specified and rewritten into the URAM Address 00H.
	8G	7G	6G	5G	4G	3G	2G	1G	

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B2	B5	B4	B3	B1	B0	2nd Data is specified and rewritten into the URAM Address 00H.
	16G	15G	11G	14G	13G	12G	10G	9G	

During a continuous data write operation from one URAM Address to the next, it is not necessary to specify the URAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 3th character pattern data byte are considered as one data item, therefore 1μs is sufficient value for parameter tDOFF between bytes. Please refer to the information below.

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	1st Column Data is specified and rewritten into the URAM Address 01H.
	8G	7G	6G	5G	4G	3G	2G	1G	

	MSB							LSB	
2nd Byte (5th)	B7	B6	B5	B4	B3	B2	B1	B0	2nd Column Data is specified and rewritten into the URAM Address 01H.
	16G	15G	14G	13G	12G	11G	10G	9G	

where:

1. U2(MSB) to U0 (LSB): URAM Address Bits.
2. 16G (MSB) to 1G (LSB): Grid Pin Setting.

Please refer to the table below for the Grid (1G~16G) position and URAM (U0~U2) Duty Timing Address setting relationship

Duty Timing (Digit) Address				1G	2G	.....	15G	16G
Universal Name	U2	U1	U0					
T17	0	0	0	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T18	0	0	1	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T19	0	1	0	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T20	0	1	1	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T21	1	0	0	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T22	1	0	1	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T23	1	1	0	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF
T24	1	1	1	ON/OFF	ON/OFF	.....	ON/OFF	ON/OFF

Notes:

1. 1G~16G="0": Grid is turned "OFF".
2. 1G~16G="1": Grid is turned "ON".

NUMBER OF DIGITS SET COMMAND

The Number of Digits Set Command is used to write the number of display digits into the display digit register. Using a 7-bit data, the Number of Digits Set Command can display 16 to 24 digits. When the power is turned ON or when the /RESET signal is inputted, the value of B7 to B4 is set to "0" and the value of B3 to B0 is set to "1". It is advisable to always execute this command before the turning on the display. The command format is given below.

	MSB							LSB
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0
	UV	F6	F5	F4	F3	F2	F1	F0

The Number of Digits Set Mode is selected and the number of digit value is specified, Universal Function set to ON/OFF.

where:

1. F6 (MSB) to F0 (LSB): Display Duty Data Bits (24 stages).
2. UV (MSB): Universal Function Set.

The table below shows the relationship between the Setup Data and the Controlled Duty Timing (Digit).

MSB							LSB
UV	F6	F5	F4	F3	F2	F1	F0

UV="0": Universal Function "OFF". Digits can set up to 16, and disable F4~F6.
UV="1": Universal Function "ON". Digits can set up to 24, and enable F4~F6.

F6	F5	F4	Digits
0	0	0	T17
0	0	1	T17~T18
0	1	0	T17~T19
0	1	1	T17~T20
1	0	0	T17~T21
1	0	1	T17~T22
1	1	0	T17~T23
1	1	1	T17~T24

F3	F2	F1	F0	Digits
0	0	0	0	T1 (1G)
0	0	0	1	T1 (1G)~T2 (2G)
0	0	1	0	T1 (1G)~T3 (3G)
0	0	1	1	T1 (1G)~T4 (4G)
0	1	0	0	T1 (1G)~T5 (5G)
0	1	0	1	T1 (1G)~T6 (6G)
0	1	1	0	T1 (1G)~T7 (7G)
0	1	1	1	T1 (1G)~T8 (8G)
1	0	0	0	T1 (1G)~T9 (9G)
1	0	0	1	T1 (1G)~T10 (10G)
1	0	1	0	T1 (1G)~T11 (11G)
1	0	1	1	T1 (1G)~T12 (12G)
1	1	0	0	T1 (1G)~T13 (13G)
1	1	0	1	T1 (1G)~T14 (14G)
1	1	1	0	T1 (1G)~T15 (15G)
1	1	1	1	T1 (1G)~T16 (16G)

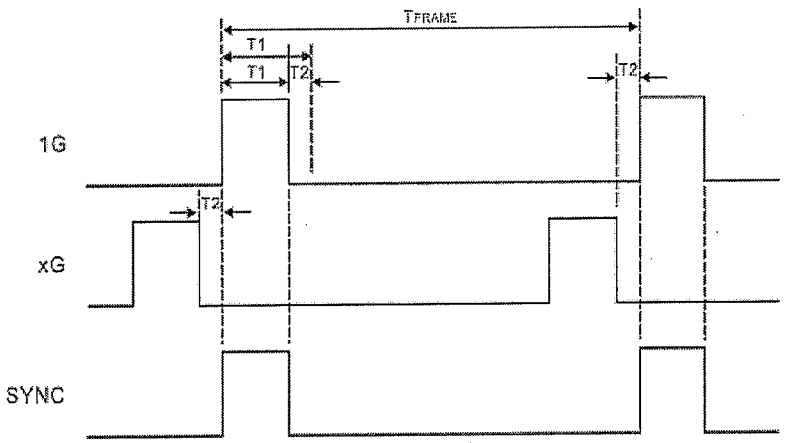
DIMMING SET COMMAND

The Dimming Set Command is used to write the display duty value to the duty cycle register. Using a 8-bit data, the display duty adjusts the contrast in 240 stages. When the power is turned ON or when the /RESET signal is inputted, the duty cycle register value is set to "0". It's advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

	MSB							LSB	
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0	Display Duty Set Mode is selected and the duty value is specified.
	H7	H6	H5	H4	H3	H2	H1	H0	

The relationship between the Setup Data, Controlled Output Duty is given in the table below

H7	H6	H5	H4	H3	H2	H1	H0	Dimming Quantity
0	0	0	0	0	0	0	0	0/255 x T
0	0	0	0	0	0	0	1	1/255 x T
0	0	0	0	0	0	1	0	2/255 x T
0	0	0	0	0	0	1	1	3/255 x T
0	0	0	0	0	1	0	0	4/255 x T
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	1	239/255 x T
1	1	1	1	0	0	0	0	240/255 x T
1	1	1	1	0	0	0	1	240/255 x T
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	240/255 x T
1	1	1	1	1	1	1	1	240/255 x T



where:

1. x=number of Grid.
2. T=T1 + T2

T1=Brightness pulse width

T2=Blank pulse width

DISPLAY LIGHT SET COMMAND

The Display Light Set Command is used to turn all display lights ON or OFF. All Display Lights On Mode is primarily used for testing the display. The All Display Light OFF Mode is used for the blinking display and to prevent any malfunction when the power is turned on. The command format is given below.

	MSB							LSB
	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	1	1	1	0	1	0	LS	HS

The table below shows Segment and Anode Display Status in relation to the Display Light Set Command data.

Bit Name		Segment and Anode Display Status
LS	HS	
0	0	Normal Display Mode
0	1	All outputs (Anode, Segment)="High" The duty of Grid will be follow Dimming Setting.
1	0	All outputs (Anode, Segment)="Low" The duty of Grid will be follow Dimming Setting.
1	1	No function, please don't use.

STAND-BY MODE COMMAND

The Stand-by Mode Command is stopped the IC's OSC Frequency.
However, in the meantime, the Anode, Segment and Grid will be Low, the "SW" will be High Level Output when ST set to "1" of the Stand-by Mode Command. Otherwise, it is a Normal Mode (OSC Frequency Active) when ST set to "0".

	MSB							LSB
	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	1	1	1	0	1	1	*	ST

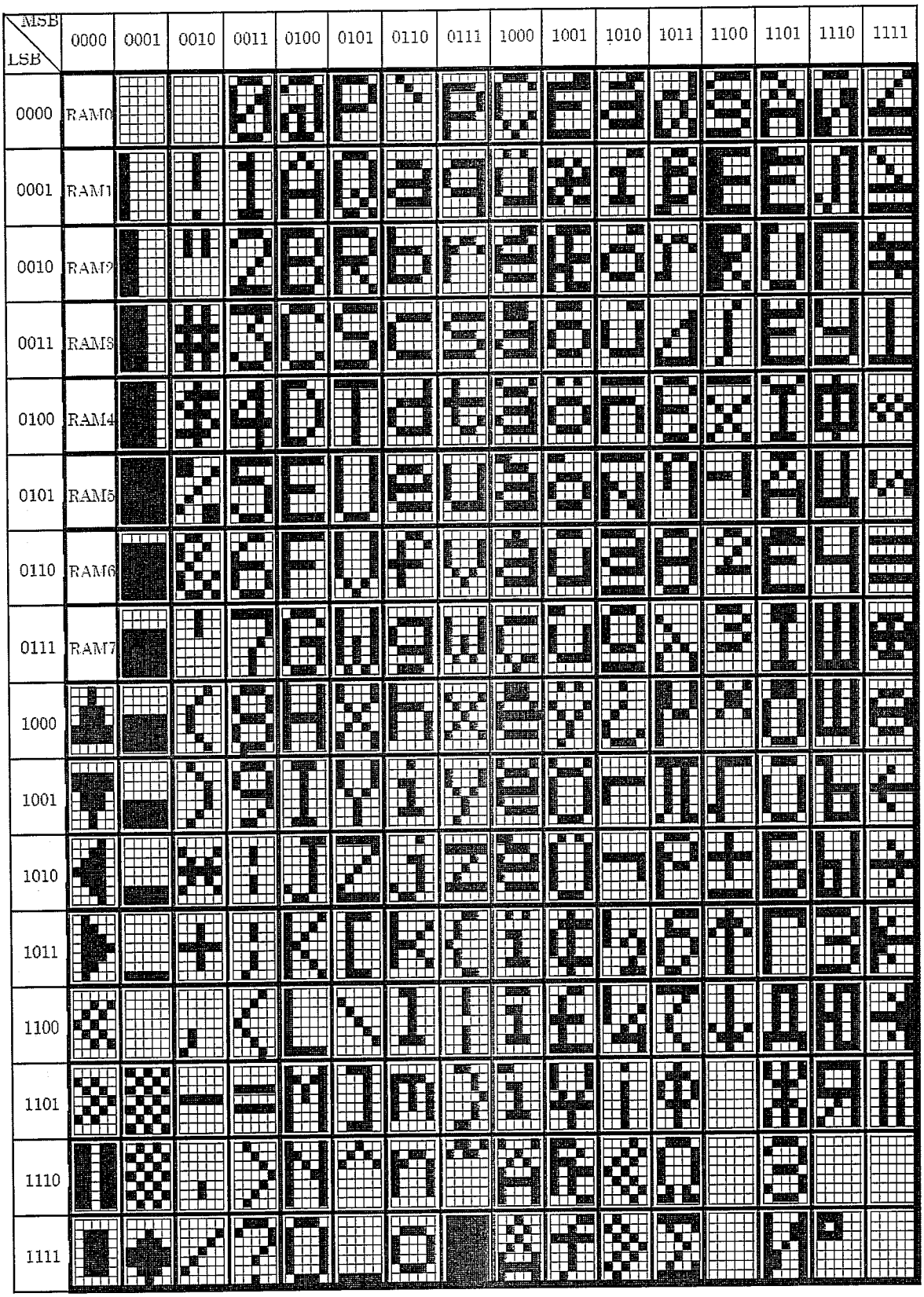
where:
1. ST="0": Normal Mode.
ST="1": Stand-by Mode.
2. *=Reserved.

RESET FUNCTION

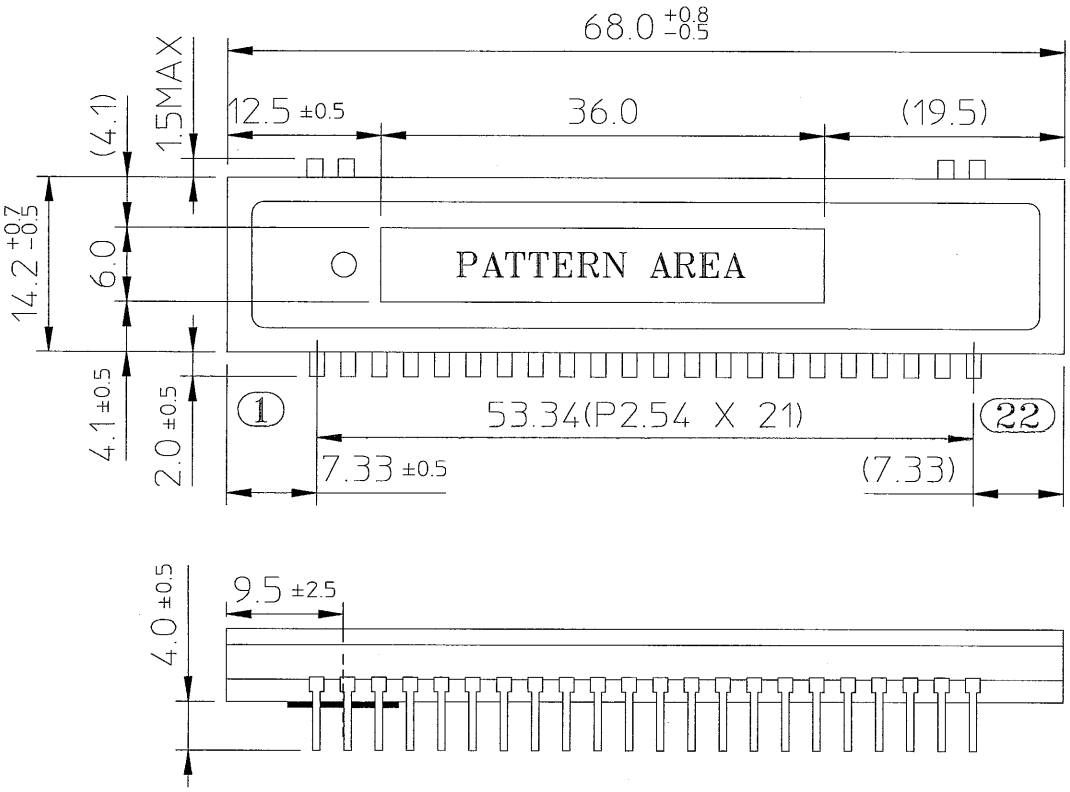
The internal status after power supply has been reset as follows

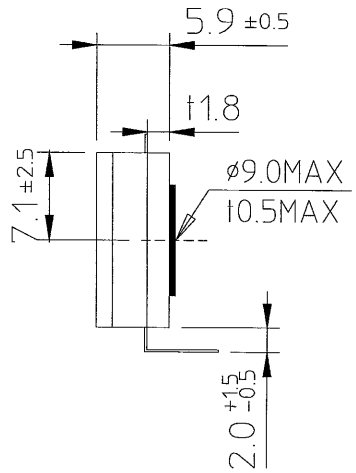
Instruction	At Reset Condition
DCRAM	DCRAM Address=00H All DCRAM_A Data=20H (Space Code)
CGRAM	CGRAM Address=00H All CGRAM Data=00H
ADRAM	ADRAM Address=00H All ADRAM Data=00H Segment OFF
URAM	URAM Disable URAM Address=00H All URAM Data=00H Grid OFF
Number of Digit Set	F0~F3="1111", F4~F6="000" Universal Function Disable (UV="0")
Dimming Set	Dimming Quantity=0/255 (H0~H7="0")
Display Light Set	HS="0" LS="1" All Output (Segment, Anode)=Low
Stand-by Mode	Disable
LED Output	LED1~4="0000" (All Low)
Charge Pump Pre-driver	Disable, "SW" set to High

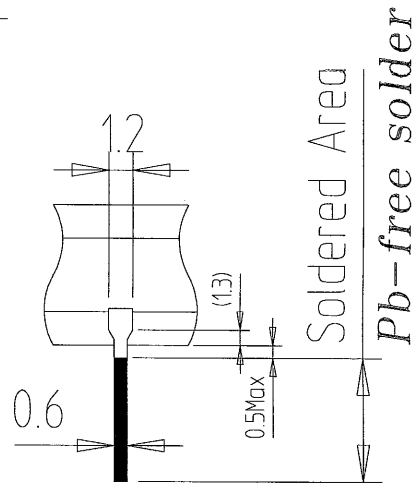
FONT


MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
RAM0
RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7

OUTER DIMENSIONS







LEAD DETAILS

PIN CONNECTION

PIN NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
PIN CONNECTION	F−	F−	NC	NC	NC	NC	DA	CP	NC	CS	NC	RESET	OSC	NC	VDD	NC	NC	VDISP	PGND	LGND	F+	F+

⊙ Notes ⊙

1) Fn : Filament pin
2) nG : Grid pin
3) Pn : Anode pin
4) NC : No Connected pin
5) NP : No pin

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OUTER DIMENSIONS
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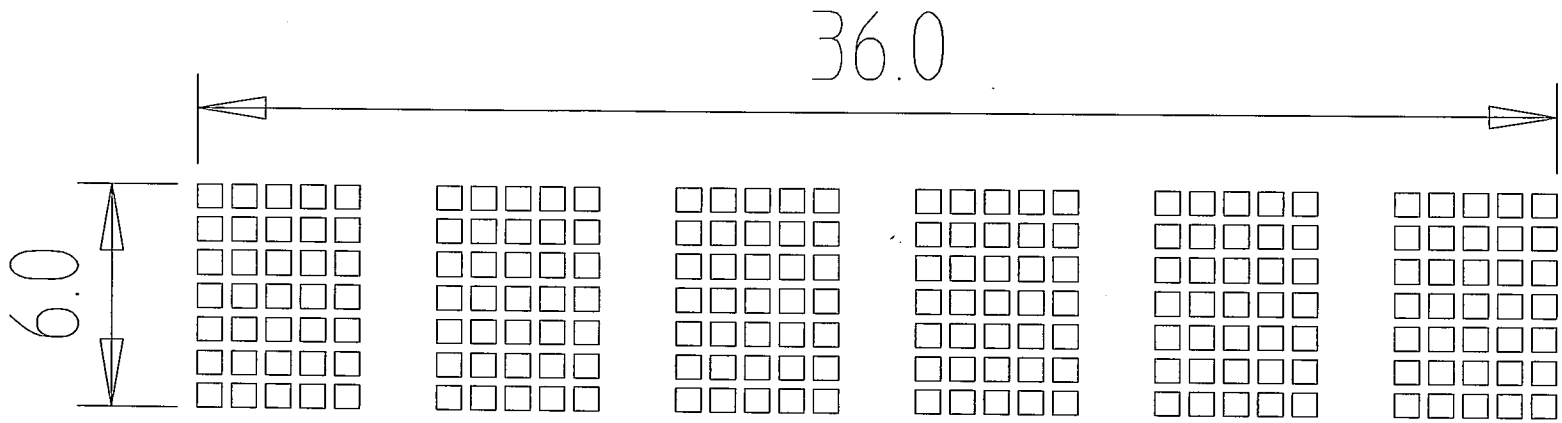
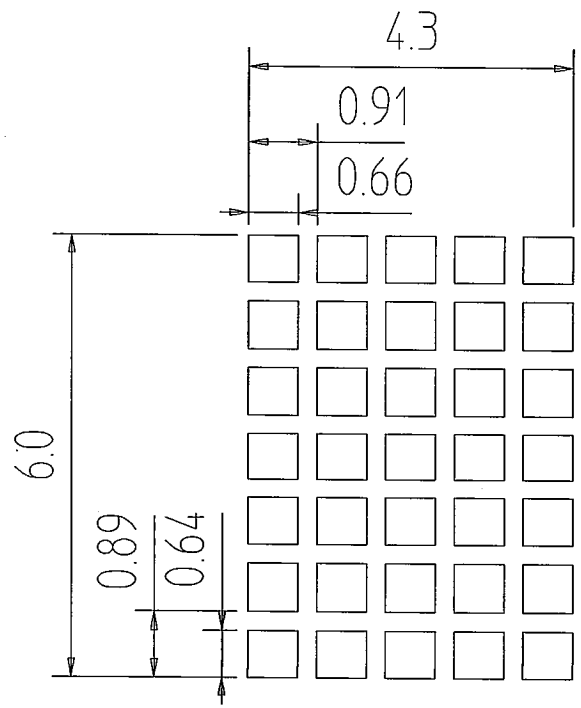
PATTERN DETAILS





◎ Color of Illumination ◎

◦ Green (G. x=0.250,y=0.439) ----- All Patterns.

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PATTERN DETAILS
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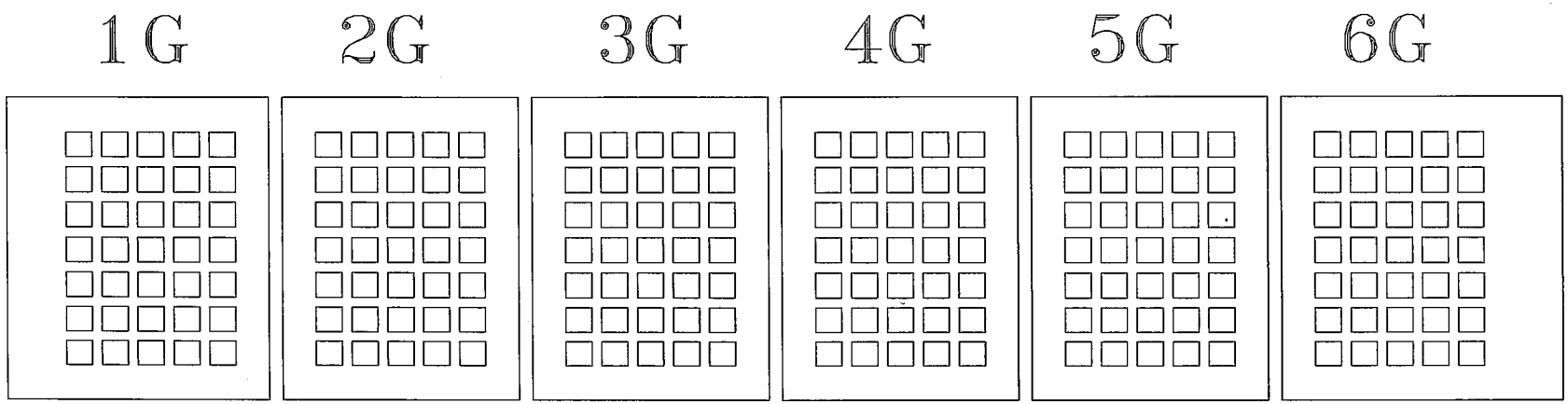
GRID ASSIGNMENT



1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35

(1G−6G)

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GRID ASSIGNMENT
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ANODE CONNECTION

	COM1-COM6
	1G-6G
SEG 1	1
SEG 2	2
SEG 3	3
SEG 4	4
SEG 5	5
SEG 6	6
SEG 7	7
SEG 8	8
SEG 9	9
SEG 10	10
SEG 11	11
SEG 12	12

	COM1-COM6
	1G-6G
SEG 13	13
SEG 14	14
SEG 15	15
SEG 16	16
SEG 17	17
SEG 18	18
SEG 19	19
SEG 20	20
SEG 21	21
SEG 22	22
SEG 23	23
SEG 24	24

	COM1-COM6
	1G-6G
SEG 25	25
SEG 26	26
SEG 27	27
SEG 28	28
SEG 29	29
SEG 30	30
SEG 31	31
SEG 32	32
SEG 33	33
SEG 34	34
SEG 35	35

MODEL : HCA-06S101T
ANODE CONNECTION
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