Cálculo da Média

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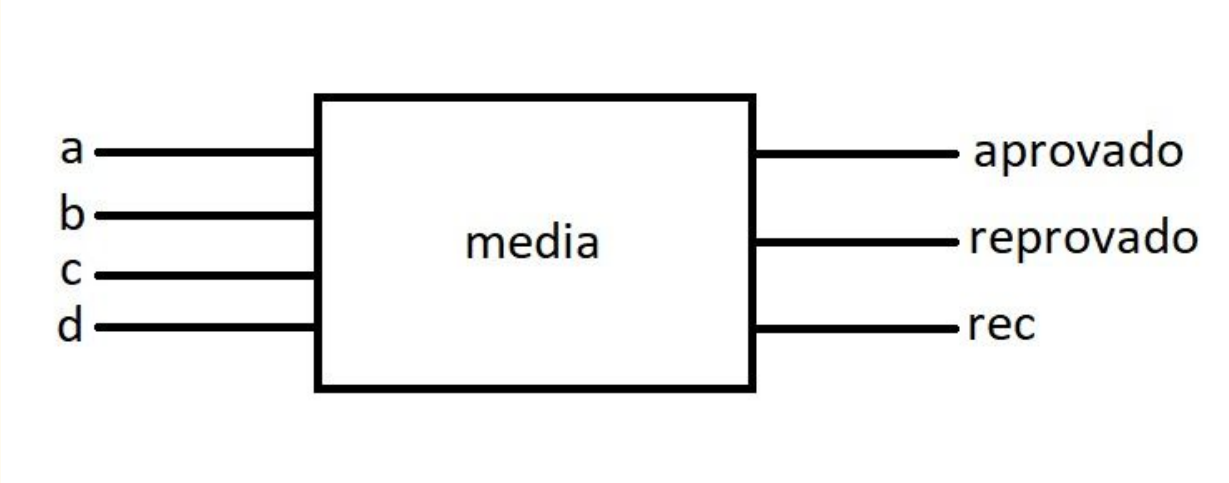
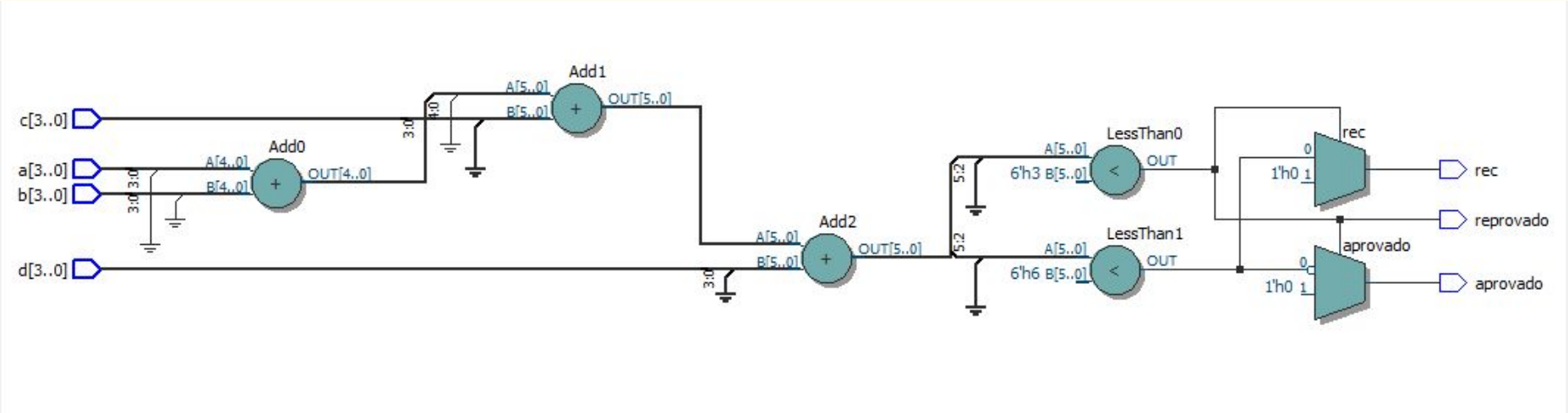
Descrição do Circuito:



VHDL:

```vhdl
entity media is
port(
        a, b, c, d: in std_logic_vector(3 downto 0);
        aprovado, rec, reprovado: out std_logic
);
end media;

architecture comp of media is
    signal total: unsigned(5 downto 0);
    signal media_nota: unsigned(5 downto 0);
begin
    total <= unsigned("00"&a) + unsigned("00"&b) + unsigned("00"&c) + unsigned("00"&d);
    media_nota <= total / 4;

process(media_nota) is
    begin
    if(media_nota < 3) then
        reprovado <= '1';
        aprovado <= '0';
        rec <= '0';
    elsif(media_nota < 6) then
        reprovado <= '0';
        aprovado <= '0';
        rec <= '1';
    else
        reprovado <= '0';
        aprovado <= '1';
        rec <= '0';
    end if;
end process;
end comp;
```

RTL Viewer:


c[3..0]
a[3..0]
b[3..0]
d[3..0]
Add0
A[4..0]
B[4..0]
OUT[4..0]
Add1
A[5..0]
B[5..0]
OUT[5..0]
Add2
A[5..0]
B[5..0]
OUT[5..0]
LessThan0
A[5..0]
6'h3
B[5..0]
OUT
LessThan1
A[5..0]
6'h6
B[5..0]
OUT
rec
1'h0
rec
reprovado
aprovado
1'h0
aprovado
3:0
5:2

Testbench:

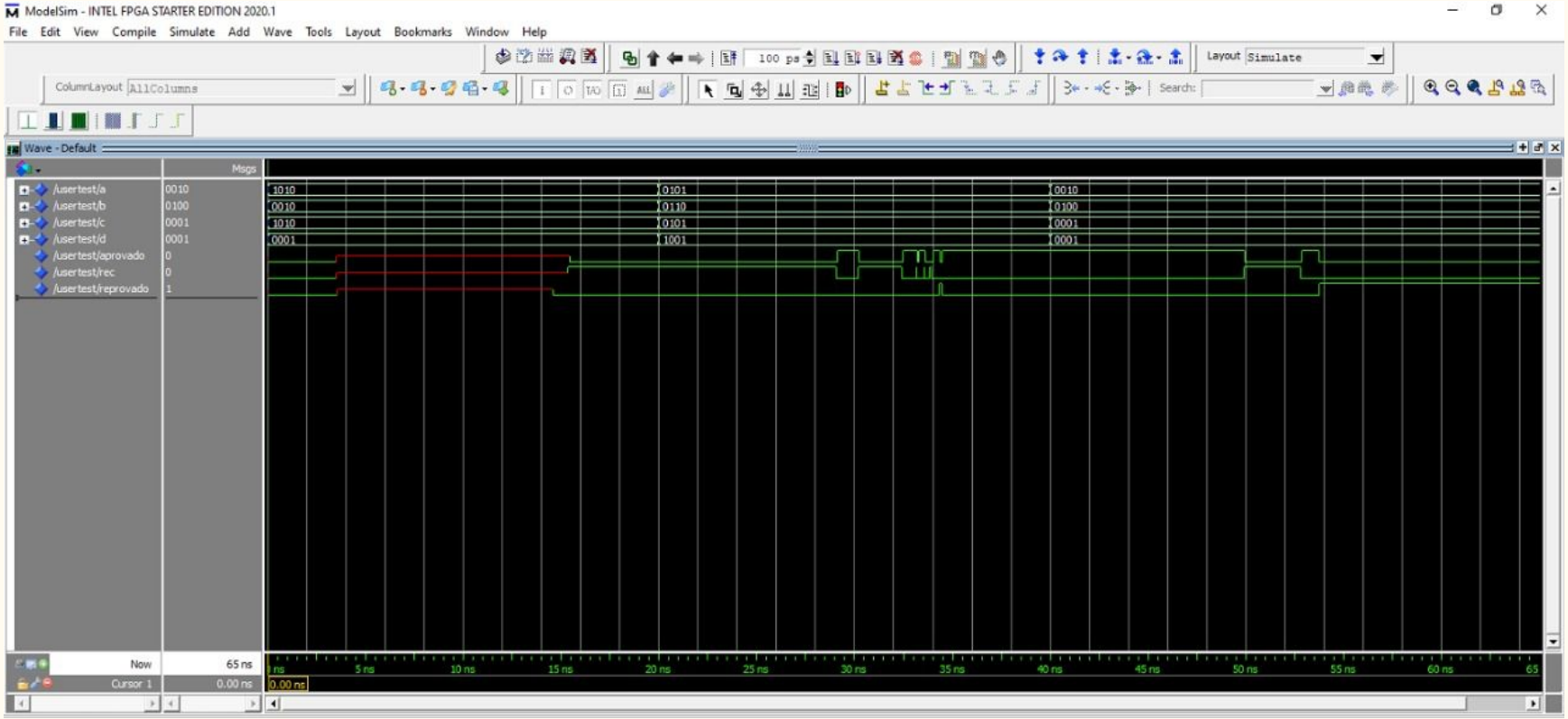
```
architecture tb of usertest is
    signal a, b, c, d: std_logic_vector(3 downto 0);
    signal aprovado, rec, reprovado: std_logic;

    component media
       port(
             a, b, c, d: in std_logic_vector(3 downto 0);
             aprovado, rec, reprovado: out std_logic
       );
    end component;

begin

    MD: media port map (a, b, c, d, aprovado, rec, reprovado);
     process
      constant period: time := 20 ns;
      begin
       a <= "1010"; b <= "0010"; c <= "1010"; d <= "0001";
       wait for period;
       a <= "0101"; b <= "0110"; c <= "0101"; d <= "1001";
       wait for period;
       a <= "0010"; b <= "0100"; c <= "0001"; d <= "0001";
       wait;
     end process;
end tb;
```

Resultados:

- Versão Quartus: Quartus 15.0 web
- Dispositivo: Cyclone IV GX EP4CGX15BF14C6
- LEs: 19
- Pinos: 19
- Registradores: 0
- Atraso: 13.099
- Como foi feita a divisão: /4

Medida	Entrada	Saída	Atraso
RR	c[0]	rec	12.747 ns
RF	c[0]	aprovado	12.762 ns
FR	c[1]	aprovado	13.099 ns
FF	c[1]	rec	13.078 ns

Simulação:


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Msgs
/usertest/a
/usertest/b
/usertest/c
/usertest/d
/usertest/aprovado
/usertest/rec
/usertest/reprovado
0010
0100
0001
0001
0
0
1
1010
0010
1010
0001
0101
0110
0101
1001
0010
0100
0001
0001
Now
65 ns
Cursor 1
0.00 ns
1 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns
40 ns
45 ns
50 ns
55 ns
60 ns