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Data Sheet: Technical Data

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MIMXRT1061CVL5A MIMXRT1061CVJ5A MIMXRT1062CVL5A MIMXRT1062CVJ5A

i.MX RT1060 Crossover Processors for Industrial Products



Package Information

Plastic Package 196-pin MAPBGA, 10 x 10 mm, 0.65 mm pitch 196-pin MAPBGA, 12 x 12 mm, 0.8 mm pitch

Ordering Information

See Table 1 on page 6

1 i.MX RT1060 Introduction

The i.MX RT1060 is a new processor family featuring NXP's advanced implementation of the Arm Cortex®-M7 core, which operates at speeds up to 528 MHz to provide high CPU performance and best real-time response.

The i.MX RT1060 processor has 1 MB on-chip RAM. 512 KB can be flexibly configured as TCM or general purpose on-chip RAM, while the other 512 KB is general-purpose on-chip RAM. The i.MX RT1060 integrates advanced power management module with DCDC and LDO that reduces complexity of external power supply and simplifies power sequencing. The i.MX RT1060 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, BluetoothTM, GPS, displays, and camera sensors. The i.MX RT1060 has rich audio and video features, including LCD display, basic 2D graphics, camera interface, SPDIF, and I2S audio interface. The

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i.MX RT1060 Introduction

i.MX RT1060 has analog interfaces, such as ADC, ACMP, and TSC.

The i.MX RT1060 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1060 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
 - 32 KB L1 Instruction Cache
 - 32 KB L1 Data Cache
 - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
 - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Tightly coupled GPIOs, operating at the same frequency as Arm
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 528 MHz
- Cortex M7 CoreSightTM components integration for debug
- Frequency of the core, as per Table 10, "Operating ranges," on page 22.

The SoC-level memory system consists of the following additional components:

- Boot ROM (128 KB)
- On-chip RAM (1 MB)
 - 512 KB OCRAM shared between ITCM/DTCM and OCRAM
 - Dedicate 512 KB OCRAM
- External memory interfaces:
 - 8/16-bit SDRAM, up to SDRAM-133/SDRAM-166
 - 8/16-bit SLC NAND FLASH, with ECC handled in software
 - SD/eMMC
 - SPI NOR FLASH
 - Parallel NOR FLASH with XIP support
 - Two single/dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
 - Two General Programmable Timers (GPT)
 - 4-channel generic 32-bit resolution timer for each
 - Each support standard capture and compare operation
 - Four Periodical Interrupt Timers (PIT)

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- Generic 32-bit resolution timer
- Periodical interrupt generation
- Four Quad Timers (QTimer)
 - 4-channel generic 16-bit resolution timer for each
 - Each support standard capture and compare operation
 - Quadrature decoder integrated
- Four FlexPWMs
 - Up to 8 individual PWM channels per each
 - 16-bit resolution PWM suitable for Motor Control applications
- Four Quadrature Encoder/Decoders

Each i.MX RT1060 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
 - Parallel RGB LCD interface
 - Support 8/16/24 bit interface
 - Support up to WXGA resolution
 - Support Index color with 256 entry x 24 bit color LUT
 - Smart LCD display with 8/16-bit MPU/8080 interface
- Audio:
 - S/PDIF input and output
 - Three synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
 - MQS interface for medium quality audio via GPIO pads
- Generic 2D graphics engine:
 - BitBlit
 - Flexible image composition options—alpha, chroma key
 - Porter-duff blending
 - Image rotation (90°, 180°, 270°)
 - Image size
 - Color space conversion
 - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
 - Standard 2D-DMA operation
- Camera sensors:
 - Support 24-bit, 16-bit, and 8-bit CSI input
- Connectivity:
 - Two USB 2.0 OTG controllers with integrated PHY interfaces
 - Two Ultra Secure Digital Host Controller (uSDHC) interfaces

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