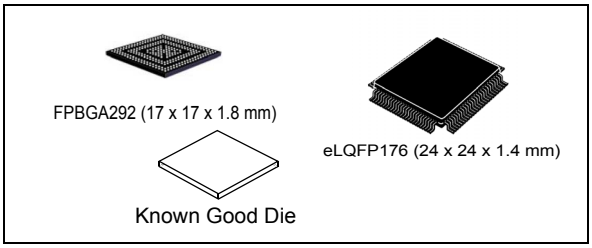
SPC58EEx, SPC58NEx

32-bit Power Architecture microcontroller for automotive ASIL-D applications

Datasheet - production data



Features

- AEC-Q100 qualified
- 32-bit Power Architecture VLE compliant CPU cores:
  - Three main CPUs, dual issue, 32-bit CPU core complexes (e200z4), two of them having one checker core in lock-step
  - Floating Point, End-to-End Error Correction
- 6576 KB (6288 KB code flash + 288 KB data flash) on-chip flash memory:
  - supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 608 KB on-chip general-purpose SRAM (in addition to 160 KB core local data RAM)
- 96-channel direct memory access controller (eDMA)
- Comprehensive new generation ASIL-D safety concept:
  - ASIL-D of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Dual-channel FlexRay controller
- Hardware Security Module (HSM)
- Junction temperature range -40 °C to 165 °C
- GTM 343 - Generic Timer Module:
  - Intelligent complex timer module
  - 144 channels (40 input and 104 output)
  - 5 programmable fine grain multi-threaded cores
  - 24-bit wide channels
- Enhanced analog-to-digital converter system with:
  - 1 supervisor 12-bit SAR analog converter
  - 4 separate fast 12-bit SAR analog converters
  - 3 separate 10-bit SAR analog converters, one with STDBY mode support
  - 6 separate 16-bit Sigma-Delta analog converters
- Communication interfaces:
  - 18 LINFlexD modules
  - 10 deserial serial peripheral interface (DSPI) modules
  - 8 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support, one supporting time-triggered controller area network (TTCAN)
- Two Ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
- Flexible Power Supply options:
  - External Regulators (1.2 V core, 3.3 V–5 V IO)
  - Single internal SMPS regulator (eLQFP176)
  - Single internal Linear Regulator with external ballast (FPBGA292)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART