NXP Semiconductors

Data Sheet: Technical Data

S32K1xx Data Sheet

Notes

- The following two attachments are available with the Datasheet:
 - S32K1xx Orderable Part Number List.xlsx
 - S32K1xx_Power_Modes_Configuration.xlsx

Key Features

- · Operating characteristics
 - Voltage range: 2.7 V to 5.5 V
 - Ambient temperature range: -40 °C to 105 °C for HSRUN mode, -40 °C to 125 °C for RUN mode
- ArmTM Cortex-M4F/M0+ core, 32-bit CPU
 - Supports up to 112 MHz frequency (HSRUN mode) with 1.25 Dhrystone MIPS per MHz
 - Arm Core based on the Armv7 Architecture and Thumb®-2 ISA
 - Integrated Digital Signal Processor (DSP)
 - Configurable Nested Vectored Interrupt Controller (NVIC)
 - Single Precision Floating Point Unit (FPU)
- · Clock interfaces
 - 4 40 MHz fast external oscillator (SOSC) with up to 50 MHz DC external square input clock in external clock mode
 - 48 MHz Fast Internal RC oscillator (FIRC)
 - 8 MHz Slow Internal RC oscillator (SIRC)
 - 128 kHz Low Power Oscillator (LPO)
 - Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
 - Up to 20 MHz TCLK and 25 MHz SWD_CLK
 - 32 kHz Real Time Counter external clock (RTC_CLKIN)

S32K1XX

- Power management
 - Low-power Arm Cortex-M4F/M0+ core with excellent energy efficiency
 - Power Management Controller (PMC) with multiple power modes: HSRUN, RUN, STOP, VLPR, and VLPS. Note: CSEc (Security) or EEPROM writes/ erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 Mhz) to execute CSEc (Security) or EEPROM writes/erase.
 - Clock gating and low power operation supported on specific peripherals.
- · Memory and memory interfaces
 - Up to 2 MB program flash memory with ECC
 - 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
 - Up to 256 KB SRAM with ECC
 - Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
 - Up to 4 KB Code cache to minimize performance impact of memory access latencies
 - QuadSPI with HyperBusTM support
- Mixed-signal analog
 - Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module
 - One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)
- · Debug functionality
 - Serial Wire JTAG Debug Port (SWJ-DP) combines
 - Debug Watchpoint and Trace (DWT)
 - Instrumentation Trace Macrocell (ITM)
 - Test Port Interface Unit (TPIU)
 - Flash Patch and Breakpoint (FPB) Unit
- Human-machine interface (HMI)
 - Up to 156 GPIO pins with interrupt functionality
 - Non-Maskable Interrupt (NMI)



· Communications interfaces

- Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
- Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
- Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
- Up to three FlexCAN modules (with optional CAN-FD support)
- FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
- Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.

· Safety and Security

- Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
- 128-bit Unique Identification (ID) number
- Error-Correcting Code (ECC) on flash and SRAM memories
- System Memory Protection Unit (System MPU)
- Cyclic Redundancy Check (CRC) module
- Internal watchdog (WDOG)
- External Watchdog monitor (EWM) module

· Timing and control

- Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
- One 16-bit Low Power Timer (LPTMR) with flexible wake up control
- Two Programmable Delay Blocks (PDB) with flexible trigger system
- One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
- 32-bit Real Time Counter (RTC)

Package

- 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX