SAMV71Q21RT

Radiation-Tolerant 32-bit Arm® Cortex®-M7 MCU

Introduction

The SAMV71Q21RT is a radiation-tolerant Arm® Cortex®-M7-based microcontroller providing the best combination of connectivity interfaces along with highest performance levels. The embedded dual CAN-FD interface and Ethernet-AVB controller provide state-of-the-art technology for high bandwidth communication. In addition to one of the most powerful Arm cores delivering 600 DMIPS, the SAMV71Q21RT features a flexible bus and memories architecture coupled with a powerful Floating Point Unit (FPU), thus providing advanced DSP and real-time capabilities to serve the most demanding aerospace applications.

Features

Core

- Arm Cortex-M7 running at up to 300 MHz
- 16 Kbytes of ICache and 16 Kbytes of DCache with Error Code Correction (ECC)
- Single- and double-precision HW Floating Point Unit (FPU)
- Memory Protection Unit (MPU) with 16 zones
- DSP Instructions, Thumb®-2 Instruction Set
- Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

Memories

- 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data
- 384 Kbytes embedded Multi-port SRAM
- Tightly Coupled Memory (TCM) interface with four configurations (disabled, 2 x 32 Kbytes, 2 x 64 Kbytes, 2 x 128 Kbytes)
- 16 Kbytes ROM with embedded Bootloader routines (UART0, USB) and IAP routines
- 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling
- 16-bit SDRAM Controller (SDRAMC) interfacing up to 256 MB and with on-the-fly scrambling
- Flash Write/Erase Cycles (Ground Level only): 10K Cycles within -40°C to 125°C temperature range
- Flash Data Retention:
  - 12 years with T_A = 125°C
  - 26 years with T_A = 110°C
  - 62 years with T_A = 95°C

System

- Embedded voltage regulator for single-supply operation

- Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation
- Quartz or ceramic resonator oscillators: 3 to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock
- RTC with Gregorian Calendar mode, waveform generation in low-power modes
- RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations
- 32-bit low-power Real-time Timer (RTT)
- High-precision Main RC oscillator with 12 MHz default frequency for device start-up. In-application trimming access for frequency adjustment. 8/12 MHz are factory-trimmed.
- 32.768 kHz crystal oscillator or Slow RC oscillator as source of Low-Power mode device clock (SLCK)
- One 500 MHz PLL for system clock
- Temperature Sensor
- One dual-port 24-channel central DMA Controller (XDMAC)

Low-Power Features

- Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wake-up logic enabled
- Ultra-low-power RTC and RTT
- 1 Kbyte of backup RAM (BRAM) with dedicated regulator

Peripherals

- One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE®1588 PTP frames and 802.3az Energy-efficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
- 12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission
- MediaLB® device with 3-wire mode, up to 1024 x Fs speed, supporting MOST25 and MOST50 networks
- Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.
- Five 2-wire UARTs with SleepWalking™ support
- Three Two-Wire Interfaces (TWIHS) (I^2C-compatible) with SleepWalking support
- Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling
- Two Serial Peripheral Interfaces (SPI)
- One Serial Synchronous Controller (SSC) with I2S and TDM support
- Two Inter-IC Sound Controllers (I2SC)
- One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
- Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor
- Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.

- Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 1.7 Msps. Offset and gain error correction feature.
- One 2-channel 12-bit 1 Msps-per-channel Digital-to-Analog Converter (DAC) with Differential and Over Sampling modes
- One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis

Cryptography

- True Random Number Generator (TRNG)
- AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications
- Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

I/O

- 114 I/O Lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination
- Five Parallel Input/Output Controllers (PIO)

Operating Range

- Temperature
  - CQFP144: -40°C to +125°C
  - LQFP144: -55°C to +125°C
- Single Supply Voltage: 3.0V to 3.6V
- Dual Supply Voltage
  - VDDIO: 3.0V to 3.6V
  - VDDCORE: 1.2V to 1.32V

Packages

- CQFP144, 144-lead CQFP, 22 x 22 mm, pitch 0.5 mm
- LQFP144, 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm

Radiation Performance

- No Single Event Latch-up Below an LET Threshold of 60 MeV.cm^2/mg @125°C
- Total Ionizing Dose of 30 krad(Si) RHA

ESD

- HBM 3000V
- CDM 750V

Mass

- CQFP144: 6187 mg
- LQFP144: 1365 mg

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog

Operating Conditions
- 2.1V to 3.6V, -40ºC to +85ºC, DC to 252 MHz
- 2.1V to 3.6V, -40ºC to +125ºC, DC to 180 MHz

Core: 252 MHz (up to 415 DMIPS) M-Class
- 16 KB I-Cache, 4 KB D-Cache
- FPU for 32-bit and 64-bit floating point math
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating, and fractional math
  - IEEE 754-compliant
- Code-efficient (C and Assembly) architecture

Clock Management
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up

Power Management
- Low-power modes (Sleep and Idle)
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)

Memory Interfaces
- 50 MHz External Bus Interface (EBI)
- 50 MHz Serial Quad Interface (SQI)

Audio and Graphics Interfaces
- Graphics interfaces: EBI or PMP
- Audio data communication: I^2S, LJ, and RJ
- Audio control interfaces: SPI and I^2C
- Audio master clock: Fractional clock frequencies with USB synchronization

High-Speed (HS) Communication Interfaces (with Dedicated DMA)
- USB 2.0-compliant Hi-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features
- Crypto Engine with RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
  - Peripheral and memory region access control

Direct Memory Access (DMA)
- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features
- 12-bit ADC module:
  - 18 Msps with up to six Sample and Hold (S&H) circuits (five dedicated and one shared)
  - Up to 48 analog inputs
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two comparators with 32 programmable voltage references
- Temperature sensor with ±2ºC accuracy

Communication Interfaces
- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I^2C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture
- Nine 16-bit or up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output
- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, pull-downs, and slew rate controls
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support
- AEC-Q100 REVH (Grade 1 -40ºC to +125ºC)
- Class B Safety Library, IEC 60730 (planned)
- Back-up internal oscillator

Debugger Development Support
- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Software and Tools Support
- C/C++ compiler with native DSP/fractional and FPU support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® μC/OS™, and SEGGER embOS®

Packages

Type	QFN	TQFP				TFBGA		VTLA	LQFP
Pin Count	64	64	100		144	100	144	124	144
I/O Pins (up to)	53	53	78		120	78	120	98	120
Contact/Lead Pitch	0.50 mm	0.50 mm	0.40 mm	0.50 mm	0.40 mm	0.65 mm	0.50 mm	0.50 mm	0.50 mm
Dimensions	9x9x0.9 mm	10x10x1 mm	12x12x1 mm	14x14x1 mm	16x16x1 mm	7x7x1.2 mm	7x7x1.2 mm	9x9x0.9 mm	20x20x1.40 mm

MSP430FR5969-SP Radiation Hardened Mixed-Signal Microcontroller

1 Device Overview

1.1 Features

- Radiation-Hardness Assured
  - Extended Temperature Operation (–55°C to 105°C) (1)
  - Single Event Latchup (SEL) Immune to 72 MeV.cm^2/mg at 125°C
  - Radiation Lot Acceptance Tested to 50 krad
  - 48-pin VQFN Plastic Package
  - Single Controlled Baseline
  - Extended Product Change Notification
  - Product Traceability
  - Extended Product Life Cycle
- Embedded Microcontroller
  - 16-Bit RISC Architecture up to 16-MHz Clock
  - Wide Supply Voltage Range (1.8 V to 3.6 V) (2)
- Optimized Ultra-Low-Power Modes
  - Active Mode: Approximately 100 µA/MHz
  - Standby (LPM3 With VLO): 0.4 µA (Typical)
  - Real-Time Clock (LPM3.5): 0.25 µA (Typical) (3)
  - Shutdown (LPM4.5): 0.02 µA (Typical)
- Ultra-Low-Power Ferroelectric RAM (FRAM)
  - Up to 64KB of Nonvolatile Memory
  - Ultra-Low-Power Writes
  - Fast Write at 125 ns Per Word (64KB in 4 ms)
  - Unified Memory = Program + Data + Storage in One Single Space
  - 10^{15} Write Cycle Endurance
  - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
  - 32-Bit Hardware Multiplier (MPY)
  - 3-Channel Internal DMA
  - Real-Time Clock (RTC) With Calendar and Alarm Functions
  - Five 16-Bit Timers With up to Seven Capture/Compare Registers Each
  - 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
  - 16-Channel Analog Comparator
  - 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold and up to 16 External Input Channels
- Multifunction Input/Output Ports
  - Accessible Bit-, Byte-, and Word-Wise (in Pairs)
  - Edge-Selectable Wake From LPM on All Ports
  - Programmable Pullup and Pulldown on All Ports
- Code Security and Encryption
  - 128-Bit or 256-Bit AES Security Encryption and Decryption Coprocessor
  - Random Number Seed for Random Number Generation Algorithms
- Enhanced Serial Communication
  - eUSCI_A0 and eUSCI_A1 Support
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI
  - eUSCI_B0 Supports
    - I^{2}C With Multiple Slave Addressing
    - SPI
  - Hardware UART
- Flexible Clock System
  - Fixed-Frequency DCO With 10 Selectable Factory-Trimmed Frequencies
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - 32-kHz Crystals (LFXT)
  - High-Frequency Crystals (HFXT)
- Development Tools and Software
  - Free Professional Development Environments With EnergyTrace++™ Technology
  - Development Kit (MSP-TS430RGZ48C)
- For Complete Module Descriptions, See the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*

(1) Refer to MSP430FR5969-SP EM Lifetime Derating Chart in the *Specifications* Section.
(2) Minimum supply voltage is restricted by SVS levels.
(3) RTC is clocked by a 3.7-pF crystal.

1.2 Applications

- Spacecraft Distributed Telemetry and Housekeeping
- Sensor Management
- Data Logging

1.3 Description

The MSP430™ ultra-low-power (ULP) FRAM platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power.

The ultra low-power architecture of the MSP430FR5969-SP showcases seven low-power modes, optimized to achieve power efficient distributed telemetry/housekeeping systems.

The integrated mixed-signal features of the MSP430FR5969-SP make it ideally suited for distributed telemetry applications in next-generation spacecraft. The strong immunity to single-event latchup and total ionizing dose, enable the device to be used in a variety of space and radiation environments.

Device Information(1)

PART NUMBER	GRADE	PACKAGE(2)
M4FR5969SRGZT-MLS	MLS	48-pin VQFN 7.00 mm × 7.00 mm
M4FR5969SPHPT-MLS	MLS	HTQFP (48) 7.00 mm × 7.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

TEXAS INSTRUMENTS

TMS320F28388D, TMS320F28386D, TMS320F28384D
TMS320F28388S, TMS320F28386S, TMS320F28384S

SPRSP14 – MAY 2019

TMS320F2838x Microcontrollers With Connectivity Manager

1 Device Overview

1.1 Features

- Dual-core C28x architecture
  - Two TMS320C28x 32-bit CPUs
    - 200 MHz
    - IEEE 754 double-precision (64-bit) Floating-Point Unit (FPU)
    - Trigonometric Math Unit (TMU)
    - CRC engine and instructions (VCRC)
    - Fast Integer Division (FINTDIV)
  - 512KB (256KW) of flash on each CPU (ECC-protected)
  - 44KB (22KW) of local RAM on each CPU
  - 128KB (64KW) of global RAM shared between the two CPUs (parity-protected)
- Two Control Law Accelerators (CLAs)
  - 200 MHz
  - IEEE 754 single-precision floating-point
  - Executes code independently of C28x CPU
- System peripherals
  - Two External Memory Interfaces (EMIFs) with ASRAM and SDRAM support
  - Two 6-channel Direct Memory Access (DMA) controllers
  - Up to 169 General-Purpose Input/Output (GPIO) pins with input filtering
  - Expanded Peripheral Interrupt controller (ePIE)
  - Low-power mode (LPM) support
  - Dual-zone security for third-party development
  - Unique Identification (UID) number
  - Embedded Real-time Analysis and Diagnostic (ERAD)
  - Background CRC (BGCRC)
- Connectivity Manager (CM)
  - Arm® Cortex®-M4 processor
  - 125 MHz
  - 512KB of flash (ECC-protected)
  - 96KB of RAM (ECC-protected or parity-protected)
  - Advanced Encryption Standard (AES) accelerator
  - Generic CRC (GCRC)
  - 32-channel Micro Direct Memory Access (µDMA) controller
  - Universal Asynchronous Receiver/Transmitter (CM-UART)
  - Inter-integrated Circuit (CM-I2C)
  - Synchronous Serial Interface (SSI)
  - 10/100 Ethernet 1588 MII/RMII
  - MCAN (CAN-FD)
- C28x communications peripherals
  - Fast Serial Interface (FSI) with two transmitters and eight receivers
  - Four high-speed (up to 50-MHz) SPI ports (pin-bootable)
  - Four Serial Communications Interfaces (SCI/UART) (pin-bootable)
  - Two I2C interfaces (pin-bootable)
  - Power-Management Bus (PMBus) interface
  - Two Multichannel Buffered Serial Ports (McBSPs)
- CM-C28x shared communications peripherals
  - EtherCAT® Slave Controller (ESC)
  - USB 2.0 (MAC + PHY)
  - Two Controller Area Network (CAN) modules (pin-bootable)
- Analog subsystem
  - Four Analog-to-Digital Converters (ADCs)
    - 16-bit mode
      - 1.1 MSPS each
      - 12 differential or 24 single-ended inputs
    - 12-bit mode
      - 3.5 MSPS each
      - 24 single-ended inputs
    - Single sample-and-hold (S/H) on each ADC
    - Hardware post-processing of conversions
  - Eight windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - Three 12-bit buffered DAC outputs
- Control peripherals
  - 32 Pulse Width Modulator (PWM) channels
    - High resolution on both A and B channels of 8 PWM modules (16 channels)
    - Dead-band support (on both standard and high resolution)
  - Seven Enhanced Capture (eCAP) modules
    - High-resolution Capture (HRCAP) available on two of the seven eCAP modules
  - Three Enhanced Quadrature Encoder Pulse (eQEP) modules
  - Eight Sigma-Delta Filter Module (SDFM) input channels, 2 independent filters per channel

ADVANCE INFORMATION

- Configurable Logic Block (CLB)
  - Augments existing peripheral capability
  - Supports position manager solutions
- Clock and system control
  - Two internal zero-pin 10-MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- 1.2-V core, 3.3-V I/O design
- Package options:
  - Lead-free, green packaging
  - 337-ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT suffix]
- Temperature options:
  - S: –40ºC to 125ºC junction
  - Q: –40ºC to 125ºC ambient (AEC Q100 qualification for automotive applications)

1.2 Applications

- Advanced Driver Assistance Systems (ADAS)
- Building automation
- Electric Vehicle/Hybrid Electric Vehicle (EV/HEV) powertrain
- Factory automation
- Grid infrastructure
- Industrial transport
- Medical, healthcare, and fitness
- Motor drives
- Power delivery
- Telecom infrastructure
- Test and measurement

1.3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing.

The TMS320F2838x is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications. The F2838x supports a dual-core C28x architecture along with a new Connectivity Manager that offloads critical communication tasks, significantly boosting system performance. The integrated analog and control peripherals with advanced connectivity peripherals like EtherCAT and Ethernet also let designers consolidate real-time control and real-time communications architectures, reducing requirements for multicontroller systems.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations.

The F2838x microcontroller family features two CLA real-time control coprocessors. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics. The dual C28x+CLA architecture enables intelligent partitioning between various system tasks. For example, one C28x+CLA core can be used to track speed and position, while the other C28x+CLA core can be used to control torque and current loops.

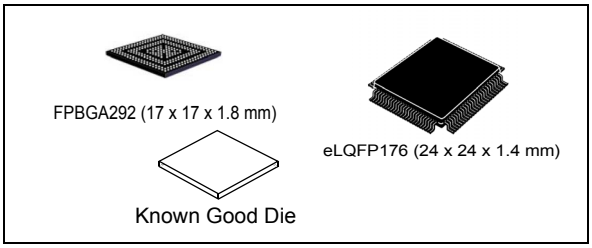
The Connectivity Manager subsystem is based on the Cortex-M4 CPU and has access to advanced communication IPs like EtherCAT, Ethernet, MCAN (CAN-FD), and AES.

The TMS320F2838x supports up to 1.5MB (512KB per CPU) of flash memory with error correction code (ECC) and up to 312KB (216KB total for C28x CPU1 and CPU2, and 96KB on the Cortex-M4) of SRAM. Two 128-bit secure zones are also available on the device for code protection.

SPC58EEx, SPC58NEx

32-bit Power Architecture microcontroller for automotive ASIL-D applications

Datasheet - production data



Features

- AEC-Q100 qualified
- 32-bit Power Architecture VLE compliant CPU cores:
  - Three main CPUs, dual issue, 32-bit CPU core complexes (e200z4), two of them having one checker core in lock-step
  - Floating Point, End-to-End Error Correction
- 6576 KB (6288 KB code flash + 288 KB data flash) on-chip flash memory:
  - supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 608 KB on-chip general-purpose SRAM (in addition to 160 KB core local data RAM)
- 96-channel direct memory access controller (eDMA)
- Comprehensive new generation ASIL-D safety concept:
  - ASIL-D of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Dual-channel FlexRay controller
- Hardware Security Module (HSM)
- Junction temperature range -40 °C to 165 °C
- GTM 343 - Generic Timer Module:
  - Intelligent complex timer module
  - 144 channels (40 input and 104 output)
  - 5 programmable fine grain multi-threaded cores
  - 24-bit wide channels
- Enhanced analog-to-digital converter system with:
  - 1 supervisor 12-bit SAR analog converter
  - 4 separate fast 12-bit SAR analog converters
  - 3 separate 10-bit SAR analog converters, one with STDBY mode support
  - 6 separate 16-bit Sigma-Delta analog converters
- Communication interfaces:
  - 18 LINFlexD modules
  - 10 deserial serial peripheral interface (DSPI) modules
  - 8 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support, one supporting time-triggered controller area network (TTCAN)
- Two Ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
- Flexible Power Supply options:
  - External Regulators (1.2 V core, 3.3 V–5 V IO)
  - Single internal SMPS regulator (eLQFP176)
  - Single internal Linear Regulator with external ballast (FPBGA292)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART

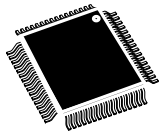
STM32F405xx
STM32F407xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

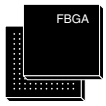
Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
- Up to 1 Mbyte of Flash memory
- Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
- Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.8 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power operation
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support



LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)

WLCSP90
(4.223x3.969 mm)



UFBGA176
(10 × 10 mm)

- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
  - Up to 3 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs (42 Mbits/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII

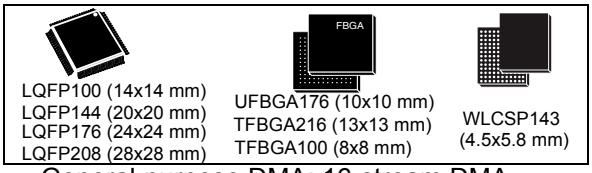
STM32F756xx

ARM®-based Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 1MB Flash/320+16+ 4KB RAM, crypto, USB OTG HS/FS, ethernet, 18 TIMs, 3 ADCs, 25 com itf, cam & LCD

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) and L1-cache: 4KB data cache and 4KB instruction cache, allowing 0-wait state execution from embedded Flash memory and external memories, frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
  - Up to 1MB of Flash memory
  - 1024 bytes of OTP memory
  - SRAM: 320KB (including 64KB of data TCM RAM for critical real-time data) + 16KB of instruction TCM RAM (for critical real-time routines) + 4KB of backup SRAM (available in the lowest power modes)
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller up to XGA resolution with dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 32×32 bit backup registers + 4KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer



LQFP100 (14x14 mm)
LQFP144 (20x20 mm)
LQFP176 (24x24 mm)
LQFP208 (28x28 mm)

UFBGA176 (10x10 mm)
TFBGA216 (13x13 mm)
TFBGA100 (8x8 mm)

WLCSP143
(4.5x5.8 mm)

- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 108 MHz
  - Up to 166 5 V-tolerant I/Os
- Up to 25 communication interfaces
  - Up to 4× I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (up to 50 Mbit/s), 3 with muxed simplex I^2S for audio class accuracy via internal audio PLL or external clock
  - 2 x SAIs (serial audio interface)
  - 2 × CANs (2.0B active) and SDMMC interface
  - SPDIFRX interface
  - HDMI-CEC
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbyte/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, triple DES, HASH (MD5, SHA-1, SHA-2), and HMAC
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F756xx	STM32F756VG, STM32F756ZG, STM32F756IG, STM32F756BG, STM32F756NG

STM32H750VB STM32H750IB STM32H750XB

32-bit Arm® Cortex®-M7 480MHz MCUs, 128 KB Flash, 1MB RAM, 46 com. and analog interfaces, crypto

Datasheet - production data

Features

Core

- 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache; frequency up to 480 MHz, MPU, 1027 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- 128 Kbytes of Flash memory
- 1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface running up to 133 MHz
- Flexible external memory controller with up to 32-bit data bus:
  - SRAM, PSRAM, NOR Flash memory clocked up to 133 MHz in synchronous mode
  - SDRAM/LPSDR SDRAM
  - 8/16-bit NAND Flash memories
- CRC calculation unit

Security

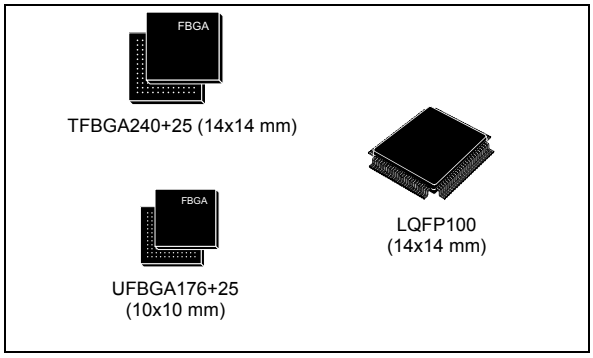
- ROP, PC-ROP, active tamper, secure firmware upgrade support, Secure access mode

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability

Reset and power management

- 3 separate power domains which can be independently clock-gated or switched off:
  - D1: high-performance capabilities
  - D2: communication peripherals and timers
  - D3: reset/clock control/power management
- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode (6 configurable ranges)
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral/V_{REF+}
- Low-power modes: Sleep, Stop, Standby and V_{BAT} supporting battery charging



Low-power consumption

- V_{BAT} battery operating mode with charging capability
- CPU and domain power state monitoring pins
- 2.95 µA in Standby mode (Backup SRAM OFF, RTC/LSE ON)

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-48 MHz HSE, 32.768 kHz LSE

- 3× PLLs (1 for the system clock, 2 for kernel clocks) with Fractional mode

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2-APB, 2× AXI2-AHB)

4 DMA controllers to unload the CPU

- 1× high-speed master direct memory access controller (MDMA) with linked list support
- 2× dual-port DMAs with FIFO
- 1× basic DMA with request router capabilities

Up to 35 communication peripherals

- 4× I2Cs FM+ interfaces (SMBus/PMBus)
- 4× USARTs/4x UARTs (ISO7816 interface, LIN, IrDA, up to 12.5 Mbit/s) and 1x LPUART
- 6× SPIs, 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock, 1x I2S in LP domain (up to 150 MHz)
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces (up to 125 MHz)
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS) crystal-less solution with LPM and BCD
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface (up to 80 MHz)

11 analog peripherals

- 3× ADCs with 16-bit max. resolution (up to 36 channels, up to 3.6 MSPS)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (7.3 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller up to XGA resolution
- Chrom-ART graphical hardware Accelerator™ (DMA2D) to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.1 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 240 MHz)
- 2× 16-bit advanced motor control timers (up to 240 MHz)
- 10× 16-bit general-purpose timers (up to 240 MHz)
- 5× 16-bit low-power timers (up to 240 MHz)
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy and hardware calendar

Cryptographic acceleration

- AES 128, 192, 256, TDES,
- HASH (MD5, SHA-1, SHA-2), HMAC
- True random number generators

Debug mode

- SWD & JTAG interfaces
- 4-Kbyte Embedded Trace Buffer

96-bit unique ID

All packages are ECOPACK®2 compliant

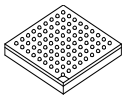
NXP Semiconductors

Data Sheet: Technical Data

Document Number: IMXRT1060IEC
Rev. 0.1, 04/2019

MIMXRT1061CVL5A **MIMXRT1062CVL5A**
MIMXRT1061CVJ5A **MIMXRT1062CVJ5A**

i.MX RT1060 Crossover Processors for Industrial Products



Package Information
Plastic Package
196-pin MAPBGA, 10 x 10 mm, 0.65 mm pitch
196-pin MAPBGA, 12 x 12 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 6

1 i.MX RT1060 Introduction

The i.MX RT1060 is a new processor family featuring NXP's advanced implementation of the Arm Cortex®-M7 core, which operates at speeds up to 528 MHz to provide high CPU performance and best real-time response.

The i.MX RT1060 processor has 1 MB on-chip RAM. 512 KB can be flexibly configured as TCM or general purpose on-chip RAM, while the other 512 KB is general-purpose on-chip RAM. The i.MX RT1060 integrates advanced power management module with DCDC and LDO that reduces complexity of external power supply and simplifies power sequencing. The i.MX RT1060 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX RT1060 has rich audio and video features, including LCD display, basic 2D graphics, camera interface, SPDIF, and I2S audio interface. The

i.MX RT1060 has analog interfaces, such as ADC, ACMP, and TSC.

The i.MX RT1060 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance

1.1 Features

The i.MX RT1060 processors are based on Arm Cortex-M7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-M7 MPCore with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Full featured Floating Point Unit (FPU) with support of the VFPv5 architecture
  - Support the Armv7-M Thumb instruction set
- Integrated MPU, up to 16 individual protection regions
- Tightly coupled GPIOs, operating at the same frequency as Arm
- Up to 512 KB I-TCM and D-TCM in total
- Frequency of 528 MHz
- Cortex M7 CoreSight™ components integration for debug
- Frequency of the core, as per Table 10, "Operating ranges," on page 22.

The SoC-level memory system consists of the following additional components:

  - Boot ROM (128 KB)
  - On-chip RAM (1 MB)
    - 512 KB OCRAM shared between ITCM/DTCM and OCRAM
    - Dedicate 512 KB OCRAM
- External memory interfaces:
  - 8/16-bit SDRAM, up to SDRAM-133/SDRAM-166
  - 8/16-bit SLC NAND FLASH, with ECC handled in software
  - SD/eMMC
  - SPI NOR FLASH
  - Parallel NOR FLASH with XIP support
  - Two single/dual channel Quad SPI FLASH with XIP support
- Timers and PWMs:
  - Two General Programmable Timers (GPT)
    - 4-channel generic 32-bit resolution timer for each
    - Each support standard capture and compare operation
  - Four Periodical Interrupt Timers (PIT)

  - Generic 32-bit resolution timer
  - Periodical interrupt generation
- Four Quad Timers (QTimer)
  - 4-channel generic 16-bit resolution timer for each
  - Each support standard capture and compare operation
  - Quadrature decoder integrated
- Four FlexPWMs
  - Up to 8 individual PWM channels per each
  - 16-bit resolution PWM suitable for Motor Control applications
- Four Quadrature Encoder/Decoders

Each i.MX RT1060 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
  - Parallel RGB LCD interface
    - Support 8/16/24 bit interface
    - Support up to WXGA resolution
    - Support Index color with 256 entry x 24 bit color LUT
    - Smart LCD display with 8/16-bit MPU/8080 interface
- Audio:
  - S/PDIF input and output
  - Three synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
  - MQS interface for medium quality audio via GPIO pads
- Generic 2D graphics engine:
  - BitBlit
  - Flexible image composition options—alpha, chroma key
  - Porter-duff blending
  - Image rotation (90˚, 180˚, 270˚)
  - Image size
  - Color space conversion
  - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
  - Standard 2D-DMA operation
- Camera sensors:
  - Support 24-bit, 16-bit, and 8-bit CSI input
- Connectivity:
  - Two USB 2.0 OTG controllers with integrated PHY interfaces
  - Two Ultra Secure Digital Host Controller (uSDHC) interfaces

S32K1XX

S32K1xx Data Sheet

Notes

- The following two attachments are available with the Datasheet:
  - S32K1xx_Orderable_Part_Number_ List.xlsx
  - S32K1xx_Power_Modes_Configuration.xlsx

Key Features

- Operating characteristics
  - Voltage range: 2.7 V to 5.5 V
  - Ambient temperature range: -40 °C to 105 °C for HSRUN mode, -40 °C to 125 °C for RUN mode
- Arm™ Cortex-M4F/M0+ core, 32-bit CPU
  - Supports up to 112 MHz frequency (HSRUN mode) with 1.25 Dhrystone MIPS per MHz
  - Arm Core based on the Armv7 Architecture and Thumb®-2 ISA
  - Integrated Digital Signal Processor (DSP)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single Precision Floating Point Unit (FPU)
- Clock interfaces
  - 4 - 40 MHz fast external oscillator (SOSC) with up to 50 MHz DC external square input clock in external clock mode
  - 48 MHz Fast Internal RC oscillator (FIRC)
  - 8 MHz Slow Internal RC oscillator (SIRC)
  - 128 kHz Low Power Oscillator (LPO)
  - Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
  - Up to 20 MHz TCLK and 25 MHz SWD_CLK
  - 32 kHz Real Time Counter external clock (RTC_CLKIN)
- Power management
  - Low-power Arm Cortex-M4F/M0+ core with excellent energy efficiency
  - Power Management Controller (PMC) with multiple power modes: HSRUN, RUN, STOP, VLPR, and VLPS. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 Mhz) to execute CSEc (Security) or EEPROM writes/erase.
  - Clock gating and low power operation supported on specific peripherals.
- Memory and memory interfaces
  - Up to 2 MB program flash memory with ECC
  - 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - Up to 256 KB SRAM with ECC
  - Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
  - Up to 4 KB Code cache to minimize performance impact of memory access latencies
  - QuadSPI with HyperBus™ support
- Mixed-signal analog
  - Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module
  - One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)
- Debug functionality
  - Serial Wire JTAG Debug Port (SWJ-DP) combines
  - Debug Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Test Port Interface Unit (TPIU)
  - Flash Patch and Breakpoint (FPB) Unit
- Human-machine interface (HMI)
  - Up to 156 GPIO pins with interrupt functionality
  - Non-Maskable Interrupt (NMI)

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

RX72M Group
Renesas MCUs

R01DS0332EJ0100
Rev.1.00
May 31, 2019

240-MHz 32-bit RX MCU, on-chip double-precision FPU, 1396 CoreMark, Arithmetic unit for trigonometric functions, up to 4-MB flash memory (supportive of the dual bank function), 1-MB SRAM, EtherCAT Slave Controller, various communications interfaces including Ethernet MAC compliant with IEEE 1588, SD host interface, quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions (optional), Serial sound interface, CMOS camera interface, Graphic-LCD controller, 2D drawing engine

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 240 MHz
  Capable of 1396 CoreMark in operation at 240 MHz
- Double-precision 64-bit IEEE-754 floating point
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

■ On-chip code flash memory
- Supports versions with up to 4 Mbytes of ROM
- No wait cycles at up to 120 MHz or when the ROM cache is hit, one-wait state at above 120 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 1 Mbyte of SRAM (no wait states; however, if ICLK is at a frequency above 120 MHz, access to locations in the 512 Kbytes of SRAM from 0080 0000h to 0087 FFFFh requires one cycle of waiting)
- 32 Kbytes of RAM with ECC (single error correction/double error detection)
- 8 Kbytes of standby RAM (backup on deep software standby)

■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 3 channels

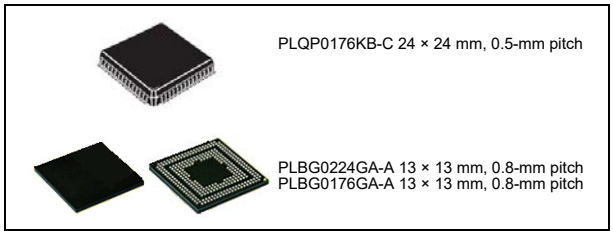
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- PLL for specific purposes
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

■ Independent watchdog timer
- 120-kHz clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.


PLQP0176KB-C 24 × 24 mm, 0.5-mm pitch

PLBG0224GA-A 13 × 13 mm, 0.8-mm pitch
PLBG0176GA-A 13 × 13 mm, 0.8-mm pitch

■ Various communications interfaces
- EtherCAT slave controller (two ports)
- Ethernet MAC compliant with IEEE 1588 (2 channels)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (3 channels)
- SCIj and SCIh with multiple functionalities (8 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (5 channels)
- I^2C bus interface for transfer at up to 1 Mbps (3 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- MMCIF with 1-, 4-, or 8-bit transfer bus width

■ External address space
- Buses for full-speed data transfer (max. operating frequency of 80 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Up to 29 extended-function timers
- 32-bit GPTW (4 channels)
- 16-bit TPUa (6 channels), MTU3a (9 channels)
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

■ 12-bit D/A converter: 2 channels

■ Temperature sensor for measuring temperature within the chip

■ Arithmetic unit for trigonometric functions

■ Delta-Sigma Modulator Interface
- Six external delta-sigma modulators are connectable

■ Encryption functions (optional)
- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

■ Up to 182 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

Chapter 1

FE310-G002 Description

1.1 Features

- SiFive E31 Core Complex up to 320MHz.
- Flexible clocking options including internal PLL, free-running ring oscillator and external 16MHz crystal.
- 1.61 DMIPs/MHz, 2.73 Coremark/MHz
- RV32IMAC
- 8kB OTP Program Memory
- 8kB Mask ROM
- 16kB Instruction Cache
- 16kB Data SRAM
- 3 Independent PWM Controllers
- External RESET pin
- JTAG, SPI I2C, and UART interfaces.
- QSPI Flash interface.
- Requires 1.8V and 3.3V supplies.
- Hardware Multiply and Divide

1.2 Description

The FE310-G002 is the second Freedom E300 SoC. The FE310-G002 is built around the E31 Core Complex instantiated in the Freedom E300 platform.

The *FE310-G002 Manual* should be read together with this datasheet. This datasheet provides electrical specifications and an overview of the FE310-G002.

The FE310-G002 comes in a convenient, industry standard 6x6mm 48-lead QFN package (0.4mm pad pitch).