RX72M Group
Renesas MCUs

R01DS0332EJ0100
Rev.1.00
May 31, 2019

240-MHz 32-bit RX MCU, on-chip double-precision FPU, 1396 CoreMark, Arithmetic unit for trigonometric functions, up to 4-MB flash memory (supportive of the dual bank function), 1-MB SRAM, EtherCAT Slave Controller, various communications interfaces including Ethernet MAC compliant with IEEE 1588, SD host interface, quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions (optional), Serial sound interface, CMOS camera interface, Graphic-LCD controller, 2D drawing engine

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 240 MHz
  Capable of 1396 CoreMark in operation at 240 MHz
- Double-precision 64-bit IEEE-754 floating point
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

■ On-chip code flash memory
- Supports versions with up to 4 Mbytes of ROM
- No wait cycles at up to 120 MHz or when the ROM cache is hit, one-wait state at above 120 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 1 Mbyte of SRAM (no wait states; however, if ICLK is at a frequency above 120 MHz, access to locations in the 512 Kbytes of SRAM from 0080 0000h to 0087 FFFFh requires one cycle of waiting)
- 32 Kbytes of RAM with ECC (single error correction/double error detection)
- 8 Kbytes of standby RAM (backup on deep software standby)

■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 3 channels

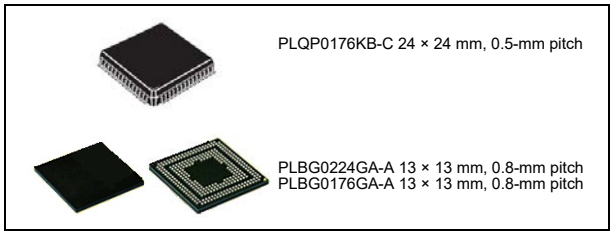
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- PLL for specific purposes
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

■ Independent watchdog timer
- 120-kHz clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.


PLQP0176KB-C 24 × 24 mm, 0.5-mm pitch
PLBG0224GA-A 13 × 13 mm, 0.8-mm pitch
PLBG0176GA-A 13 × 13 mm, 0.8-mm pitch

■ Various communications interfaces
- EtherCAT slave controller (two ports)
- Ethernet MAC compliant with IEEE 1588 (2 channels)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (3 channels)
- SCIj and SCIh with multiple functionalities (8 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (5 channels)
- I^2C bus interface for transfer at up to 1 Mbps (3 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- MMCIF with 1-, 4-, or 8-bit transfer bus width

■ External address space
- Buses for full-speed data transfer (max. operating frequency of 80 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Up to 29 extended-function timers
- 32-bit GPTW (4 channels)
- 16-bit TPUa (6 channels), MTU3a (9 channels)
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

■ 12-bit D/A converter: 2 channels

■ Temperature sensor for measuring temperature within the chip

■ Arithmetic unit for trigonometric functions

■ Delta-Sigma Modulator Interface
- Six external delta-sigma modulators are connectable

■ Encryption functions (optional)
- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

■ Up to 182 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C