A flexible stand-alone FPGA-based ATE for ASIC manufacturing tests

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***Abstract*—Technology scaling made possible to increase IC capabilities from one node to the next by adding more transistors within the same die area while keeping a low pin count. As a consequence, test complexity increased exponentially, requiring engineers to use not only better test pattern generation software, but also powerful and expensive Automatic-Test-Equipments (ATE), usually not viable and accessible for small fabless start-ups and universities. In this work, we propose a low-cost and flexible ATE intended for manufacturing tests of the digital part of a multi-million gate industrial mixed signal ASIC produced in a 130nm technology that will be used at CERN in the ALICE experiment. The proposed ATE was built upon a ready-to-use platform including an embedded processor ARM-based and an FPGA to effectively apply the test vectors via the Device-Under-Test (DUT) scan chains in a feasible time and viable cost without the need for a PC. The ATE was operated to execute in-series manufacturing tests on two versions of the SAMPA chip, allowing identifying on-silicon defects.**

***Keywords*—FPGA-based ATE, Manufacturing tests, Low-cost, Flexible, Stand-alone**

I. Introduction

Continuous technology scaling and complexity increasing of integrated circuits make the verification and validation tasks a bottleneck in the microelectronic production flow. Complex digital circuits employ Design-for-Test structures (DfT), more typically scan-chains, to facilitate the final silicon validation procedures by improving the controllability and observability of internal gates and electrical wires in order to check whether a chip has any defects stemmed from the manufacturing process [1]. The importance of test is to identify any issue as soon as possible immediately after the manufacturing process in order to screen out bad components or chips from good ones and prevent them from being assembled, which could imply on an exponentially increasing cost (a.k.a *rule of 10*) as the product reaches the final customer.

There are some companies that provide proper equipment or ATE to apply all types of tests vectors, from analog to digital ones, on a DUT, such as Advantest and Teradyne. However, such ATEs are expensive to acquire or hire during the post-silicon validation phase, and are usually employed during manufacturing tests on a large production. For example, they are most typically suitable to be used on a validated design and when test sequences demonstrate to cover all chip functionality, i.e. manufacturing issues, analog and digital measurements, current and high-speed tests execution, etc. The design validation cost of a complex ASIC can add up to 40% of the cost of the total chip project [2] when considering to contract specialized test companies. Whereas final in-series manufacturing tests on validated design and methods can sum up to 10%. In the last decades, an increasing number of small companies or startups designing ASICs emerged, and considering a tight budget, they looked for cheaper solutions to validate and test their manufactured chips. A good solution example is provided by Teseda [3], that is considered to provided low-cost focused testers (Tesedas V500 approximate cost is $60K) according to [4]. Moreover, research work as [5] developed its own ATE for preliminary digital testing on a very reduced scale, in particular for design validation of several samples.

The SAMPA is a custom front-end ASIC for gaseous detectors readout which formats and amplifies the charge signal induced on pads connected to its inputs into digital Semi-Gaussian pulses [6], [7]. It integrates 32 channels per chip of the full data processing chain and supports continuous and triggered read-out modes. The acquired data are transferred to a GBTx ASIC (described in [8]) via up to eleven SLVS (Scalable Low Voltage Signaling)links, which multiplex and transmit them via versatile optical link components to a Common Readout Unit. The SAMPA ASIC was designed by the *Laboratorio de Sistemas Integraveis* (LSI) at the University of So Paulo (USP) and produced in a 130nm CMOS technology at TSMC. It is important to mention that to keep SAMPA costs within budget, the wafer testing at TSMC was dispensed, hence a wafer map [9] informing the good and bad dice could not be provided. In this case, all dice were packaged regardless if they had visual defects or not and therefore, all packaged samples must undergo testing as part of the manufacturing validation process before qualification tests and applied in field.

Primary motivated by the necessity of providing a quick and cheap solution for validating SAMPA and secondary by similar low-cost test solution proposed by other related works, furthermore justified from the missing wafer map fact; In this work, we propose a low-cost and flexible in-house ATE to validate and elaborate in-series tests of a population of the manufactured SAMPA ASIC. The proposed solution is an FPGA-based ATE implemented upon a cutting-edge SoC (System-on-Chip) development platform, known as SOCKIT. It integrates an ARM-based Hard Processor System (HPS) consisting of a CPU, several peripherals and memory interfaces with a dedicated FPGA, all tightly connected within the semiconductor fabric. Additionally, we exploited the High-Speed Mezzanine Connector (HSMC) interface to bridge the connections between the SAMPA ASIC board and the proposed ATE in order to fulfill the test requirements of frequency and I/O pins connections. Finally, we exploit the ATE to screen-out defective SAMPA dice from good ones, allowing further tests.

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The rest of this paper is organized as follow: Section II describes backgrounds on the SAMPA ASIC, the DfT design, test vectors generation and some ATE options and related works. Section III includes the proposed ATE characteristics and addresses the steps and challenges to implement a low-cost ATE solution, explaining the developed FPGA project and test application software. In section IV we show some results of the proposed ATE and its application to execute in-series manufacturing tests of two versions of the SAMPA ASIC and finally we draw conclusions in section V.

II. Background

A. SAMPA ASIC

The ALICE experiment will upgrade its time projection chamber (TPC) detector during the long shutdown of CERNs Large Hadron Collider, foreseen to start in 2019 [10]. In the upgraded TPC, the gas electron multiplier (GEM) technology and continuous readout will replace the existing technology. The GEM signals will be processed using the SAMPA ASIC, new custom designed mixed signal front-end chip.

The diagram of the SAMPA architecture is shown in figure 1 and it is composed of different analog and digital blocks. The analog part includes the Charge Sensitive Amplifier (CSA) , Shaper, Band gap, bias and Analog-to-Digital Converter(ADCs).The digital part is comprised of only one block: the DSP. Looking to 1,from left to right, the signals are acquired by the analog inputs, then amplified, filtered, shaped and finally digitized by the ADC to interface with the DSP.

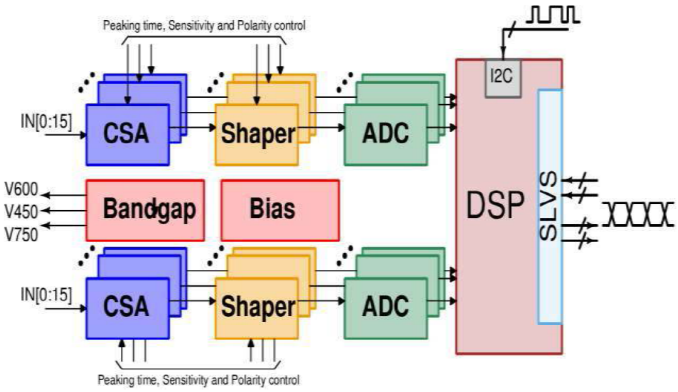

Fig. 1. Block Diagram of the SAMPA ASIC

The data sent by SAMPA consists of a fixed length header and variable length data payloads, both combined form a packet. The data are written the least significant bit first on rising edge of the clock. The data payload contains zero-suppressed and runs length encoded samples to save space and bandwidth in the communication links.

Due to SAMPA's size and complexity, the layout flow took special attention to the signal integrity requirement. During the digital layout flow, extra space was added for comfortable routing the clock trees, e.g. clkADCin, clkBXin, clkSOin, as well as for DfT, in particular, scan chain stitching of the signals SDI, SDO, SEN and TRSTs.

The described strategy is a simple and effective solution to avoid cross-talk between the nets with a high level of variation, like the clock nets. The routing layer of the reset (Hrstb) and the power-on automatic reset (PORin) signals were controlled in order to prevent the nets to pass excessive noise to memory IPs, also avoiding crosstalk and failures due to aggressor induced effects in this kind of susceptible signals.

The first version of SAMPA, considering only the analog blocks, was delivered in 2014. In 2016 the second version was produced with all blocks included (Analog and Digital). Finally, the third version of SAMPA was concluded in 2017 with improvements and corrections.

B. DfT Design

Traditionally, design and test processes were kept separate, with test considered only at the end of the design cycle. However, in contemporary design flows, test merges with the design much earlier in the design flow, creating the already mentioned DfT. DfT is a technique sought to borrow a small IC space in the design to greatly reduce test complications by improving the ATE's ability to quickly apply effective test patterns and detect failing parts. DfT does not perform the design functional verification, once it is done by simulations. The most vastly used DfT technique is the scan-chain, whose target is to be sure that there are no defects on the IC's gates or nets, e.g. shorts or opens due to the errors in the manufacturing process usually caused by misplaced impure particles.

The scan-chain method provides testability with a controlled scan chain that inserts stimuli into the internal state elements of the design. According to [11] the scan chain could be designed either as a dedicated scan path or functional scan path. The functional scan path architecture tries to organize the sequential elements of the design into the scan chain by utilizing existing flip-flops as much as possible, instead of inserting additional hardware into the project.

The SAMPA uses the functional scan path and has implemented five scan chains. The average length of the five scan chains was 24259 scan flip-flops for SAMPA V2 and 24596 for SAMPA V3. There are five pins for scan in (sdi), five pins for scan out (sdo), five pins for scan enable (ena) and a specified clock for the DfT bits insertion and shift. The constraints of this DfT clock were taken into account during the back end flow as well.

C. Vector Tests Generation - Encounter Test

As the first step to perform an in-house test of the manufactured SAMPA, test vectors were elaborated by the Cadence ATPG tool, named Encounter Test (ET). In the ET must be defined the design netlist, the technology libraries used during the synthesis, the SAMPA pin assignment file and also a pin exclusion file, which removes unaccessible digital pins, for example, the input pins of the ADC. The DfT design during the digital block development defines the maximum coverage possible related to the number of scan chains and its flip-flops. Moreover, the ET property configured also influences in the final coverage.

This work focus on the single stuck-at fault model, which is able to identify defects as shorts between a signal and VCC

(stuck-at-1) or a signal and GND (stuck-at-0) taking place within a manufactured integrated circuit. Due to its simplicity, it offers many advantages in fault detection, i.e. covers a large portion of manufacturing defects and algorithms and tools for generation stuck-at patterns are well-developed and very efficient [12]. Also, [11] mention that this is the most commonly used fault model.

The ET generated two set of test vectors file. One of them is a short test vector intended to test the scan chains integrity quickly. The other is the full test with all sequences of stimuli aimed for the highest coverage of stuck at faults. The generated test vectors for SAMPA are defined as multi-dimensional, once the inputs sequences are independents, which means, each applied sequence of the test vector file to the IC has a well-defined stimulation target, i.e. some gates implementing a specific logic or state elements, allowing confirming the proper production.

D. Automatic Test Equipment - ATE

ATEs are typically used in the last step of the ASIC manufacturing process flow with the following goals:

- to facilitate post-silicon validation
- to execute manufacturing tests
- to allow diagnosis and correction
- to gather valuable information for manufacturing process refinement

In post-silicon validation tasks (usually known as bring-up), the ATE is configured to exercise the ASIC w.r.t. design and manufacturing specifications to prove design and fabrication process correctness. In this phase, several different lab equipment and ATEs may be employed to collect valuable test information. Whereas manufacturing tests use the configured ATE to apply structural test sequences on a production population of ASICs to screen-out defective chips from good ones. Note that these tasks are linked and must be carefully planned and executed, otherwise too much testing may lead to production overkill and too little will allow test escapes. In either situation the manufacturer will have economic loss.

Furthermore, the ATE may also be employed to perform on-the-fly diagnosis and quickly correct the ASICs w.r.t specifications by tweaking on-silicon configurations, or permanently disable defective parts and replace with good ones, e.g. memory cells. In addition, the ATE applies tests to every manufactured IC and can collect valuable information over time used for refining the manufacturing process or even helping to reduce unnecessary costs. For example, when test results show that some dice are failing because of their position on the wafer caused by mask misalignment. This knowledge helps test engineers to select only the so-called *known-good-dies* for packaging, thus reducing costs from the early stages in the manufacturing process back-end.

The technology shrink made possible to include more transistors per mm^2 on silicon, thus increasing IC capabilities from one technology node to the next. As a consequence, test complexity also scaled exponentially due to the quadratically increasing number of internal nodes while keeping a similar amount of pins, hence making test procedures a major quality and cost concern for semiconductor companies, especially when dealing with increased ATE processing power and test time. On the other hand, reduced chips with increased capabilities allowed the insurgence of even smaller high performance embedded computers which in turn have been employed to implement low-cost ATEs. Additionally to increasingly exploitation of DfT techniques to aid test generation and application, low-cost ATEs have become a viable solution for fabless semiconductor start-ups and universities to reduce costs. Such scenario made possible the co-existence of several ATEs in a test ecosystem with several types of testers targeting different strategies based on circuit complexity, test time, test volume and costs.

Table I shows ATE types and their characteristics as cost, test data volume, test DUT quantity per year and overall data transfer rate.

TABLE I. ATE TYPES

Type	Cost ($)	Test Data Vol.(GB)	Product. Vol./Yr	Data rate
Big Iron	>1000K	10^{12}	>1M	>5Gbps
Medium iron	300K-1000K	10^{6}	< 1M	<5Gbps
Custom commercial	10K-300K	10^{6}	< 100K	<1Gbps
Custom low-cost	< 10K	10^{3}	< 30K	<300Mpbs

Big iron ATEs are the most expensive testers because they are comparable to main frame computers and may provide up to thousands of usable pins to apply test patterns concurrently to many units-under-test (UUT). Not only they account on state-of-the-art proprietary software for elaborating test sequences and analyzing results, but also to implement most test protocols compatible with industry test standards. They are usually used by semiconductor companies delivering more than 10M units per year. Medium iron and custom commercial ATEs can also deliver comparable results to big iron. The former uses less computing power and it is usually dedicated for medium production volume up to 1M units per year. The latter, on the other hand, is customized for very specific niche ICs that requires proprietary information such as design and communication protocols. This is the case for memory and security ICs, where secrecy is the key for a successful product. All the above mentioned ATEs are already mature products that have undergone thorough product validation and, once in operation, they may also exploit handlers to reduce test time, by speeding-up the UUT's loading and unloading tasks.

The most recent type of ATEs, as shown in the last row of table I, is the low-cost one. It has become a viable solution for fabless companies and universities whenever a small number of prototypes or production of ASICs need to be tested. For instance, it is suitable for the IC bring-up phase as well as in-series manufacturing tests on a very low-volume production, i.e. reaching up to thousands of units per year. The main drawback of this type of ATE is that it needs to be developed almost from scratch, which may cause quality and test time concerns due to repetitive validation tasks on the platform itself before using it on the DUT. Thanks to the increasing number of easy-to-use reconfigurable development boards including state-of-the-art electronic components that were made available in the past decade, developing a low-cost tester has become much easier to implement within a reasonable time.

Following the perspective on the development of low-cost ATE, in the literature several successful attempts have been made in the past with different strategies [13] [5]. In [13], the authors developed an FPGA-based ATE to test in series a small production of SoCs embedding an 8051 CPU core. Using a computer, they were able to transfer data across to the platform and initiate test sequences. Besides developing the ATE, they tackled the main problem with testing SoCs and their framework: test data volume. In particular, at the time their ATE was implemented, they had available an embedded SoC running embedded linux to control communication between the host pc and the FPGA manipulating the test pins. Moreover, they did not have enough storage for keeping the test patterns and retrieving large amounts of data through a slow communication channel. So, they solved this issue by implementing test data compression as well as optimizing the test data set by pruning redundant test patterns. Their overall methodology was capable of achieving a compression ratio of 69%, thus making the platform useful for SoC in series testing.

In [5], the authors proposed a low-cost FPGA-based ATE for testing digital ICs. Their architecture was implemented on a development board including a Xilinx Spartan 3 FPGA, which proved to be cost and test effective for their study case. This is especially true, because commercial ATEs were not an option due to the excessive costs. Also, it relied on a computer communicating to the FPGA development board via USB to RS232 serial connection, which included some peripherals and a dedicated FSM as the main controller.

III. Proposed ATE

In this paper, we propose an FPGA-based ATE suitable for applying in-series manufacturing tests able to identify stuck at and transition faults or even delay on a small population of the ASIC SAMPA, previously described in section II. In particular, the proposed ATE must include characteristics not yet exploited in the custom low-cost ATE domain and are listed below:

- *Flexibility* - Allows easy reconfiguration of the system to test different designs
- *Stand-alone* - Capability of automatically applying tests and saving cumulative results with minimal or no computer interaction during testing all DUTs
- *Fast data transfer* - Ability to transfer large volume of test data via a fast communication channel (Ethernet) or removable storage devices (SD cards)
- *BGA support* - The target DUT has a BGA package, hence the ATE must include proper connections
- *Easy-of-use* - DUT Loading, test application, results collection and DUT unloading must be very easily and reliably executed
- *Low-cost* - Uses cutting-edge Components-Off-The-Shelf (COTS) to keep costs within project budget while allowing other institutions to replicate the same ATE principles.

The following subsections give better details about the proposed ATE implementation, operation, FPGA and C application core functions to configure pins and apply test sequences.

A. Implementation

In order to implement a dedicated ATE with the features listed above, we resorted to the SOCKIT development board [14] supplied by Terasic. It includes an SoC that integrates an FPGA Cyclone V SX tightly connected with a Dual-Core ARM Cortex - A9 HPS within the semiconductor fabric. The HPS memory interface is connected transparently with the FPGA via a high-bandwidth interconnect backbone, namely Avalon. The interface between ATE and SAMPA boards was done via the HSMC, which allows quickly applying the test vectors on high-frequency SAMPA samples. The ATE-to-SAMPA connection is addressed via some test pins: scan-in, scan-out, scan enable and the scan clock, which is the most important. The ATE block diagram is shown in 2 whose main blocks are numbered from 1 to 5 to allow better understanding of the data flow.

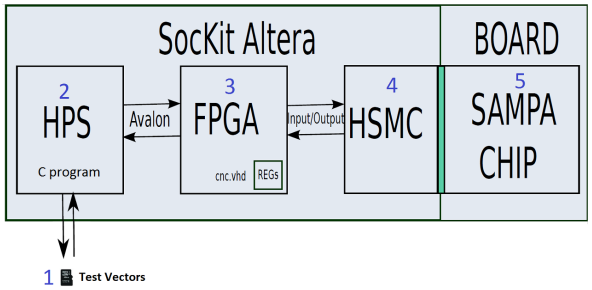

Fig. 2. ATE block diagram.

B. Operation

Additionally, an embedded Linaro-based Linux image was uploaded to the system to be executed in the HPS, thus adding core software functions for easily handling peripherals and communication ports. We also implemented a C application capable of parsing test information to correctly configure the development board to actually become the flexible ATE, which will be better explained in the following subsections. Once the everything is connected together and the operating system and C program are running, the system is ready for use. Taken into consideration Fig.2, the ATE is operated as follows:

1) The test vector file generated with ET is copied to the SD card (1) via USB or Ethernet
2) A C program running in (2) reads a sequence, i.e a stimuli, from the test vector file to be applied
3) Via FPGA (3) the C program apply the stimuli in the HSMC (4) pins
4) The SAMPA board (5) apply the stimuli to the chip and the correspondent answer is write back in the HSMC interface
5) The FPGA reads the SAMPA chip answer and write in a memory
6) The C program reads the answer and compare with the expected values.
7) If any value is different a led start to blink and a log file is generated. If not, the C program read the next sequence and the flow repeat.

8) As soon as the test vector is read and the stimuli insertion were concluded successfully another LED lights up.

The execution from 1 to 7 correspond to a cycle of one sequence in the test vector file and will be later explained.

Note that it is possible to operate the ATE in its stand-alone form by using only one SD card containing the test sequence information and the FPGA configuration, which can be flexibly re-configured for different designs. Both informations are enough to repeatedly use the ATE for testing a small production of ASICs without resorting to a computer. Nonetheless, if one may find useful, the system also allows the user to connect to the ATE via ethernet and view verbose information.

C. FPGA project

The FPGA project developed for our ATE can be described as the merge of the HPS, the Avalon bus and bus connected peripheral blocks. The Avalon Memory-Mapped (MM) is one important bus interface. It uses a master-slave protocol, with a CPU, i.e. HPS, being the master and the peripherals being the slaves [15].

A part of the RAM memory that the HPS access can be mapped to be exposed to the Avalon bus and other kinds of interconnect providing a direct way for writing and reading data from the linux memory space to the FPGA. This is a method known as memory-mapped I/O.

In this way, the I/O access to the SAMPA chip during the test were transparent to the C program. Moreover, this mapping is easy to be changed in the case of a new test chip with different pins organization.

Hence, to insert the stimuli in the SAMPA chip and scan the answers from the differential pairs of the HSMC, a peripheral connected to the Avalon was developed and synthesized. To interconnect the developed peripheral was used the Qsys tool, once it saves time and effort in the system design process, helping to generate interconnect logic to weld HPS, intellectual property (IP) functions, subsystems and peripherals.

D. C program - Pattern injection

The C program flow developed to insert the test vectors is summarized in the figure 3, being that there are tree main stages: the first cycle, a loop with many cycles, that depends of the number of sequences, and the last cycle.

During the first cycle, the values of the primary inputs (stim_PIs) and primary outputs (resp_POs) are inserted, which correspond the values of the input and output pins not related to the scan chain. Those values are used to increase the coverage once they activate different state elements for different values. Moving forward, the five scan chains are enabled and a sequence is inserted concluding the first cycle.

After the first cycle, there is a loop that inserts all test sequences and compare the results of resp_POS and the scan out. The first procedure is the comparison of the RESP, namely Test_Cycle. If some of the 96 primary outputs used of the SAMPA responses a wrong value, the test stops and reports an error, flashing a led on the SOCKIT board. Else, new primary inputs and primary outputs are inserted for the next cycle. Next, the scan chain is enabled and the vectors are inserted and the scan response is compared. It is a very iterative process, since each bit is inserted it generates a bit output in the scan out. If some value is different from the expected, the test stops and reports an error, also flashing the SOCKIT led.

The last cycle performs only the comparison for the values already inserted in the scan chain and primary inputs.

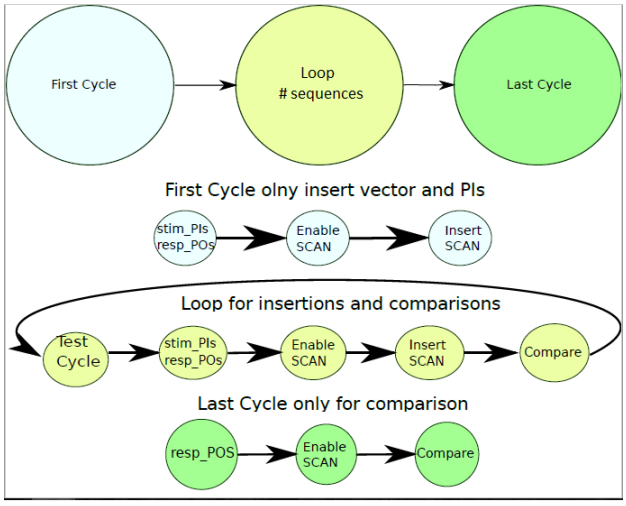

Fig. 3. Pattern injection program flow.

IV. Experimental Results

The two versions of the SAMPA ASIC were produced and encapsulated by TSMC, been SAMPA V2 in 2016 and SAMPA V3 in 2017. Both BGA chips were assembled in a socket board to perform the tests. The real system described in the block diagram 2 and the socket board is shown in the picture 4

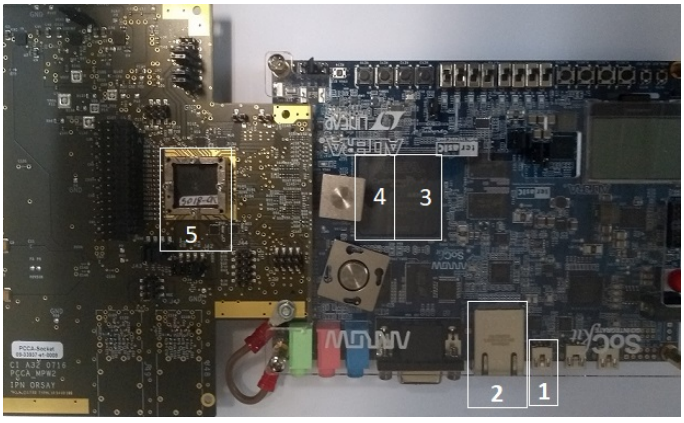

Fig. 4. ATE connected to the socket board with one SAMPA package.

In Fig.4 a photo of the proposed ATE is shown. The enumerated parts correspond to: (1) USB emulated UART connection, (2) Ethernet port, (3) HPS in the same package as (4) FPGA, and finally (5) the BGA socket including the DUT SAMPA ASIC.

Once the ATE is configured in stand-alone mode, the only two required operations to complete in-series manufacturing tests are the manual replacement of each SAMPA sample connected to the ZIF BGA socket and restart the ATE.

The characteristics of the developed ATE are:

- Cost: $1K (SOCKIT and socket boards)
- Test Data Volume: 16GB (200MB for test vectors file and 15GB for cumulative results)
- Tests: 120 units/day (30K units/year)
- Data Rate: 20 Mbps

Figure 5 shows the screen log of the successful ATE execution of a short test vector being monitored via Secure Shell (SSH) using the Ethernet connection.

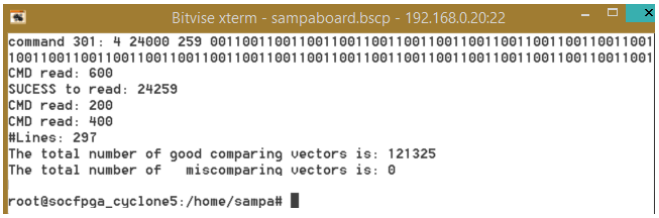

Fig. 5. Screen of one successful test execution.

A. SAMPA V2 and V3

The ATE was used by four test centers in order to validate both SAMPA ASIC versions: Sao Paulo - USP, Orsay - IN2P3, Lund University and Dubna - JINR.

Considering SAMPA V2 and its generated test vectors, the ATE execution spent around 60s to complete the validation of each chip. USP and Orsay have tested 80 SAMPA samples. The short test vector identified six of them with scan integrity problems. Besides that, the full test file was applied and a total of eight chips have failed, showing stuck-at faults by determining test miss compares with golden results. The yield for the SAMPA V2 was around 80%.

For SAMPA V3 version, the software was upgraded because the scan chains size increased by some bits. Moreover, for the this version, we elaborated new test vectors using the Cadence ATPG tool ET. The ATE test time to validate a SAMPA V3 ASIC was around 40s. The results are summarized in the table II:

TABLE II. SAMPA V3 TEST RESULTS

Test Center	#SAMPA ASIC	Yield
SAO PAULO	99	89%
Orsay	29	90%
Lund	115	81%
Dubna	22	82%

The time to reconfigure the ATE from one SAMPA version to another was basically the ATPG operation to create the new set of test vectors and quickly reconfigure pins, which in this case was not necessary. Thus demonstrating the flexibility of the proposed ATE to go from testing one design to another.

Some of the SAMPA V3 tested at USP are shown in the picture 6, were is possible to realize the labels identifying the good and one bad socket chips. The picture also shows the BGA balls layout.

Fig. 6. Photo of the tested SAMPA BGA encapsulated.

V. CONCLUSIONS

This work presented the development and usage of an ATE able to validate an industrial ASIC by applying multi-dimensional test vectors in a feasible time, ensuring a satisfactory number of tested chips. The proposed ATE is an in-house flexible stand-alone FPGA-based solution, which is significantly low-cost, intended to test a series of manufactured SAMPA ASICs, where the costs for a dedicated enterprise solution would not worth the deal. Our results support the usage of the ATE once it had success identifying defective SAMPA samples with stuck-at failures. Due to the ATE and the easy-to-use socket interface board connected to the HSCM connector, hundreds of chips could be quickly tested, showing that the achieved manufacturing yield was in the range of 80-90%. The ATE proved effective for applying initial manufacturing tests and was distributed to 3 more involved test centers,thus allowing selecting good dice to perform qualification tests and to be further used in the CERN ALICE experiment.

VI. ACKNOWLEDGMENTS

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