On-Silicon Validation of a Benchmark Generation Methodology for Effectively Evaluating Combinational Cell Library Design

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Abstract — This work presents the validation in silicon of a test chip for the evaluation of ensembles of combinational CMOS gates (cell library). The design methodology and the architecture of this simple, efficient and easy-to-use test circuit were already proposed theoretically in the past, having been demonstrated its functionality only through partial electrical simulations. The fabrication and measurements over on-silicon prototype provide important information about design improvement possibilities of such a test circuit and its architecture. The results are presented and discussed in this paper.

Index Terms—CMOS logic circuit, circuit testing, standard cell library, measurements.

I. Introduction

The cell-based approach is definitely the most applied strategy in ASIC design. This top-down IC design methodology considers the reuse of library cells to build more complex digital circuits. As the technology mapping task in standard cells IC design flow is based on pre-characterized data of pre-designed logic gates, the ASIC design space and efficiency turns to be bounded by the profile of the target library. The availability of different logic functions and cell drive strength options potentially increases the possibilities for design quality improvement [1-6]. In standard cell libraries, three groups of logic gates co-exist: (1) inverters/buffers; (2) combinational cells and (3) storage elements (latches and flip-flops). Mainly due to the large number of different Boolean functions and driving strength options needed for typical designs, the largest of the three aforementioned groups is naturally the one of combinational gates.

However, on-silicon validation of logic gates in terms of functionality and performance is marketed as a competitive reliability advantage before using them into consumer products. Different methods for silicon validation are presented in [7-12]. In [12], the authors proposed an effective methodology to automatically produce a test circuit for complete functional and electrical validation of an ensemble of logic gates. It presents a straightforward operation and monitoring procedure. At the silicon level, the main goal is to provide a solution with limited number of I/O pads and minimum use of ATPG (Automatic Test Pattern Generation) tools, reducing significantly the test engineering cost to on-silicon test for physical verification. Additionally, the test circuit can serve as a degradation monitoring scheme to evaluate the impact in design of emerging sub-nanometer aging mechanisms, due to the easy intermittent running in self-timed mode. Finally, a diagnosis operating mode, which allows the configuration of a wide range of different logic paths and facilitates failure identification, turns to be a very useful vehicle for library cell yield learning [13].

In this paper, we present the on-silicon validation of the test circuit proposed in [12]. A commercial 0.6 µm library was used as case study. The obtained results can be seen not only as the validation task of such a standard cell library test methodology, but also they are quite useful to improve the test circuit architecture and functionality.

The rest of the paper is organized as follows. In Section II, the circuit architecture and the library test methodology are briefly described, whereas more details are presented in [12]. In Section III, we describe the case study library, benchmark and test application tools. In Section IV, we show some measurement results of several tests applied to the test chip prototype. Finally, in Section V, we outline some conclusions.

II. Circuit Architecture and Proposed Operation

The circuit architecture is depicted in Fig. 1, where the combinational blocks are the key factor of the test circuit efficiency.

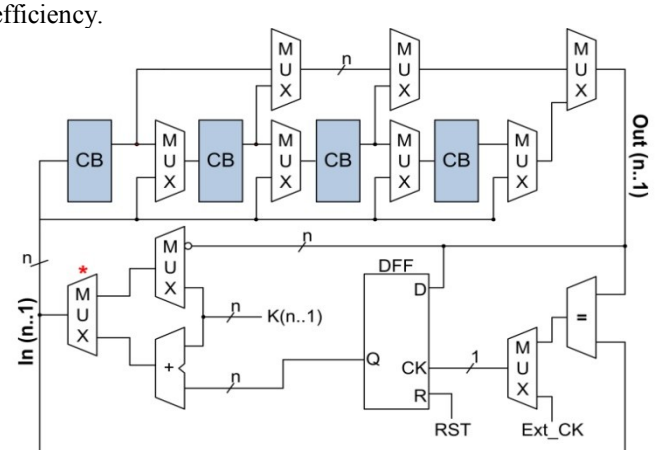


Figure 1. Block diagram of the test circuit.

They are built to guarantee the application of complete functional stimuli on the ensemble of logic gates to be verified. To achieve that, each block is composed of two stages, as illustrated in Fig. 2.

The first stage receives an input code ‘In’ and produces an intermediate code ‘W’. The second stage receives the intermediate code ‘W’ and produces the output code ‘Out’. The first stage is designed with a single logic depth topology where every instantiated cell ‘Ci’ is connected to (shared) primary inputs (the input code ‘In’) of the combinational block and generates one of the bits Wi of the intermediate code ‘W’.

The second stage receives the signals of the intermediate code (‘W’), provided by the cells at the first stage, and recreates the input code ‘In’ at the block outputs. It means that the output code ‘Out’ is equal to the input code ‘In’, *i.e.*,

In≡Out. The first stage produces the intermediate code Wi and the second stage recovers the input information from the intermediate code.

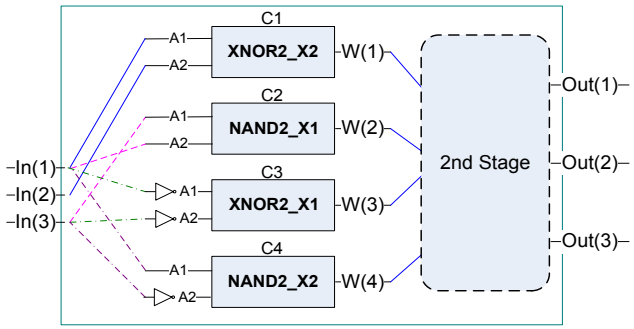


Figure 2.Example of a 3-bit combinational block.

Using such strategy, the full functional verification of the cells placed at the first stage is achieved by applying at the block inputs all possible input code combinations. Moreover, since the same input information is available at the block output code, easy verification of the correct logic behavior is attained by just comparing both input and output codes. Furthermore, this characteristic allows cascading the blocks to transmit the complete functional stimuli and taking advantage from the straightforward input-output verification feature. Long paths with higher delay are better for timing measurements.

The architecture depicted in Fig. 1 can be configured in four distinct operation modes to test sets of combinational blocks. To provide a sequence of test vectors with minimum external intervention, the signals at the end of the combinational block ('CB') chain are reconnected to the beginning of the chain in a ring configuration. The ring can be closed in different configurations with the help of multiplexers. Other optional elements include a register barrier and an adder block. The register barrier (D-type flip-flops – 'DFF') is introduced into the feedback path to avoid racing. The adder circuit is used to increment the binary vector, also making the circuit to modify the data in the ring and to play as a counter. The adder is able to perform 'modulo-K' increment enabling more than just modulo-1 counting. It allows for a wide range of different signal transitions which are important to check different charging and discharging conditions at intra- and inter-cell nodes. The basic architecture also includes a comparator ('=') and multiplexers ('MUX') to configure different operating modes and, consequently, different data evaluation conditions. The four distinct circuit operating modes are briefly described below.

A. Synchronous Mode

In the synchronous operating mode, the register barrier is controlled by an external clock signal. The adder is used to increment the vector in the ring, acting as a synchronous '+K' counter. The correct behavior of the counting sequence indicates the correct functionality of the combinational blocks and, consequently, the right functional behavior of the whole ensemble of cells being verified.

The maximum operating frequency of the circuit, which is associated to the worst case path delay, can be obtained by increasing the clock frequency until the ring counter is not able to complete the counting sequence. Such critical path delay can be different by changing the counting modulo 'K'.

Another benefit of the synchronous mode is the evaluation of the power dissipation, including the dynamic and static components. The external control of the clock signal imposes the operating frequency for switching and the associated amount dynamic power consumption. By varying the frequency, it is possible to verify the dynamic power consumption of the circuit, as the same transitions occur repeatedly. The static power, on the other hand, can be measured at DC condition or at very low frequencies. For each new input state in the circuit, the static consumption can be obtained since such power dissipation component depends strongly on the circuit steady state.

B. Asynchronous Mode

In the asynchronous mode, or self-timed ring configuration, the clock signal of the flip-flops is provided by the comparator that checks whether or not the input vector *In*(n..1) has already propagated to the end of the combinational block chain *Out*(n..1). When the same vector applied to the circuit inputs get to the end of the chain, the comparator switches from '0' to '1', clocking the register. The new data is stored in the register and passed to the adder. The adder increments the data and applies the new vector to the chain. At this moment, since *In*(n..1) no longer equals *Out*(n..1), the comparator output is back to '0' and remains at this state until the new vector propagates through the chain of combinational blocks. In addition, a normal comparator may produce spikes when its inputs are changing, which could be a problem when generating a clock signal for the circuit. To deal with this issue, a 3-input comparator was employed. Besides taking as inputs *In* and *Out*, an intermediate node in the chain was selected.

In this operating mode, just an external signal transition is enough to start the self-timed counting, and the right operation keeps the circuit running. If a cell is defective, the data at the end of the chain will no longer be equal to the data at the circuit inputs. This way, the comparator does not switch to '1' and the self-timed execution stops.

The self-checking property of the asynchronous mode makes it quite appropriate for functional cell verification with minimum external intervention. The correct logic operation can be checked by just monitoring the internal clock signal or only one data bit in the loop path.

Timing information can be extracted from complete '+K' counting cycles. This measure represents the average logic path delay since in a self-timed circuit the speed is as fast as possible according to the delay of each transition, or the time to finish a computation.

C. Single Bit Closed Loop Mode

The single bit closed loop mode is inspired in the digital oscillation BIST approach presented in [14] to allow the verification of time fault. The basic principle of the single bit closed loop mode is to cause the oscillation of a single bit in closed loop while the other bits remain in open loop. In the synchronous or asynchronous mode described in prior sections, the same binary value of an i-index input is expected to re-appear at the corresponding i-index output of the test circuit. This property is ensured by the construction of the combinational blocks. If the i_{th}-output is directly connected to the i_{th}-input, the i_{th}-path is kept in steady state, while closing the feedback loop. However, when the i_{th}-output is inverted before connecting to i_{th}-input, as indicated in Fig. 3, a negative polarity logic feedback occurs and the i_{th}-path oscillates. According to this principle, in the oscillation mode the feedback loop is closed such that at least one of the primary inputs of the chain receives the negation of its previous value.

Notice that, the logic path followed by the oscillating signal inside each combinational block depends on the binary values

of the side inputs provided in open loop. This feature allows configuring a wide range of different oscillating paths by choosing one bit at a time for the oscillation and by modifying the static values of the input bits in open loop.

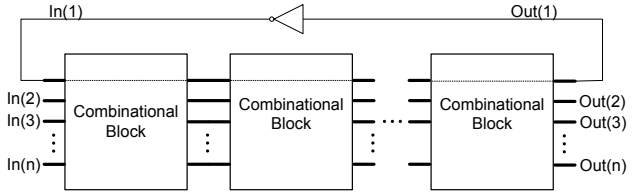


Figure 3.Oscillation BIST path illustration.

D. *Diagnosis or Functional Mode*

To perform defect diagnosis, multiplexers can be included in the circuit architecture at no significant area penalty, in order to select only part of the combinational block chain. Multiplexers at the inputs of each combinational block can select the signal from the previous block or directly from the beginning of the chain, removing the influence of the previous blocks in the ring loop. Similarly, multiplexers at the output of the blocks can send the data from the middle of the chain directly to the end of the chain. This way, the chain can be easily reduced to a single block or even none, allowing verify the counter and the register barrier without the influence of the combinational chain.

This mode provides the diagnosis of a faulty block, and it also allows the different circuit operating modes, described above, to run through part of the entire chain. The diagnosis can also be performed in open ring configuration, as the multiplexer used to provide the oscillation BIST mode can be also applied to interrupt the ring configuration without additional circuitry. The open chain mode allows the external control of the signal stimuli that are sent to the combinational blocks chain. This mode can be used to identify faulty blocks, and could be improved for the identification of faulty cells.

III. CASE STUDY

In order to evaluate the effectiveness of the benchmark generation methodology described in Section II, we use it to build a tangible design with some I/Os to allow measuring operating frequencies, power consumption and signal delay propagation. Power consumption is determined by measuring the voltage on a shunt resistor of 100 Ω inserted in series between the external power supply and VDD pin. The following paragraphs give more details in terms of the chosen cell library, the generated benchmark, the manufacturing foundry and packaging, and the adopted test methods and tools.

A. *Cell Library*

The benchmark was manufactured in a commercial 0.6µm CMOS technology using the standard cell library provided by XFAB. Both the target process and cell library are mature enough to guarantee the correct functionality of the set of cells, so allowing the effective validation of the benchmark and, consequently, the methodology used to create it. The library is composed of 403 combinational cells and 99 sequential cells.

B. *The Generated Benchmark*

The circuit generation method exploits a tool capable of automatically assembling the benchmark together [12]. The tool used the abovementioned described library to generate our benchmark case study comprising 20 combinational blocks (CB). Each CB is composed of a number of cell instances, as shown in Table I.

Table I. Cell instantiation per combinational block.

CB	Distinct cells in the First Stage	Cells in the Second Stage
0	19	157
1	18	172
2	51	279
3	16	141
4	23	193
5	31	184
6	31	205
7	23	199
8	20	174
9	35	235
10	16	117
11	19	128
12	14	44
13	8	8
14	14	26
15	19	56
16	15	43
17	11	55
18	11	44
19	9	26
Total	**403**	**2486**

Moreover, the benchmark has a total of 3,688 cell instances: 2,889 cells distributed over the CBs and 799 cells implementing the control logic composed of several multiplexers, a 6-bit register, a 6-bit adder, 6-bit *In* port and 6-bit *Out* port.

C. *Manufacturing and Packaging*

The test chip including the generated benchmark was manufactured in a 0.6µm CMOS process at the XFAB facilities in Germany. In total, 61 dice were manufactured and sent to CEITEC S.A., in Brazil, where they were packaged into two packaging types, as shown in Fig. 4.

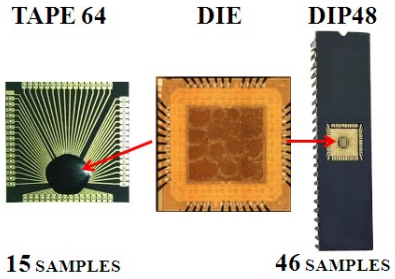


Figure 4. Test chip packaged samples.

D. *Testers and Workbenches*

The design was built without any internal micro pads, which are usually needed to evaluate specific internal logic by using a probe station. However, the benchmark test modes may configure the circuit to route observability points to the output without actually needing expensive equipment to evaluate the circuit.

Two workbenches were developed to test and evaluate the 61 samples. The first (functional workbench) includes an FPGA-based test equipment capable of applying structural tests to screen bad samples from good ones. A DE0 Terasic board including a Cyclone III FPGA from Altera was used to implement this test equipment.

The second workbench (characterization workbench) included some laboratory equipments like a 250MHz Agilent oscilloscope, voltmeter, a daughter board socket to properly connect the testing samples pins to the tester, and some switches to correctly configure the circuit in its several test modes, as described in Section II. This workbench was used

for executing characterization tests: measuring operating electrical and timing information of a good sample. Also, a 16903A Agilent logic analyzer has been used to catch propagation delay.

IV. Circuit Evaluation and Measurements

The benchmark generation methodology was validated by analyzing results of the on-silicon validation tests applied to the generated benchmark. Several validation tests were conducted to determine whether the circuit works accordingly to its functionality and specifications. The following discuss the results according to the circuit operation mode, as described in Section II.

A. Functional mode validation

In this mode, structural tests (manufacturing tests) targeting stuck-at faults can be applied to the samples. Usually, design-for-testability (DfT) structures are inserted in VLSI designs to aid on test pattern generation and application. However, one of the benchmark generation methodology goals is to build a combinational circuit with exactly one register barrier (*i.e.*, comprising six D-type FFs) to allow evaluating its combinational cells. Thus, inserting scan chains do not increase the fault coverage, neither simplifies the test application. Nonetheless, the benchmark has other test modes that make the circuit function as a BIST-like structure for testing the CBs.

In order to test each CB individually, an exhaustive test pattern was applied to the 61 samples. Although it is not a common strategy for large VLSI designs because it may increase test time and data volume, this approach was selected once the benchmark is a relatively small circuit. For instance, the total number of applied patterns was only 1,408. They were capable of detecting 80% of the total stuck-at faults. This number can be improved by routing some intra-CB signals to observable output pins. Moreover, the residual uncovered faults are known to be untestable, but also redundant, *i.e.*, their insurgence does not modify the circuit functions. Despite the low coverage obtained for the whole circuit, these patterns were able to cover 100% of the target cells, meaning that at least one instance of each distinct cell in the library could be controlled and evaluated.

Manufacturing tests were conducted by setting up the functional workbench operating the samples in functional mode applying the exhaustive test pattern. Initially, the control logic (adder, FFs and multiplexers) were tested. Then, each CB was solely tested, and finally all CBs together with the controlling logic. Fig. 5 shows the chain *In* and *Out* values being captured by the logic analyzer, demonstrating that the connected CBs are working correctly in functional mode.

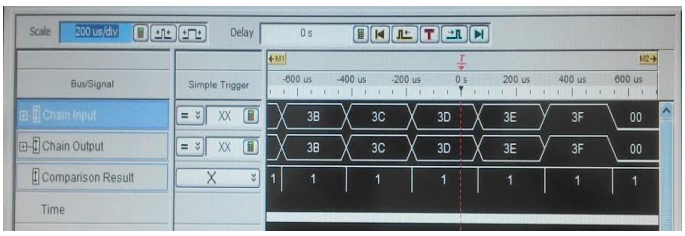
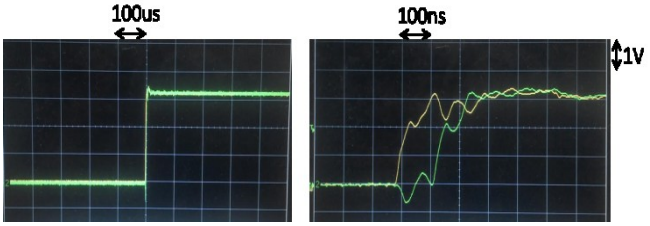


Figure 5: In and Out values captured by the logic analyzer.

Fig. 6 shows the propagation delay of the least significant bit (LSB) when switching from $3E_{hex}$ to $3F_{hex}$ values. The image in Fig. 6(a) is the perception of an instant change of *In* (in yellow) and *Out* (in green), whereas in Fig. 6(b) shows a time amplification of the same bit to evaluate its propagation delay. The voltage scale on both images is 1 Volt/div and the time scales in Fig. 6(a) and Fig. 6(b) are, respectively, 100 µs/div and 100 ns/div. Notice that the LSB propagation delay when testing all CBs is around 140ns.



(a) (b)

Figure 6: (a) In-out delay perception (b) In-out actual delay

The stimuli starting from 00_{hex} and ending in $3F_{hex}$ were applied to *In* inputs and observed at the *Out* signal outputs. Notice that functional mode operates without a clock, and its only job is to pass the applied input stimuli through the CBs to finally reach the output, as observed in Fig. 5 and in Fig. 6.

After testing all devices in functional mode, we determined that 14 out of 61 samples worked perfectly without any error, 34 samples presented less than 3 small errors, and the remaining 13 samples had severe errors, due to some kind of defect that could be observed on a microscope (burnt logic, misplaced contact, scratches, etc.). We verified that the insurgence of these defects was clearly caused by human error during packaging, transportation, handling, and misusage.

B. Synchronous mode validation

Initially, we validated this mode by configuring the circuit according to the explanation in Section II. We observed that the up-counter increments by one every time the external clock is pulsed. Also, the counter automatically goes to zero when an overflow occurs, *i.e.*, when adding 1_{dec} to 63_{dec} on a 6-bit adder, showing that the mode actually works.

This mode is useful for executing two types of characterization tests:

- maximum operating frequencies
- lowest working power supply value (VDD).

In the first test, we measured the maximum frequencies and power consumption not only at 3.3 V nominal power supply, but also at 2.2 V and 1.1 V. Initially, we set the VDD level, then slowly increased the clock frequency (starting from 10 Hz) until the *Out* signal started to misbehave or miscompute, and finally we measured the frequency and power consumption. We are able to detect miscomputation when some counting is missed out by the logic gates due to the high clock frequency, which can be visually identified on the logic analyzer screen.

Besides discovering the maximum operating frequency of the circuit, we also determined the maximum power consumption of each CB, distinguishing static and dynamic dissipations. Fig. 7 and Fig. 8 show, respectively, maximum operating frequencies and power consumptions of every CB at different VDD levels.

The measured results show that CB 19 is the fastest and also the most power hungry, mainly because it is also one of the smallest CBs, accounting on just 35 combinational cells. Conversely, CB 2 is the largest circuit containing 330 cells and also the slowest, as shown in the graphs. The maximum frequency when all CBs are tested together is around 7 MHz and consumes 25 mW of power, which means around 3.6nW/Hz. Finally, we verified that as VDD scales down from

one level to another, the maximum frequency and power consumption reduce, respectively, by half and about 5 times.

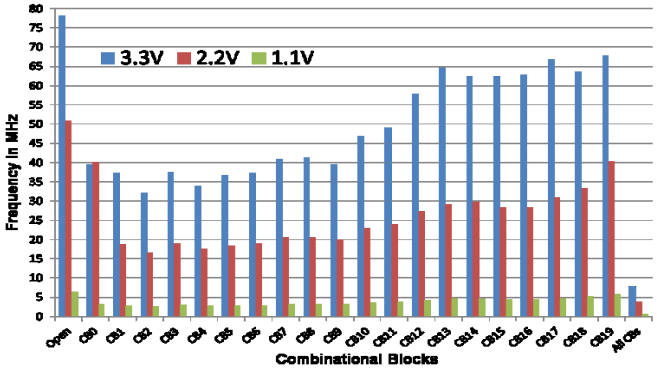


Figure 7: Frequency of each CB in synchronous mode.

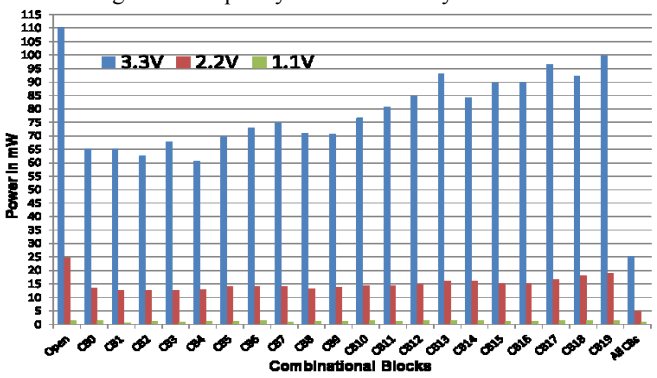


Figure 8: Power consumption of each CB in synchronous mode.

The second test in synchronous mode allowed measuring the lowest working VDD. To understand how to determine initial voltage levels, we looked at the circuit physical synthesis constraints and manufacturing technology limits VDD levels. In synthesis, a 0.9 V minimum VDD was constrained by designers, and the synthesis and simulation tools guaranteed that the circuit would function correctly.

On the other hand, the technology limit defines the lowest working voltage as 0.75 V, also known as threshold voltage. By analyzing these limits, we have decided to evaluate the circuit under three VDD levels: the lowest (~0.75 V), synthesis constrained (0.9 V) and an intermediate value (0.8 V).

We carried out the second test by initially setting VDD to 0V and clock frequency to 1Hz. Then, we slowly increased VDD until the correct counting behavior was observed at the *Out* signal. Indeed, we observed that the lowest working VDD varied from 0.74 V to 0.76 V. At this point, we also increased the clock speed until the circuit stopped functioning again. Finally, we measured frequency and power consumption. This experiment was then repeated for 0.8 V and 0.9 V for every CB.

As the circuit operates near threshold voltages, leakage power and measurement difficulties started influencing on final power consumption values, diversely from the first test in synchronous mode. This assumption derived from the information seen in graphs in Fig. 9 and Fig. 10, where the power consumption difference was constant between the three VDD levels. Also, they have shown be uncorrelated with the switching activity factor and their corresponding frequencies that operate in the order of KHz.

Although results in Fig. 7 and Fig. 8 show a certain irregularity when comparing frequency and power measurements to Fig. 9 and Fig. 10, the circuit was able to function correctly according to the specifications presented in [12].

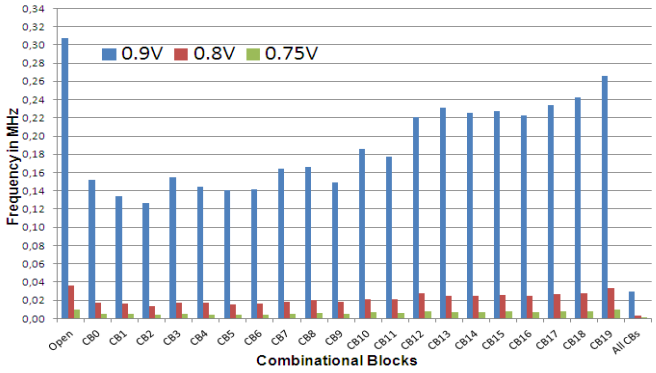


Figure 9: Frequency of each CB in Synchronous mode.

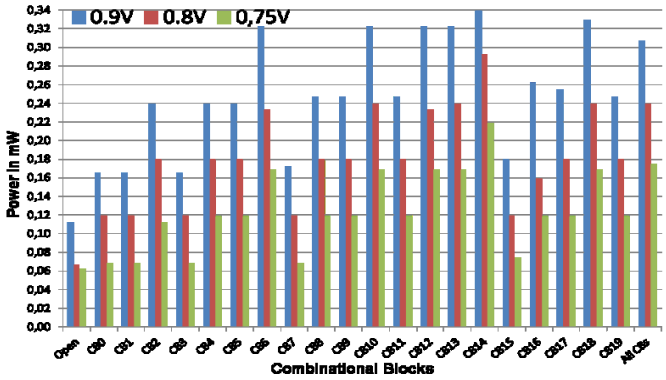


Figure 10: Power consumption of each CB inSynchronous mode.

C. *Asynchronous mode validation*

The asynchronous mode configures the benchmark in an up-counter whose outputs stimulate the target CB. This mode was sought to easily detect defective CBs without needing external clocks and/or specific test equipments.

The main advantage of this mode lies in its self-test ability, because it is capable of providing an internal clock that is generated from an embedded comparator (see Section II for details). Notice that the way the internal clock is generated also produces a jitter,due to the different path the stimuli take inside each CB every time its input changes.

We measured the generated internal clock frequency for all CBs and they ranged from 5MHz (all CBs) to 61 MHz (CB19). The open chain created a 65 MHz clock. Besides measuring the internal clock maximum frequency in this mode, we also determined the propagation delay from *In* to *Out* of the chain.

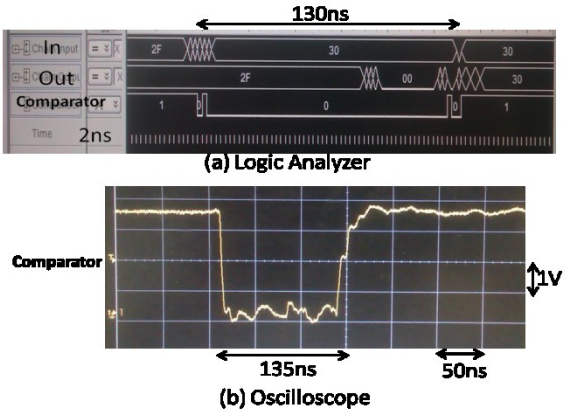


Figure 11. Maximum propagation delay of the comparator

Fig. 11 shows the comparison propagation delay measurements when all CBs are connected to chain. At the top image (Fig. 11a), the logic analyzer measurement shows the

comparator maximum functional delay when *In* is changing from 011111_{bin} to 100000_{bin}. This particular test pattern was selected because all *In* and *Out* bits differ (*i.e,* the Hamming distance is 6) to forcefully stress the comparator logical computation and verify that output glitches would not appear to produce a wrong clock signal. The bottom image (Fig. 11b) shows the actual electrical measurement acquired by the oscilloscope. Notice that there is a small time difference between both results due to the logic analyzer resolution.

D. *Single Bit Closed Loop Mode validation*

In this last mode, we evaluated whether a selected input bit oscillated through the entire circuit passing through the chain including all CBs. Results showed that the maximum oscillation frequency was 110 MHz in open chain, 75 MHz (CB19), and around 5.4 MHz when all the CBs were connected to the chain. However, more interesting than measuring the oscillating frequency, we evaluated the path delay of a signal going from 0 to 1, and vice-versa. In order to do this, we selected the LSB bit to oscillate in a ring oscillation configuration that this test mode provides. Then, we used the logic analyzer to catch the specific delays from the rising and falling transitions. Fig. 12 shows 3 images of the same time frame. Fig. 12(a) shows the continuous ring oscillation of the desired bit, demonstrating that the closed-loop oscillation mode functions correctly. Also, we observed that the path delay of a rising transition signal from *In* to *Out* passing through all CBs is 80 ns, whereas for the falling transition signal is 100 ns.

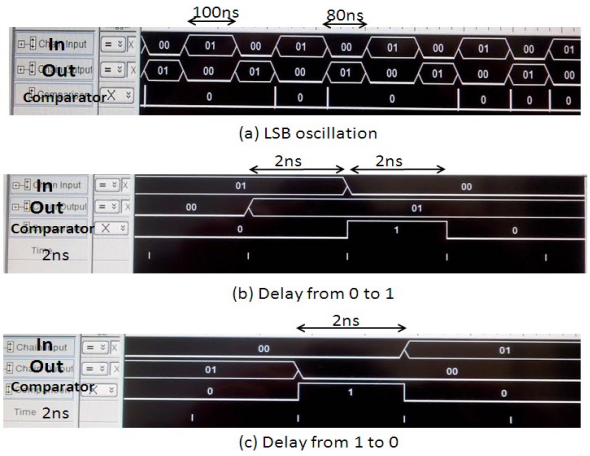


Figure 12. Closed-loop oscillation mode timing evaluation.

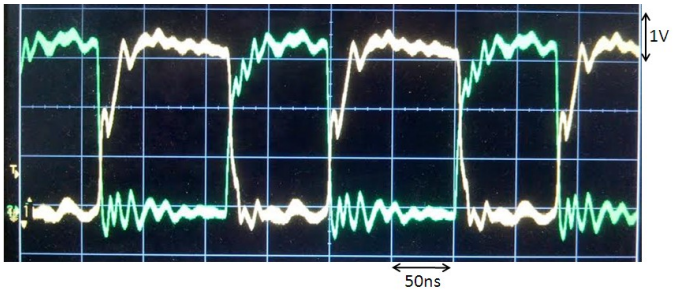


Figure 13. Closed-loop oscillation mode electrical evaluation.

The image in Fig. 12(b) illustrates the path delay of a rising transition, showing that it takes 2ns to propagate the edge from *Out* to *In*. In addition, as a collateral result, we detected that there is also a 2 ns response delay (*i.e.,* shifted 2ns in time) in the comparator. Sometimes, the comparator cannot cope with the speed that misses out some comparisons. The falling transition path delay depicted in Fig. 12(c) is also 2 ns whereas, in this case, the comparator was able to reply promptly without the 2ns delay.

We also analyzed this mode in the oscilloscope to determine some electrical characteristics. Fig.13 shows the oscilloscope screen showing the LSB of the *In* value (in yellow) and the *Out* value (in green). Notice that in Fig. 13, the time scale is 50ns per horizontal division and the voltage scale is 1V per vertical division. These results also corroborate with the ones shown in Fig. 12. Both provide scientific experimental evidence that the closed-loop oscillation BIST mode works properly according to the desired specifications described in section II.

V. CONCLUSIONS

In this work, we validated the effectiveness of the benchmark generation for cell library design evaluation. This goal was achieved by applying validation tests on a 0.6µm technology test chip and measuring electrical and timing information. Since the benchmark is supposed to help on-silicon evaluation of a cell library, it was fundamental to manufacture an IC to verify whether the method works or not. In order to test the chip, we used the functional mode to apply manufacturing test patterns on 61 samples to screen good chips from bad ones. Then we used a good sample operating in the other modes to evaluate its functional, electrical, and timing characteristics. The gathered results presented in this paper show that all functions of the benchmark were functioning correctly, thus validating its generation methodology. In addition, we were able to evaluate each CB and their design, by determining their power consumption and frequency under different power supply levels. As future works, we propose adding to the benchmark more observability points to increase fault coverage as well as some fault injection mechanisms to evaluate the circuit in the presence of faults.

REFERENCES

[1] P. de Dood, B. Lee and D. Albers. “Optimization of circuit designs using a continuous spectrum of library cells”. US Patent 7107551. 2003.

[2] S. Gavrilov, A. Glebov, S. Pullela, S.C. Moore, A. Dharchoudhury, R. Panda, G. Vijayan and D. T. Blaauw, “Library-less synthesis for static CMOS combinational logic circuits,” ICCAD 1997, pp.658-662.

[3] F. S. Marques, L. S. Rosa Jr, R. P. Ribas, S. S. Sapatnekar and A. I. Reis. “DAG based library-free technology mapping,” GLSVLSI 2007, pp.293-298.

[5] R. Roy, D. Bhattacharya and V. Boppana. “Transistor-level optimization of digital designs with flex cells,” IEEE Computer, Feb. 2005, vol. 38, no. 2, pp. 53- 61.

[6] Ricci, A., De Munari, I. and Ciampolini, P. “An evolutionary approach for standard-cell library reduction,” GLSVLSI 2007, pp.305-310.

[7] R.-B. Lin, I. S.-H.Chou and C.-M. Tsai, “Benchmark circuits improve the quality of a standard cell library,” Asia and South Pacific Design Automation Conference (ASP-DAC), 1999, pp.173.

[8] W. D. Heavlin, “System and method for designing, fabricating and testing multiple cell test structures to validate a cell library,” US Patent 5724251, 1998.

[9] W. Agatstein, K. McFaul and P. Themins, “Validating an ASIC standard cell library,” Third Annual IEEE ASIC Seminar and Exhibit, Sep. 1990.

[10] N. Salgunan, “Library test circuit and library test method,” US Patent 0157141, 2007.

[11] K. S. Kim, S. Mitra and P. G. Ryan, “Delay defect characteristics and testing strategies,” IEEE Design & Test of Computers, Sep.-Oct. 2003, pp.8-16.

[12] R. P. Ribas, S. Bavaresco, N. Schuch, V. Callegaro, M. Lubaszewski and A. I. Reis, “Contributions to the evaluation of ensembles of combinational logic gates,” Microelectronics Journal, vol. 42, 2011, p.371-381.

[13] M. Keim, N. Tamarapalli, H. Tang, M. Sharma, Rajski, C. Schuermyer and B. Benware, “A rapid yield learning flow based on production integrated layout-aware diagnosis,” IEEE International Test Conference (ITC), 2006, paper 7.1.

[14] K. S. Kim, S. Mitra and P. G. Ryan, “Delay defect characteristics and testing strategies,” IEEE Design & Test of Computers, Sep.-Oct. 2003, pp.8-16.