Mauricio De Carvalho, PhD.

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Projects: **https://github.com/mauriciomc**

OBJECTIVE

ASIC/FPGA design and verification engineer

TECHNICAL SKILLS:

Experience in SoC design verification and post-silicon validation
Strong knowledge of Computer Architecture and Digital Systems
Experience with Standard Cell ASIC design flow (3 tapeouts)
RTL design of CPUs, Hardware Arithmetic, and peripherals
Good knowledge of Verilog, SystemVerilog and VHDL
Experience with Commercial EDA tools: Cadence, Synopsys and Mentor
Experience with Open source EDA tools: Verilator, QFlow, Electric VLSI and Magic VLSI
Experience with FPGA prototyping: Xilinx and Altera
FPGA tools experience: Xilinx ISE, Xilinx Vivado and Altera Quartus II
Soft/Hardcore experience: Zynq, MicroBlaze/PicoBlaze and Nios II
Embedded systems design: NRF, LPC, IMX28, IMX6, Zynq; Microchip, 8051, HC11,
Programming skills in C/C++, Java, Assembly, bash, TCL, Python
Expert user of Linux (Ubuntu, Rhel, Fedora) and Embedded Linux Yocto
Experience with Lab equipments: Oscilloscope (Analog and Digital), logic analyzer, voltmeter.
PCB layout: Kicad, Eagle, DesignSpark
Version control: SVN, GIT and DesignSync

PERSONAL SKILLS

Quick-learner, hard-working, problem solver, self-motivated, patient, concentrated and friendly.

EXPERIENCE

FPGA Hardware and Software Engineer **CellXica**, Cambridge, UK *Sep. 2018 - Mar 2019*

- Electronic engineer contractor working on base station LTE platform
- Vivado-FPGA Zynq ARM and verilog dev.; Embedded C++ applications; Driver development;

Principal Engineer (Embedded Systems) **IEVO ltd**, Newcastle, UK *Dec. 2016 - Aug. 2018*

- Team lead of a small group of Engineers
- ARM Embedded C/C++ Programming to fix the main product bugs
- Extensive System Debug with GDB-Eclipse and Redmine to track issues and meet deadlines
- Improved overall biometric system performance by 25%
- Hardware debug and improvements reducing product costs
- PCB development using Kicad to release three IMX6-based products
- PCB product follow-up from design to validation and production
- Hardware validation using Oscilloscope, Multimeter and logic analyzer
- Embedded Linux Kernel compilation (Yocto, bitbake)
- Responsible for coordinating projects together with Operations Manager.

Mixed-signal verification engineer (Contractor) **AMS**, Graz, Austria *July 2016 - December 2016*

- Coded in SV analog models to speed-up simulations and verification of ASICs
- Coded in SV verification test cases
- Helped build-up the Mixed-signal simulation environment
- Responsible for synchronizing contractors with mixed skill-sets to speed-up verification.

ASIC Design and Design-for-Test Engineer **NSCAD/CEITEC**, Brazil *August 2014 - May 2016*

- Developed an FPGA-based (Cyclone IV) tester for test automation of digital ICs
- Validated on silicon the CEITEC's first industrial cell library in 0.6 um
- Developed from scratch a small CPU including Memory IPs (RTL-Verif-Synth-Layout)
- Developed hierarchical DFT Synthesis strategy for an ARM0-based Satellite SoC
- Post-silicon validation of several benchmarks
- Test pattern generation for achieving high fault coverage
- Characterization tests on 60 samples
- Test strategy and plan development
- Developed a PONG game using Cyclone IV Terasic DE0 board for teaching students
- Instructed DFT and Test for more than 125 IC Engineers at **IC-Brazil program** on a 40-hour course.

Research Assistant **Politecnico di Torino**, Turin, Italy *March 2010 - Dec 2010*

- SBST pattern generation for Automotive SoCs on-line testing to comply with the ISO26262 standard. Collaboration work with STMicroelectronics for Bosh and Audi applications
- Accurate failure analysis of embedded memories in automotive SoCs. This worked involved developing a java tool capable of manipulating data and determining where faults occurred, improving the fabrication process. Collaboration work with STMicroelectronics and NplusT companies.
- Design circuit for emulating on-line testing of the above mentioned SoC.

R&D Consultant **Eltra srl**, Turin, Italy *Feb 2008 - Sep 2008*

- Embedded systems development for parking ticket dispenser machines.
- Electronic Schematics and PCB Layout design using Eagle.
- Firmware development in assembly for HC11 microcontroller.
- Self-test mechanisms for product quality and reliability.

C++ Software Developer **VFR Sistemas**, Porto Alegre, Brazil *Aug 2006 - Aug 2007*

- Interface and driver development for medical equipment
- QT C/C++ Development of a hospital management software
- Software verification and validation of older versions offering reliability to clients
- Schematics and PCB layout of interface systems between computer and medical equipment.

R&D Consultant **Stark Transformers**, RS, Brazil *Nov 2004 - Jul 2005*

- Digital controller development for Uninterrupted Power Supplies (UPS)
- Embedded system development with PIC16F877
- PCB Layout using Eagle and Tango
- Product verification and validation on new products

EDUCATION

Politecnico di Torino Turin, Italy *Jan. 2011 - Feb. 2015*
PhD. in Computer Engineering at **CAD and Reliability Group**
Doctoral Thesis: **Innovative Techniques for Testing and Diagnosing SoCs**
Collaboration: STMicroelectronics - Bosch - Audi, **NPlusT**, **LIRMM** and **UFRGS**

Politecnico di Torino Turin, Italy *Sep. 2007 - Feb. 2010*
M.Sc. in Computer Engineering: Hardware design track
Thesis: Automatic Generation of Functional Stress Patterns for SoC Reliability Characterization
Final Vote: **104/110**

State University of Rio Grande do Sul Porto Alegre, Brazil *Jan. 2004 - Aug. 2007*
B.Sc. in Digital Systems Engineering: Hardware design track

Fundacao Escola Tecnica Liberato Salzano Novo Hamburgo, Brazil *Jan. 1999 - Dec. 2003*
Technological degree in electronics

LANGUAGES

Portuguese	Mother tongue
English	Fluent (IELTS:7/9 + 7 years living in UK)
Italian	Fluent (6.5 years living in Turin, Italy)
French	Intermediate (6 months living in Montpellier, France)

PERSONAL PROJECTS

Open source RISCV-based SoC development with open source tools (Verilator, Yosis, Electric VLSI)
Open source PDK development for Brazilian Foundry 0.6um technology
NRF51822 IoT device + Android and IPhone APP development (Commercial product).

OTHER QUALIFICATIONS

11 IEEE Conference Papers and 2 Journals on testing
SoC 93K Verigy 40-hour qualification for Digital Test in 2012 at **LIRMM**
Microelectronics course EMICRO at **Federal University of Rio Grande Do Sul** 04/2006
Texas instruments DSC training 09/2006
Freescale training 03/2007
Texas instruments MSP430 training 5/2007.

Note: Publication list and reference letters upon request.