COSC 4310 Computer Architecture Instructor: Prof. JIANGJIANG (JANE) LIU Project

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CPU	Clock Rates	Enabled (core chip thread/core)	# of cache lvls	# of cache in l1	# of Cache In l2	# of Cache In l3	Cache size	Memory size	Storage
AMD Ryzen 9 7950X	5700	16 cores, 1 chip, 2 threads/core	3	2	1	1	32 KB I + 32 KB D on chip per core 1 MB I+D on chip per core 64 MB I+D on chip per chip, 32 MB shared / 8 cores	64 GB (2 x 32 GB 2Rx4 PC5-5600B-R , running at 5200)	500 GB NVMe M.2
Intel Xeon Gold 6454S	3400	64 cores, 2 chips, 2 threads/core	3	2	1	1	32 KB I + 48 KB D on chip per core 2 MB I+D on chip per core 60 MB I+D on chip per chip	1 TB (16 x 64 GB 2Rx4 PC5-4800B-R)	1 x 1.6 TB PCIe NVMe SSD
Intel Xeon Platinum 8454H	3400	64 cores, 2 chips, 2 threads/core	3	2	1	1	32 KB I + 48 KB D on chip per core 2 MB I+D on chip per core 82.5 MB I+D on chip per chip	1 TB (16 x 64 GB 2Rx4 PC5-4800B-R)	1 x 960 GB M.2 SSD SATA

Cache configurations of CPUs play an important part in high-performance computing. I chose 3 CPUs to demonstrate cache. The AMD Ryzen 9 7950X, Intel Xeon Gold 6454S, and Intel Xeon Platinum 8454H are three CPUs in this context. With a clock speed of 5700 MHz and 16 cores, the AMD Ryzen 9 7950X stands out for its potential in single-threaded programs and gaming. This processor's cores each include 32 KB Instruction and 32 KB Data caches in L1, as well as a 1 MB combined Instruction and Data cache in L2. Cache L3 has 64 MB shared across the chip and 32 MB dynamically allocated over 8 cores to improve speed in large datasets.

Both Intel Xeon Gold 6454S and Platinum 8454H are designed for server and enterprise environments, with a greater core count which is 64 cores and memory capacity. Both CPUs have a similar L1 and L2 cache architecture, with 32 KB Instruction and 48 KB Data caches per core in L1 and a 2 MB combined cache in L2. Their L3 cache configurations, however, differ: the Gold 6454S has a 60 MB shared cache, but the Platinum 8454H has a slightly bigger 82.5 MB, making it more capable of handling multi-threaded workloads and massive data sets.

A comparison of these CPUs, puts an emphasis on cache miss rates, would provide information on their performance efficiency. The Ryzen 9 7950X is expected to provide lower miss rates in single-threaded operations due to its high clock rate, but it may struggle in multi-threaded workloads due to a smaller cache per core than the Xeon versions. The Xeons are designed to perform in scenarios that require robust multitasking and frequent access to shared data due to their bigger L3 caches. This analysis shows the need of specialized processor design to meet the needs of modern computer applications, that can range from gaming and personal use to more complex solutions.

Testing Results from program:

The cache implementation program begins with a basic interface that makes the users enter block addresses. Users are presented with an option, that allows them to select settings depending on the stated set associativity. Following that, the program used techniques to compute and show the final cache results in an orderly way. This interactive method fits to the project's criteria, allowing the user to interact with many set associativity options and finally delivering information into cache performance based on the block addresses.

Four way- 8 cache..

```
How many blocks are there in the cache?: 8
which set associativity?:
0: Fully associative cache
1= Direct-mapped cache
2= 2-way Set associative cache
3= Four-Way
:3
select one of these two options:
1 == Yes
0 == No
Use the LRU rule.
Enter the address... 3 4 0 0 6
[3, empty, empty]
[empty, empty, empty]
Miss
[0, empty, empty]
[empty, empty, empty]
Miss
Final state...
[0, empty, empty]
[empty, empty, empty]


...Program finished with exit code 0
Press ENTER to exit console.
```

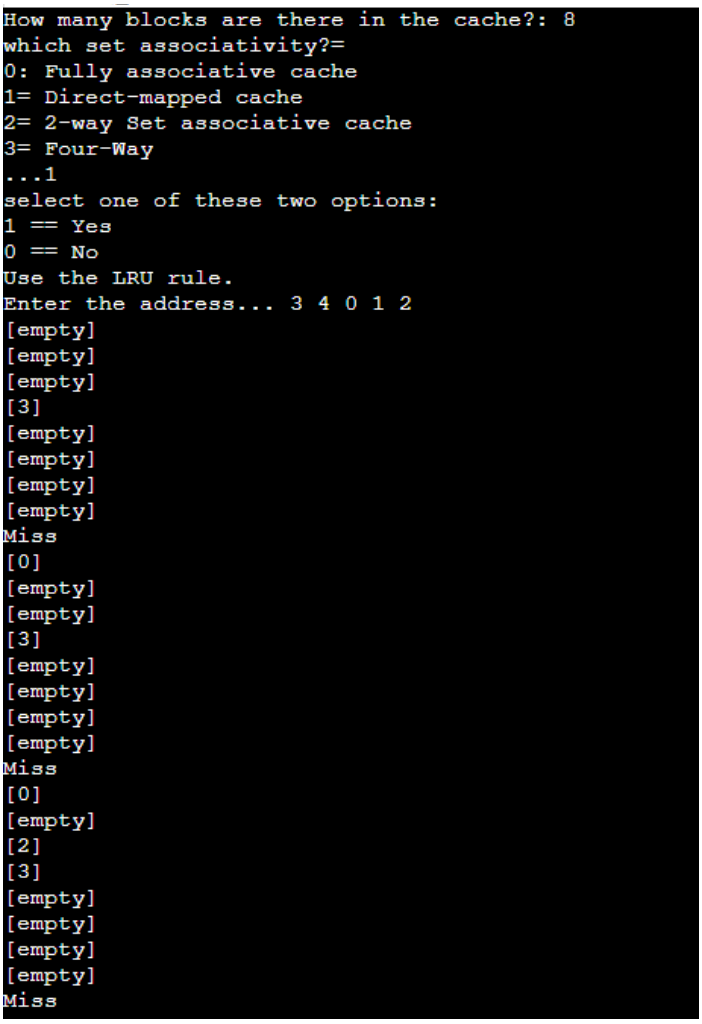
2-way:

```
How many blocks are there in the cache?: 8
which set associativity?:
0: Fully associative cache
1= Direct-mapped cache
2= 2-way Set associative cache
3= Four-Way
:2
select one of these two options:
1 == Yes
0 == No
Use the LRU rule.
Enter the address... 5 6 3 5 2
[empty, empty]
[5, empty]
[empty, empty]
[empty, empty]
Miss
[empty, empty]
[3, empty]
[empty, empty]
[empty, empty]
Miss
[2, empty]
[3, empty]
[empty, empty]
[empty, empty]
Miss
```

Fully associative cache :

```
How many blocks are there in the cache?: 8
which set associativity?=
0: Fully associative cache
1= Direct-mapped cache
2= 2-way Set associative cache
3= Four-Way
...0
select one of these two options:
1 == Yes
0 == No
Use the LRU rule.
Enter the address... 5 4 3 5 1
[5, empty, empty, empty, empty, empty, empty, empty]
Miss
[3, empty, empty, empty, empty, empty, empty, empty]
Miss
[1, empty, empty, empty, empty, empty, empty, empty]
Miss
```

Direct mapped cache:



In conclusion, the AMD Ryzen 9 7950X, Intel Xeon Gold 6454S, and Intel Xeon Platinum 8454H represent distinct design approaches in the field of high-performance computing. The Ryzen excels in single-threaded applications like gaming, whereas the Xeons, with higher core counts and larger caches, excel at multi-threaded workloads in enterprise settings. This emphasizes the significance of specialized processor design, highlighting that the best decision is dependent on the specific requirements of applications ranging from gaming to complicated corporate solutions.