Version	Date/ Datum	Initiated by/ Veranlasser	Reason of modification / Grund der Änderung item, section / Position, Absatz
01	2006-04-27	Ghani Wee, Fakhariah (OPD - Oled FE Prod. Dev.)	New Specification

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Applicable Area - Scope / Gültigkeitsbereich	
Corporation:	OSRAM Opto Semiconductors
Location:	Penang
Cluster:	OLED
Unit:	Module
SubUnit:	Calgary
Process:	

Function / Funktion	Name & Dienststelle (in Druckschrift) Name & Department (printed letters)	Date / Datum	Signature / Unterschrift
Author/Change-Author	Ghani Wee, Fakhariah (OPD - Oled FE Prod. Dev.)	2006-04-27	sgd. per Livelink Workflow
Document Control	Lee, Lin-Yong (QAD - Quality Assurance Department); Bt Yusof, Noorrida (QAD - Quality Assurance Department)	2006-05-30; 2006-05-29	sgd. per Livelink Workflow
Head Of Org Unit	Lacey, David (OLM - OLED Mfg Support)	2006-05-29	sgd. per Livelink Workflow
Internal Customer	Felder, Alfred (OS OLED Management)	2006-05-23	sgd. per Livelink Workflow
Order Fulfillment (OF)	Teo, Wei-Wei (OLM - OLED Mfg Support)	2006-05-03	sgd. per Livelink Workflow
Process Development	Lui, MW (OLED Product Development)	2006-05-04	sgd. per Livelink Workflow
Process Engineering	Lim, Kheng-Siang (OLN - OLED Engineering)	2006-05-04	sgd. per Livelink Workflow
Product Development	Bin Abdul Manaf, Shahrol-Izzanni (OMN - OLED BE Module Engrg)	2006-05-04	sgd. per Livelink Workflow
Product Engineering	Tan, Hong-Kiet (OLM - OLED Mfg Support)	2006-05-08	sgd. per Livelink Workflow
Production QM/QE	Lim, Lim-Ling (QRE - Reliability Engineering)	2006-05-03	sgd. per Livelink Workflow

Revision Log

Rev.	Description	Orig. By	ECN # / Date
A	New Spec	Fakhariah	
B	Update Power up and Power down Sequence Update Recommended DC Operating Conditions table Add in new luminance of 50cd/m^2 at 12V datas for Power Consumption, Initialization Code and Initial Luminance Upadate Sample Initialization Code table Update maximum luminance in Color Coordinates and Initial Luminance table Update QUALIFICATION TESTS and COSMETIC CRITERIA table Update GENERAL OLED MODULE HANDLING & CARE	Fakhariah	

CONTENT Page

1. TITLE

1.1. Product Specification for Pictiva™ 128 X 64 OLED Module, SSD0323, Calgary 4-bits H55XX OS128064PK27MX0BX0

2. PURPOSE

2.1. This product specification is specifically for OLED Calgary Module H55XX

3. SCOPE

3.1. This product specification is specifically for OLED Calgary Module H55XX

4. REFERENCE DOCUMENTS

4.1. Module Product Drawing Document Number

C63062- H5500- A001-*	Calgary OLED Module with Bezel (H55X0)
C63062- H5500- A002-*	Calgary OLED Module without Bezel (H55X3)
C63062- H5500- A003-*	Calgary OLED Module with Bezel Type2 (H55X1)

4.2. Solomon Systech SSD0323 128X80, Dot Matrix OLED/PLED Segment/Common Driver with Controller

5. OTHER REQUIREMENTS

5.1. FEATURES, FUNCTIONS, and REQUIREMENTS

5.1.1. Product Summary

General OLED Module Description

Display Format	128 columns x 64 rows
Pixel Pitch	0.48 (W) x 0.48 (H) mm
Pixel Size	0.45 (W) x 0.45 (H) mm
Display Diagonal	2.7”
Color	Elegance Yellow; Spring Green
Grayscale	4 bit
Active Area	61.41 (W) X 30.69 (H) mm
Viewing Area	63.41 (W) X 32.69 (H) mm
Module Size	Varies. See next table.
Glass Size	74.00 (W) X 41.86 (H) X 2.20 (T) mm (including polarizer)
Driver IC	SSD0323 (SSD0323 on SSD1325T6R1 TAB)
Interface	4-wire Serial or 8-bit Parallel, User Configurable
Packaging and Interconnect	ZIF
OLED Power Supply	Dual voltage supplies

5.1.2. Part Number

Part Number Description

OS128064PK27MXXXXX	Q Number	Color	Bezel	Module Size, mm	Factory Code
XXXXX = Y0B00	Q65110A4433	Elegance Yellow	Metal	Refer to Product Drawing	H5550[1]
XXXXX = G0B00	Q65110A4434	Spring Green	Metal	Refer to Product Drawing	H5560[1]
XXXXX = Y0B10	Q65110A5416	Elegance Yellow	None	Refer to Product Drawing	H5553[2]
XXXXX = G0B10	Q65110A5415	Spring Green	None	Refer to Product Drawing	H5563[2]
XXXXX = Y0B40	Q65110A5593	Elegance Yellow	Metal*	Refer to Product Drawing	H5551[3]
XXXXX = G0B40	Q65110A5592	Spring Green	Metal*	Refer to Product Drawing	H5561[3]

[1] For this OLED Module Product Drawing, please refer to page 22

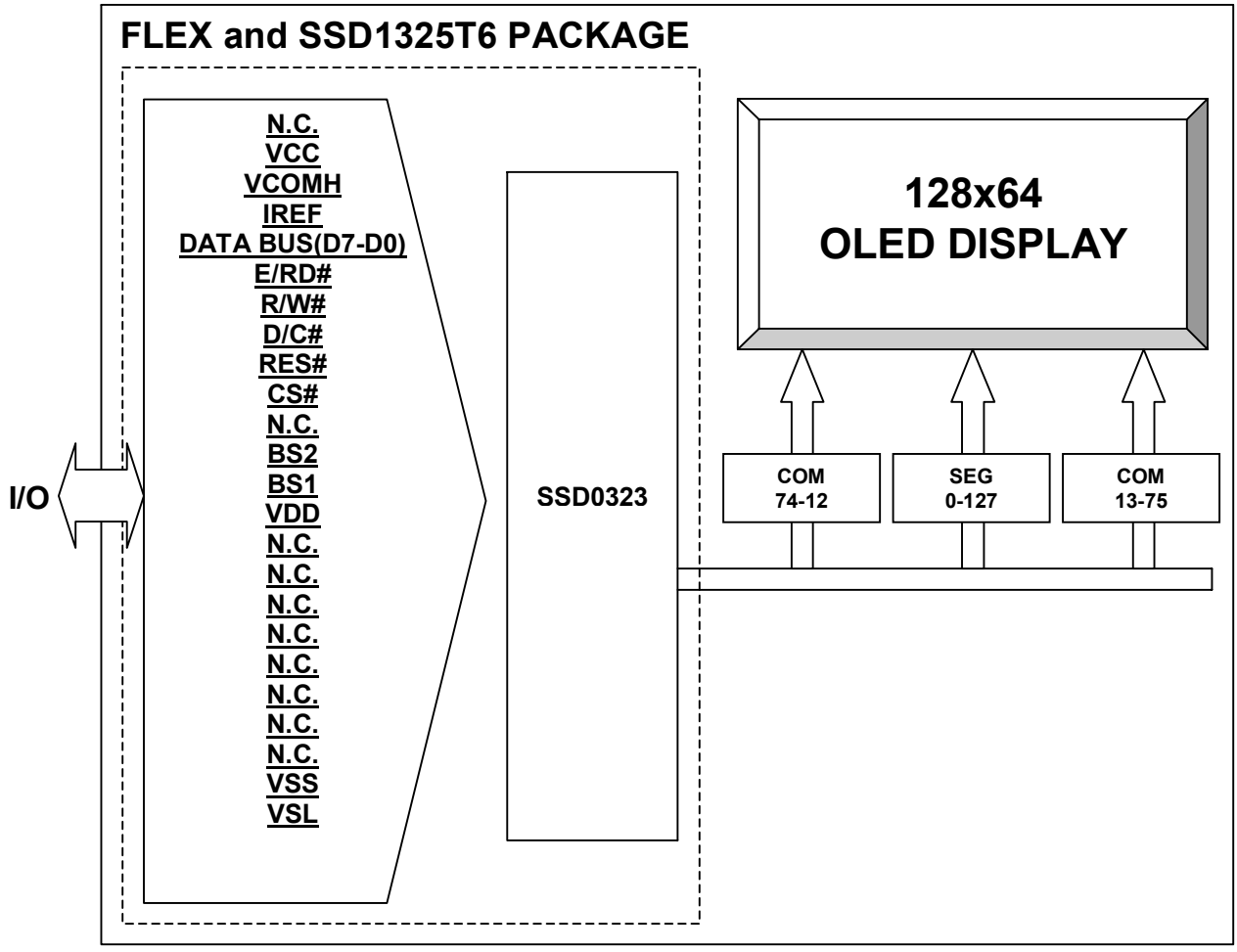
[2] For this OLED Module Product Drawing, please refer to page 23

[3] For this OLED Module Product Drawing, please refer to page 24

*Note: These products are having a different bezel type and outline from [1]

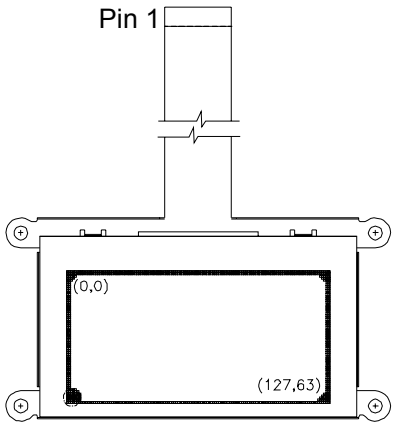
5.1.3. Electrical Characteristics

Functional Block Diagram



Overall block diagram of display module assembly and interface

5.1.4. Graphic Area Pixel Mapping:



Pixel mapping

5.1.5. Graphic Display Data RAM (GDDRAM) access

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to table below for GDDRAM address map description)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
⋮	⋮										
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124		SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]		D5040[7:4]	(HEX)
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
⋮	⋮										
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]		D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E	D5055[7:4	D5055[3:0	D5054[7:4	D5054[3:0		D4993[7:4	D4993[3:0	D4992[7:4	D4992[3:0	
COM79	4F	D5119[7:4	D5119[3:0	D5118[7:4	D5118[3:0		D5057[7:4	D5057[3:0	D5056[7:4	D5056[3:0	

COM Outputs | Row Address (HEX)

(Display Startline=0)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re- map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs | Row Address (HEX)

(Display Startline=10H)

GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, … , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00										(HEX)
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs | Row Address (HEX)

(Display Startline=0)

5.1.6. Duty Cycle

The pixel rows are multiplexed and will operate at a nominal duty cycle of 1/64. The default duty cycle is 1/80. During initialization, a software command must be used to set the required duty cycle.

5.1.7. Interface Pin Out

Flex Connection Pin Out

PIN	Name	DESCRIPTION
1	NC	No connect.
2	VCC(VLL)	OLED power supply voltage VCC (VLL).
3	VCOMH	Common (Row) High Voltage, a capacitor should be connected between this pin and VSS.
4	IREF	Segment (Column) Current Reference. A resistor should be connected between this pin and VSS.
5	D7	Parallel Data 7
6	D6	Parallel Data 6
7	D5	Parallel Data 5
8	D4	Parallel Data 4
9	D3	Parallel Data 3
10	D2	Parallel Data 2 (Serial Mode: Floating)
11	D1	Parallel Data 1 (Serial Mode: Data)
12	D0	Parallel Data 0 (Serial Mode: Serial Clock)
13	E (RD#)	E clock for 68 series; RD strobe for 80 series
14	R/W (WR#)	Read/Write selector for 68 series; Write strobe for 80 series
15	D/C	HIGH = Bus contains data for DDRAM, LOW = Bus contains command.
16	RES#	Reset.
17	CS#	Chip Select.
18	NC	No Connect.
19	BS2	Interface Selection Pin 2:
		| | 6800 Parallel | 8080 Parallel | Serial |
		| BS1 | 0 | 1 | 0 |
		| BS2 | 1 | 1 | 0 |
20	BS1	Interface Selection Pin 1: See BS2 above.
21	VDD	Positive logic supply voltage.
22	NC	No connect.
23	NC	No connect.
24	NC	No connect.
25	NC	No connect.
26	NC	No connect.
27	NC	No connect.
28	NC	No connect.
29	VSS	Ground.
30	VSL	Voltage Segment Low, a capacitor should be connected between this pin and VSS.

5.1.8. Absolute Maximum Ratings:

Absolute Maximum Ratings

Symbol	Description	Range	Unit
VDD	Supply Voltage for logic	-0.3 to +4.0	V
VCC	Supply Voltage for driver	0 to +16	V
Vin	Input Voltage	VSS-0.3 to VDD+0.4	V
Top(1)	Operating Temperature	-30 to +70	ºC
Top(2)		-40 to +85	
Tstg(1)	Storage Temperature	-40 to +70	ºC
Tstg(2)		-40 to +85	
Pop / Pstg	Pressure Operating and Storage	> 0.500	atm

(1) This temperature range is valid for Elegance Yellow Products

(2) This temperature range is valid for Spring Green Products

5.1.9. DC Characteristics of Complete Module:

(-30°C to +70°C Temperature Range, except as noted)

Recommended DC Operating Conditions

Description		Symbol	Min.	Typ.	Max.	Unit
Logic operating voltage		VDD	2.4	3.0	3.5	V
OLED driver input voltage		VCC(1)	14.25	15.00	15.75	V
		VCC(2)	12.0	12.5	13.0	V
VDD Operating Current		IDD	-	-	650.0	µA
VCC Operating Current		ICC	-	-	55.0	mA
Driver Sleep Mode Current (at 25°C)		ISL	-	-	5.0	µA
Logic input voltage	High	VIH	.8 *VDD	-	VDD	V
	Low	VIL	0	-	.2*VDD	V
Logic output voltage	High (IOH=-.1mA)	VOH	.9 *VDD	-	VDD	V
	Low (IOL=.1mA)	VOL	0	-	.1*VDD	V

(1) This voltage level is use to get luminance of 100 cd/m².

(2) This voltage level is use to get luminance of 75 cd/m².

5.1.10. Power Consumption: (VDD = 3.0V, VCC = 15V, Frame Frequency = 100 Hz, unless otherwise stated)

Power Consumption (External Vcc mode)

		Typical Power Consumption* (mW), Dual supply (VDD, VCC)				
Color	**Typical Luminance** cd/m²	Power Save mode (Sleep mode)	All pixels ON @ typical luminance	10% ON @ typical luminance	10% ON @ 15% of typical luminance	2% ON @ 15% of typical luminance
Elegance Yellow	100	0.018	716	92	25	13
Spring Green	100	0.018	477	66	19	10

5.1.11. Power Consumption: (VDD = 3.0V, VCC = 12V, Frame Frequency = 100 Hz, unless otherwise stated)

Power Consumption (External Vcc mode)

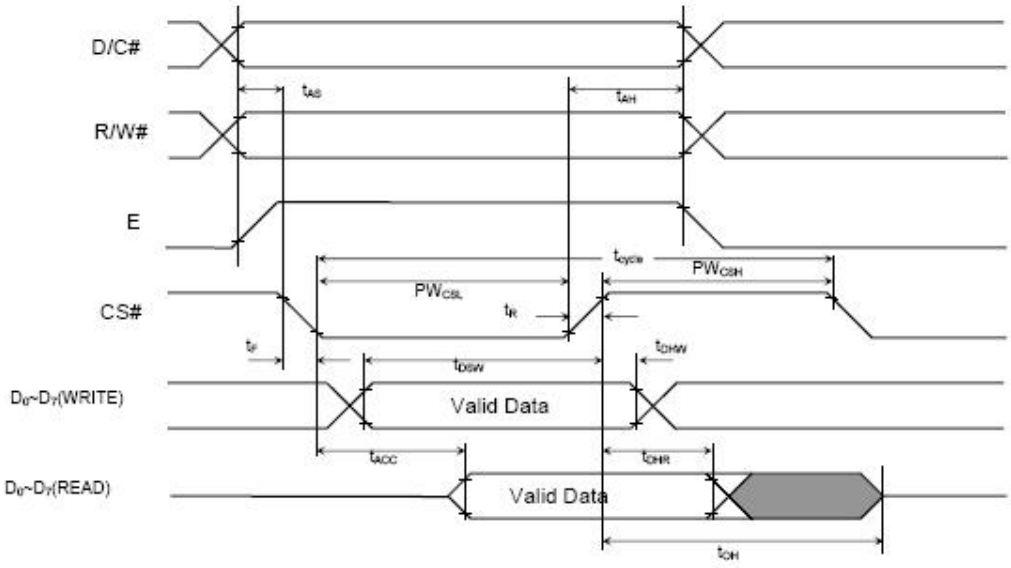
		Typical Power Consumption* (mW), Dual supply (VDD, VCC)				
Color	**Typical Luminance** cd/m²	Power Save mode (Sleep mode)	All pixels ON @ typical luminance	10% ON @ typical luminance	10% ON @ 15% of typical luminance	2% ON @ 15% of typical luminance
Elegance Yellow	75	0.016	440	58	21	10
Spring Green	75	0.016	295	38	14	7
Elegance Yellow	50	0.016	250	35	5	2
Spring Green	50	0.016	225	30	4	1

5.1.12. AC Timing Characteristics

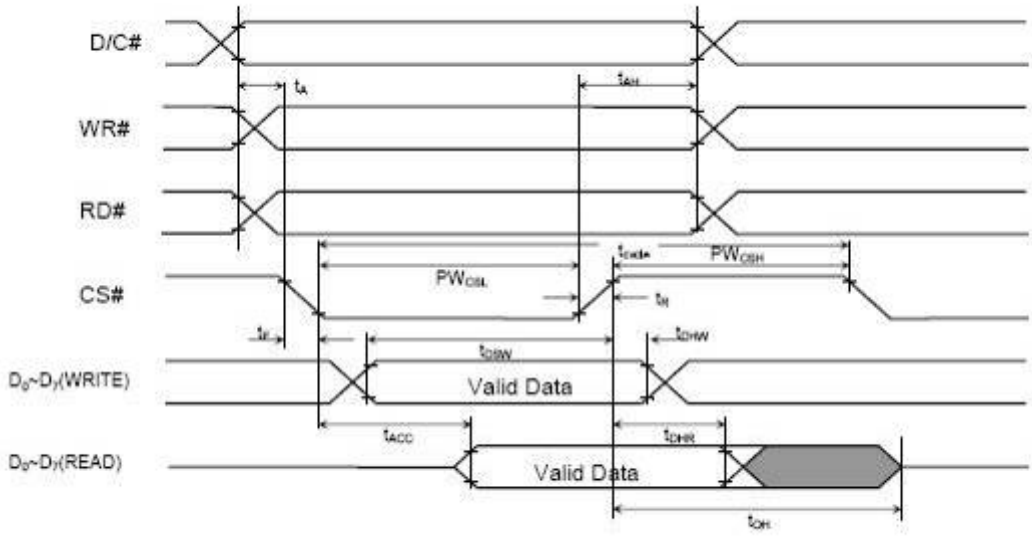
5.1.12.1. Parallel Interface Timing Characteristics

Parallel Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	300	-	-	ns
Address Setup Time	tAS	0	-	-	ns
Address Hold Time	tAH	0	-	-	ns
Write Data Setup Time	tDSW	40	-	-	ns
Write Data Hold Time	tDHW	15	-	-	ns
Read Data Hold Time	tDHR	20	-	-	ns
Output Disable Time	tOH	-	-	70	ns
Access Time	tACC	-	-	140	ns
Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	PW CSL	120 160	-	-	ns
Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	PWCSH	60 60	-	-	ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



Parallel Interface Timing Diagram for 68 Series MPU

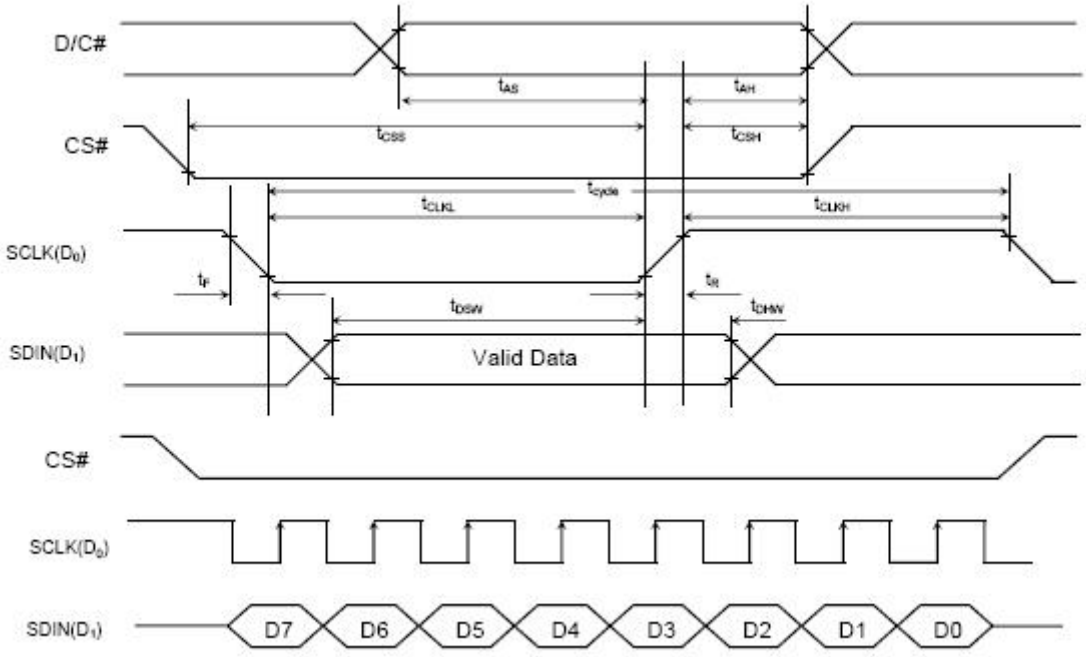


Parallel Interface Timing Diagram for 80 Series MPU

5.1.12.2. Serial Interface Timing Characteristics

Serial Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	250	-	-	ns
Address Setup Time	tAS	150	-	-	ns
Address Hold Time	tAH	150	-	-	ns
Chip Select Setup Time	tCSS	120	-	-	ns
Chip Select Hold Time	tCSH	60	-	-	ns
Write Data Setup Time	tDSW	100	-	-	ns
Write Data Hold Time	tDHW	100	-	-	ns
Clock Low Time	tCLKL	100	-	-	ns
Clock High Time	tCLKH	100	-	-	ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



Serial Interface Timing Diagram

5.2. DISPLAY PROGRAMMING

5.2.1. Power Up and Down Sequence

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

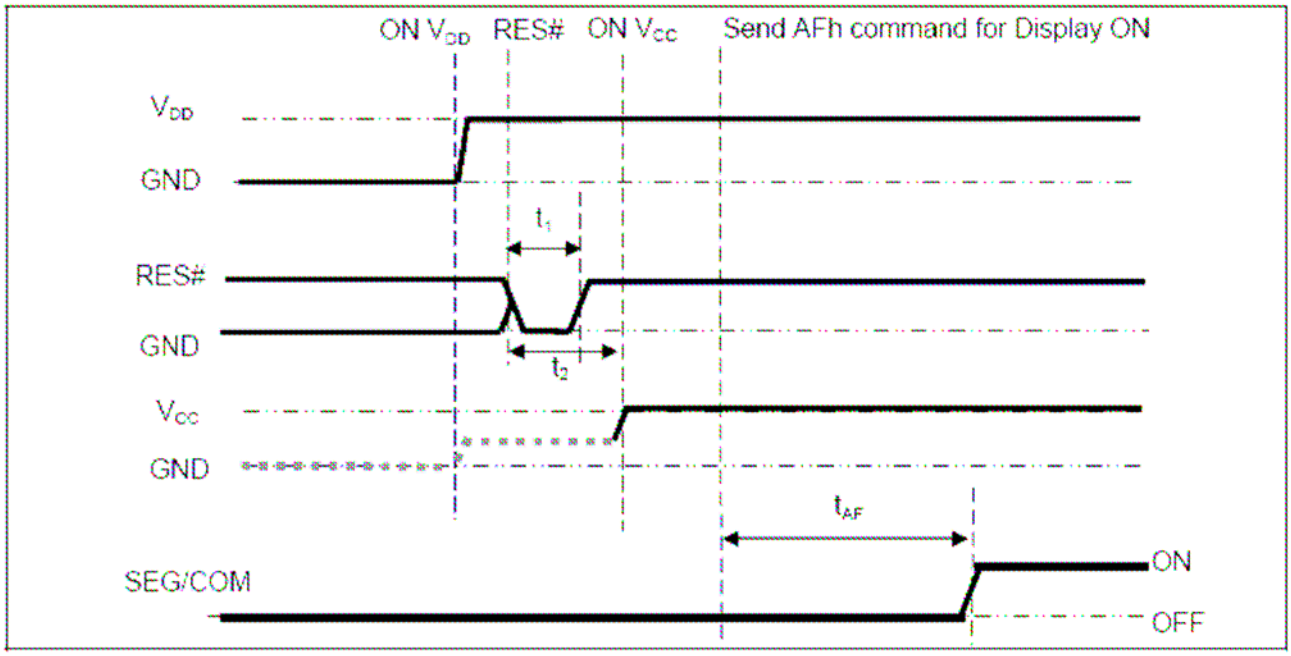
Power-Up Sequence:

i) Power-Up Vdd

ii) After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us (t_1) and then HIGH (logic HIGH)

iii) After set RES# pin LOW (logic LOW), wait for at least 3us (t_2). Then Power ON V_{CC}

iv) After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 30ms (t_{AF}).



Power-Up Diagram

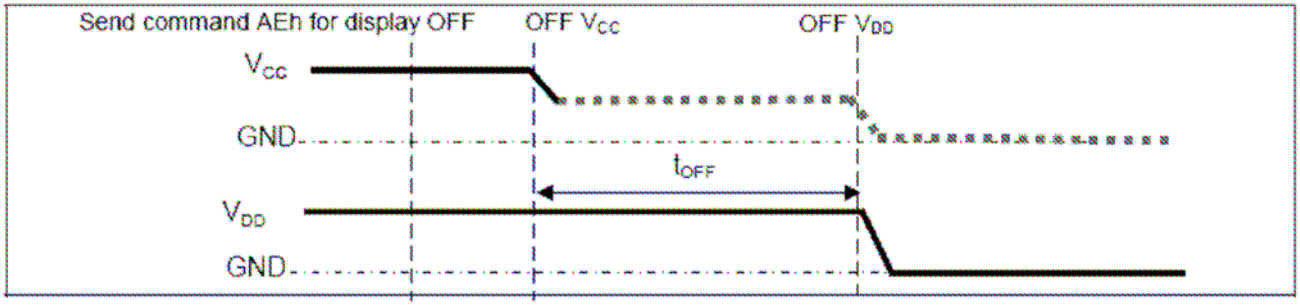
Power-Down Sequence:

i) Send command AEh for Display off

ii) Wait until panel discharges completely

iii) Power down Vcc

iv) Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=30ms)



Power-Down Diagram

5.2.2. Recommended Initialization Command

Command at VDD= 3.0V, ***VCC = 15V***, Frame Frequency = 100 Hz

Refer to IC specification: Solomon SSD0323/SSD1325 OLED/PLED Segment/Common Driver with Controller CMOS. After power up, the commands specified in below table must be executed during initialization.

Initialization Sequence

Command	Code	Default on POR	Initialization (Dual Voltage Supply)	
			Elegance Yellow	Spring Green
Set Column Address	15	00 3F	Default	
Set Row Address	75	00 4F	00 3F	
Set Contrast Control	81	40	6D*	4C*
Set Current Range	84~86	Quarter (84)	Full (86)*	
Set Re-map	A0	00	41	
Set Display Start Line	A1	00	Default	
Set Display Offset	A2	00	44	
Set Multiplex Ratio	A8	4F	3F	
Set Display ON/OFF		AE	AF	
Set Display Mode		A4	Default	
Set DC-DC Converter	AD	03	02 (disabled)	
Set DC-DC Bias Current	CF	F0	Default	
Set Row Period	B2	25	46	
Set Pre-charge Compensation Enable	B0	08	28	
Set Pre-charge Compensation Level	B4	00	07	
Set Clock Divide	B3	02	91	
Set Phase Length	B1	P1 = 3, P2 = 5	22 (P1 = 2, P2 = 2)	
Set VSL	BF	0E	0D	
Set VcomH	BE	11	02*	00*
Set Vprecharge	BC	18	10*	0B*
Set Gray Scale Table	B8	All 1	Refer to Grey Scale Settings Table	

*Note: This setting represents maximum luminance for proper operation of the display. Lower setting can be used for dimming. Higher setting will adversely affect the operating lifetime as defined in this specification and can lead to crosstalk effects if the Vcomh setting is not corrected accordingly.

Command at VDD= 3.0V, ***VCC = 12V***, Frame Frequency = 100 Hz

Refer to IC specification: Solomon SSD0323/SSD1325 OLED/PLED Segment/Common Driver with Controller CMOS. After power up, the commands specified in below table must be executed during initialization.

Initialization Sequence

Command	Code	Default on POR	Initialization (Dual Voltage Supply)	
			Elegance Yellow	Spring Green
Set Column Address	15	00 3F	Default	
Set Row Address	75	00 4F	00 3F	
Set Current Range	84~86	Quarter (84)	Full (86)	
Set Re-map	A0	00	41	
Set Display Start Line	A1	00	Default	
Set Display Offset	A2	00	44	
Set Multiplex Ratio	A8	4F	3F	
Set Display ON/OFF		AE	AF	
Set Display Mode		A4	Default	
Set DC-DC Converter	AD	03	02 (disabled)	
Set DC-DC Bias Current	CF	F0	Default	
Set Row Period	B2	25	46	
Set Pre-charge Compensation Enable	B0	08	28	
Set Pre-charge Compensation Level	B4	00	07	
Set Clock Divide	B3	02	F1	
Set Phase Length	B1	P1 = 3, P2 = 5	22 (P1 = 2, P2 = 2)	
Set VSL	BF	0E	0D	
Set VcomH	BE	11	02 *	00*
Set Vprecharge	BC	18	10 *	0B*
Set Gray Scale Table	B8	All 1	Refer to Grey Scale Settings Table	

For different luminance settings, the command specified in below table must be executed during initialization:

Command	Code	Default on POR	Luminance, cd/m^2	Initialization (Dual Voltage Supply)	
				Elegance Yellow	Spring Green
Set Contrast Control	81	40	75	66 *	40 *
			50	33 *	2C *

*Note: This setting represents maximum luminance for proper operation of the display. Lower setting can be used for dimming. Higher setting will adversely affect the operating lifetime as defined in this specification and can lead to crosstalk effects if the Vcomh setting is not corrected accordingly.

Sample Gray Scale Settings (Decimal)

GS level	Phase 1	Phase 2	S/W Set	GS Pulse	Total DCLK
L0	2	2	0	0	4
L1	2	2	1	1	5
L2	2	2	1	3	7
L3	2	2	1	5	9
L4	2	2	2	8	12
L5	2	2	2	11	15
L6	2	2	2	14	18
L7	2	2	3	18	22
L8	2	2	3	22	26
L9	2	2	4	27	31
L10	2	2	4	32	36
L11	2	2	5	38	42
L12	2	2	5	44	48
L13	2	2	6	51	55
L14	2	2	6	58	62
L15	2	2	7	66	70

5.2.3. Sample Initialization Code

```
/*****************************************
// Calgary 4 Bits SSD0323 H555X Elegance Yellow Initialization Command
*****************************************/
void blank(void)
{
   uint i,j;
   for (j=0;j<80;j++)        /* 80 row */
   {
      CST = 0;
      DC  = 1;
      WRT = 0;
      for (i=0;i<64;i++)     /* 128 column (1 byte = 2col ) */
      {
                             wr_dt(0x00);
      }
      WRT = 1;
   }
}

// Column Address
   WriteCommand(0x15);   /* Set Column Address */
   WriteCommand(0x00);   /* Start = 0 */
   WriteCommand(0x3F);    /* End = 127 */
// Row Address
   WriteCommand(0x75);   /* Set Row Address */
   WriteCommand(0x00);   /* Start = 0 */
   WriteCommand(0x3F);    /* End =  63 */
// Contrast Control
   WriteCommand(0x81);   /* Set Contrast Control (1) */
   WriteCommand(0x6D);   /* 0 ~ 127 */
// Current Range
   WriteCommand(0x86);   /* Set Current Range 84h:Quarter,  85h:Half, 86h:Full*/
// Re-map
   WriteCommand(0xA0);   /* Set Re-map */
   WriteCommand(0x41);   /* [0]:MX, [1]:Nibble, [2]:H/V address [4]:MY, [6]:Com Split Odd/Even "1000010"*/
// Display Start Line
   WriteCommand(0xA1);   /* Set Display Start Line */
   WriteCommand(0x00);   /* Start at row 0 */
// Display Offset
   WriteCommand(0xA2);   /* Set Display Offset */
   WriteCommand(0x44);   /* Offset 68 rows */
// Display Mode
   WriteCommand(0xA4);   /* Set DisplaMode,A4:Normal,    A5:All ON, A6: All OFF, A7:Inverse       */
// Multiplex Ratio
   WriteCommand(0xA8);   /* Set Multiplex Ratio */
   WriteCommand(0x3F);   /* 64 mux*/
// Phase Length
   WriteCommand(0xB1);   /* Set Phase Length */
   WriteCommand(0x22);   /* [3:0]:Phase 1 period of 1~16 clocks */
                         /* [7:4]:Phase 2 period of 1~16 clocks /* POR = 0111 0100 */

// Set Pre-charge Compensation Enable
   WriteCommand(0xB0);   /* Set Pre-charge Compensation Enable */
   WriteCommand(0x28);   /* Enable*/
// Set Pre-charge Compensation Level
   WriteCommand(0xB4);   /* Set Pre-charge Compensation Level */
   WriteCommand(0x07);   /* Higher level */
// Row Period
   WriteCommand(0xB2);   /* Set Row Period */
   WriteCommand(0x46);   /* [7:0]:18~255, K=P1+P2+GS15 (POR:4+7+29)*/
// Display Clock Divide
   WriteCommand(0xB3);   /* Set Clock Divide (2) */
   WriteCommand(0x91);   /* [3:0]:1~16, [7:4]:0~16, 100Hz */
     /* POR = 0000 0001 */
// VSL
   WriteCommand(0xBF);   /* Set VSL */
   WriteCommand(0x0D);   /* [3:0]:VSL */
// VCOMH
   WriteCommand(0xBE);   /* Set VCOMH (3) */
   WriteCommand(0x02);   /* [7:0]:VCOMH, (0.53 X Vref = 0.53 X 15 V = 7.95V)*/
```

```
// VP
   WriteCommand(0xBC);   /* Set VP (4) */
   WriteCommand(0x10);   /* [7:0]:VP, (0.67 X Vref = 0.67 X 15 V = 10.05V) */
// Gamma
   WriteCommand(0xB8);   /* Set Gamma with next 8 bytes */
   WriteCommand(0x01);   /* L1[2:1] */
   WriteCommand(0x11);   /* L3[6:4], L2[2:0] 0001 0001 */
   WriteCommand(0x22);   /* L5[6:4], L4[2:0] 0010 0010 */
   WriteCommand(0x32);   /* L7[6:4], L6[2:0] 0011 1011 */
   WriteCommand(0x43);   /* L9[6:4], L8[2:0] 0100 0100 */
   WriteCommand(0x54);   /* LB[6:4], LA[2:0] 0101 0101 */
   WriteCommand(0x65);   /* LD[6:4], LC[2:0] 0110 0110 */
   WriteCommand(0x76);   /* LF[6:4], LE[2:0] 1000 0111 */

// Set DC-DC
   WriteCommand(0xAD);   /* Set DC-DC */
   WriteCommand(0x02);   /* 03=ON, 02=Off */
// Display ON/OFF
         WriteCommand(0xAF);         /* AF=ON, AE=Sleep Mode */
```

*Note: The code for initialization command above is valid with reference to the table of Initialization Sequence.

5.3. OPTICAL CHARACTERISTICS (Ta = 25°C, unless otherwise stated)

Optical & Operating Lifetime Characteristics

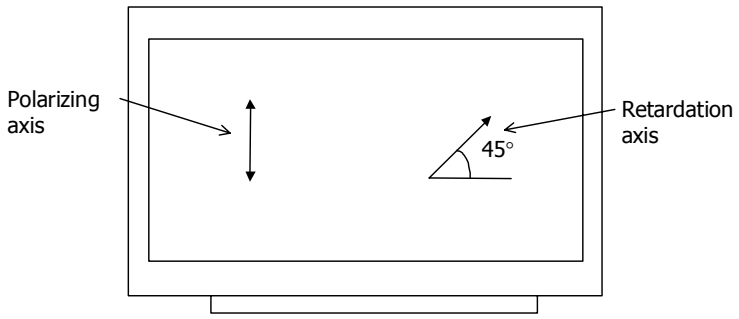
	Condition	Min.	Typ.	Max.	Unit
Contrast Ratio	$\upsilon = \phi = 0°$, Dark	-	2000	-	-
	Direct Sun Light	1.05	-	-	
Brightness Uniformity	$\upsilon = \phi = 0°$	-	-	+20	%
Visible Flicker	$\upsilon = \phi = 0°$	-	None	-	-
Cross Talk (Brightness variation of non-selected pixels)	$\upsilon = \phi = 0°$	-	-	10	%

Color Coordinates and Initial Luminance

Product	Color	X, Y color coodinate, 1931CIE ±0.02	Initial Luminance, cd/m²			Operating Life*, hour, @ 25°C
			Min.	Typ.	Max.	
H555X-OS128064PK27MY0BX0	Elegance Yellow	0.46 ± 0.03; 0.54	90	100	120	40K
			65	75	95	55K
			40	50	70	TBA
H556X-OS128064PK27MG0BX0	Spring Green	0.41 ± 0.03; 0.58	90	100	120	15K
			65	75	95	19K
			40	50	70	TBA

*Operating Lifetime is Time to Half Luminance; based on the display operated at 25°C at typical brightness level with specified software settings, until 50% of initial luminance is reached.

5.3.1. Polarizing Angle



Orientation of OLED polarizer angle

5.4. MECHANICAL CHARACTERISTICS

5.4.1. Interconnections

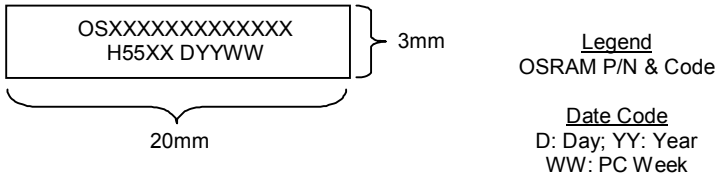
The display module should be electrically connected to a controller on the user's board through the 30-contact pad ZIF tail.

5.4.2. Recommended mating connectors

5.4.2.1. Bottom Contact : MOLEX 52893-3095, or equilvalent
5.4.2.2. Top Contact : MOLEX 54104-3031, or equilvalent

5.4.3. Product Marking

Parts are marked with a label on the module

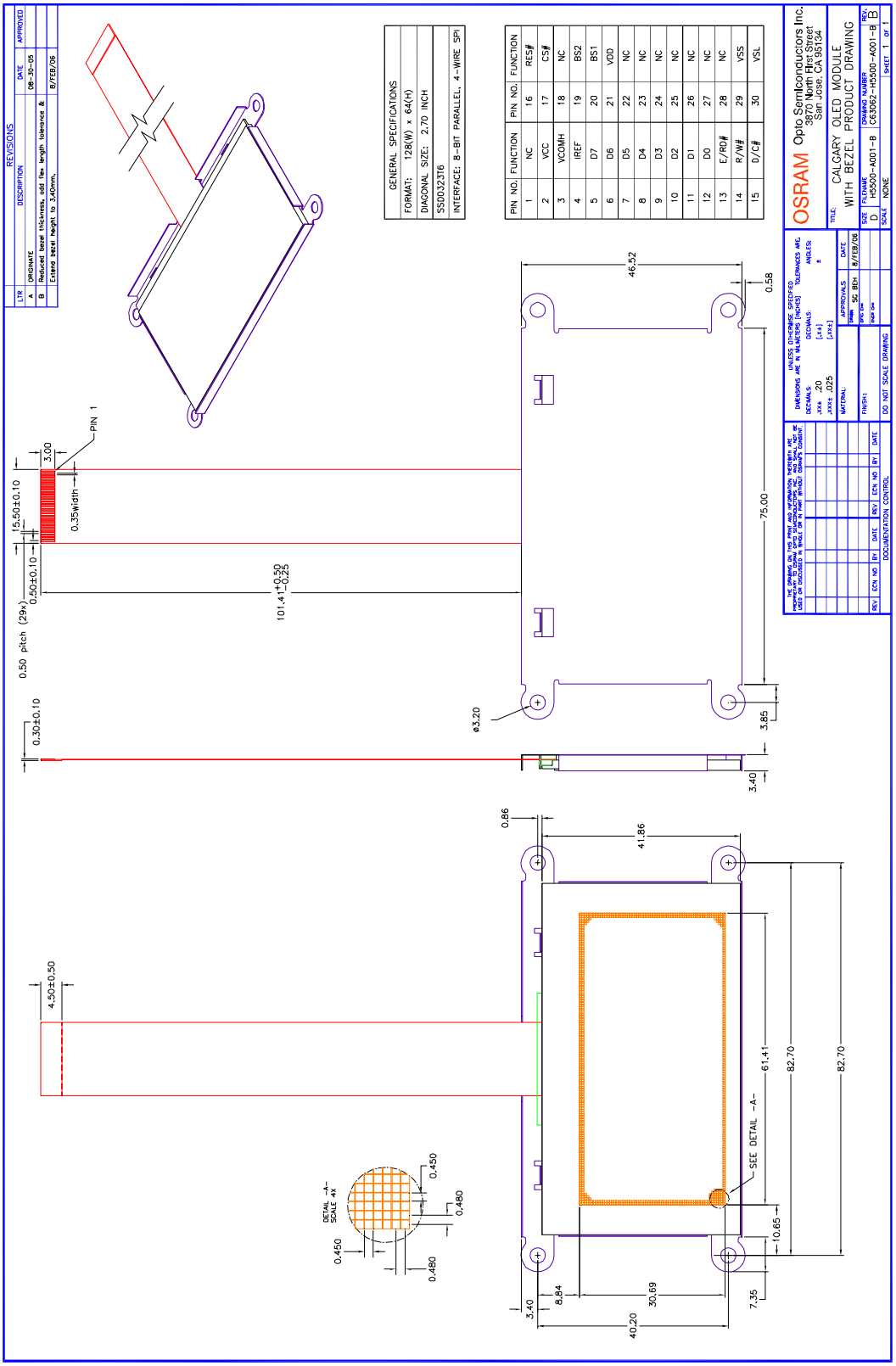


Description of part label marking requirements

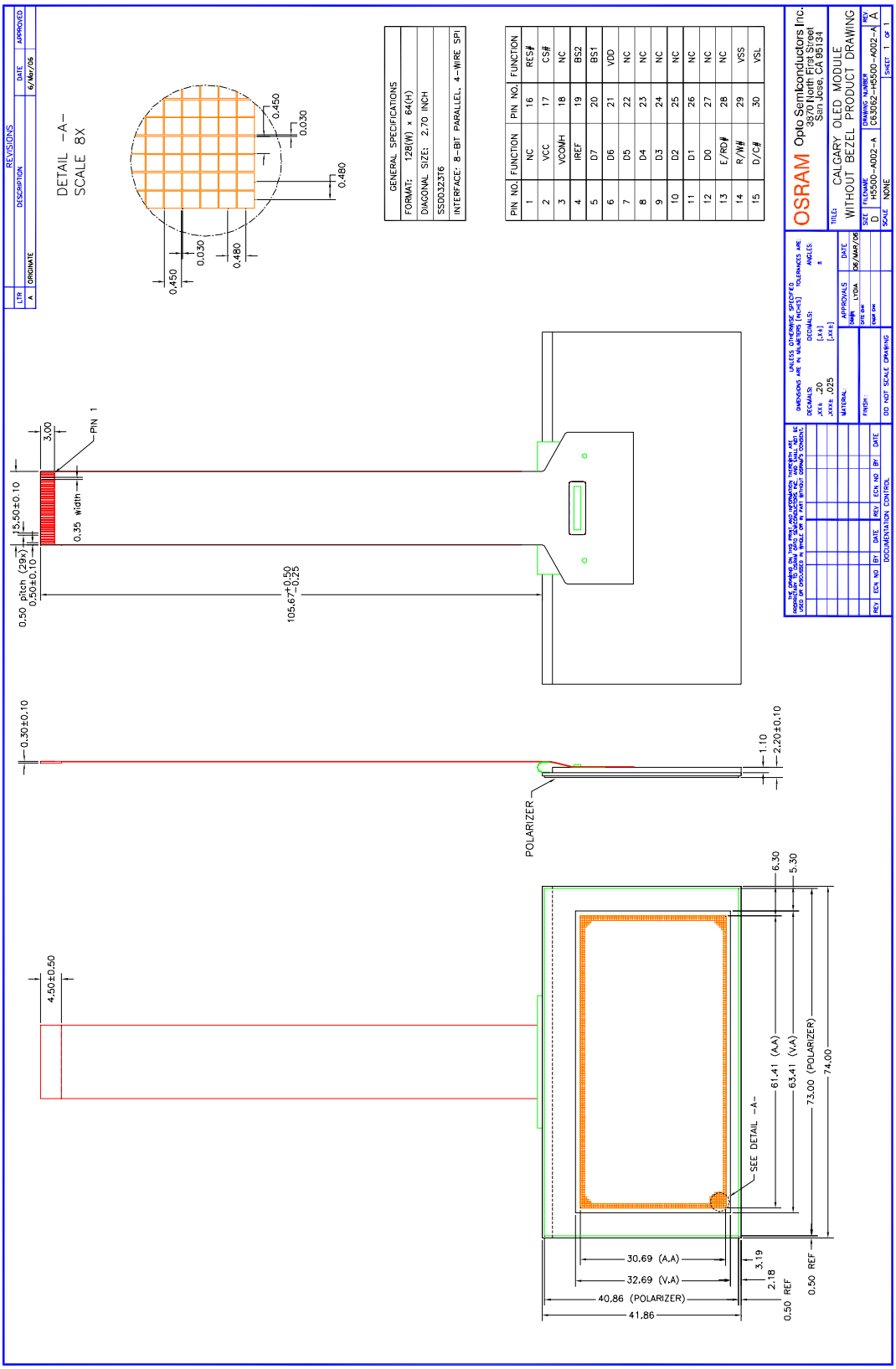
5.5. MODULE MECHANICAL DRAWING

The mechanical drawings shown below are for reference.

Module drawing for parts with bezel (H55X0)

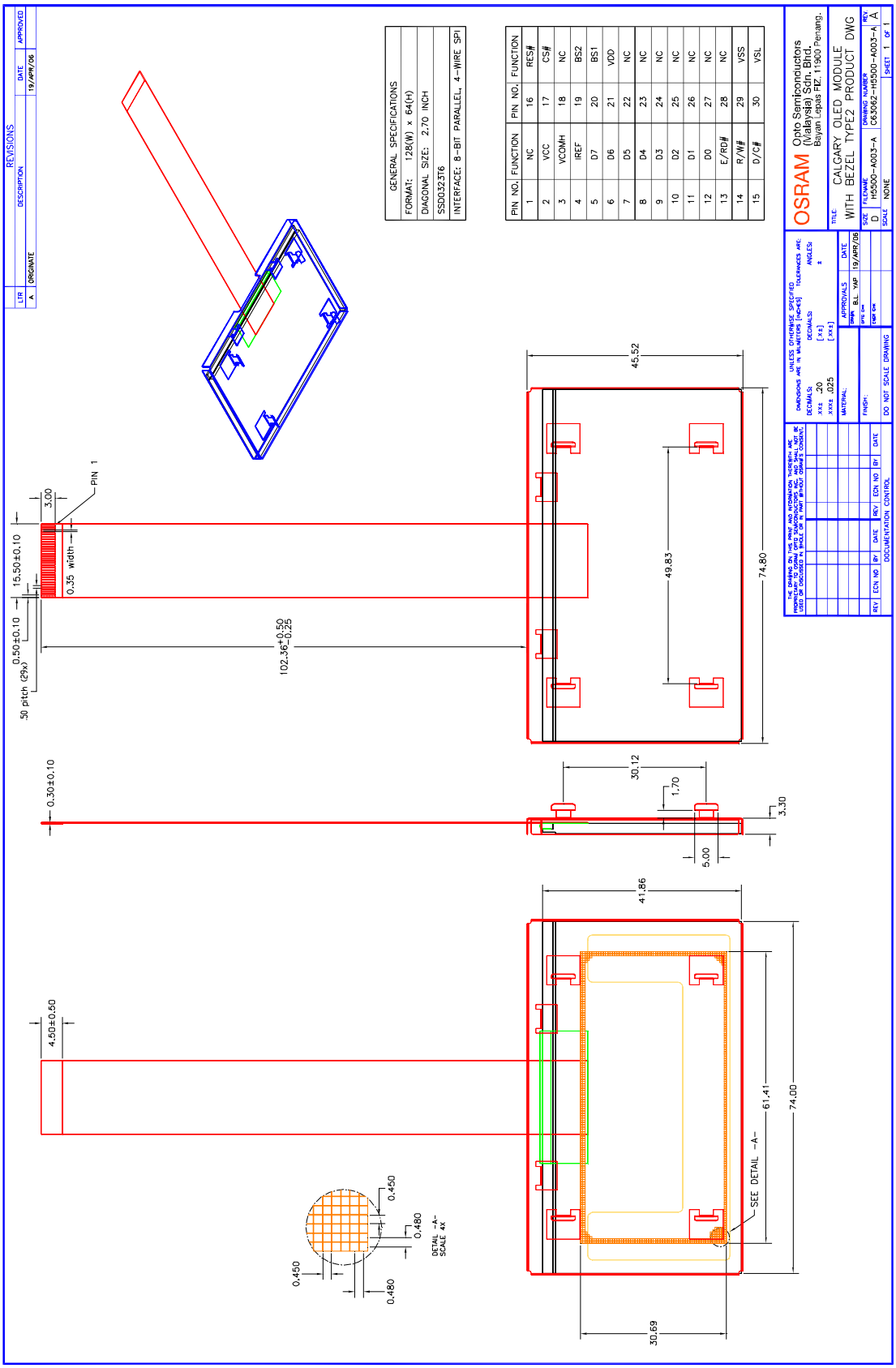


Module drawing for parts without bezel (H55X3)



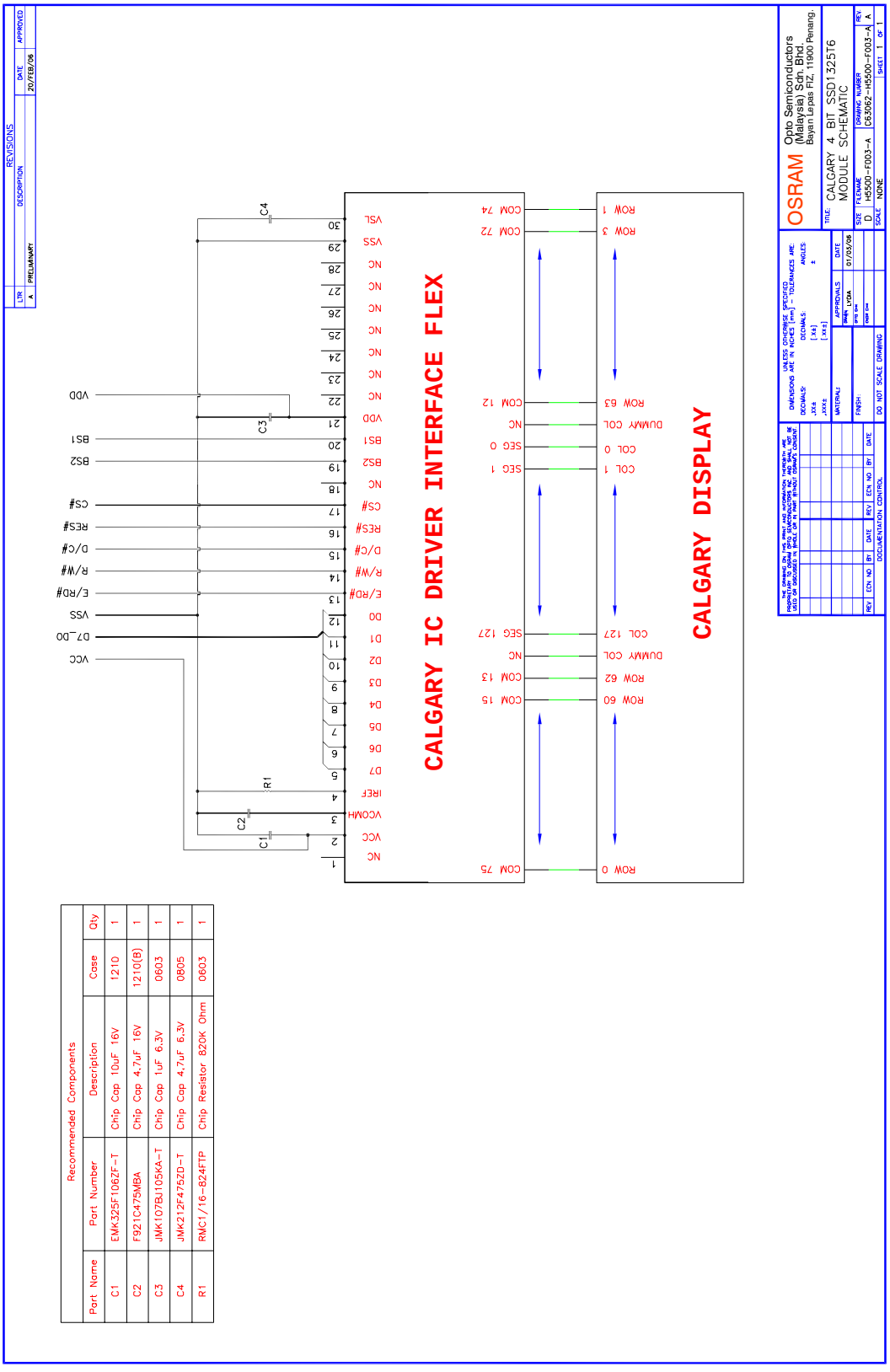
*Remarks: SSD0323 is labeled with SSD1325T6 on TAB

Module drawing for parts with bezel type2 (H55X1)



6. SCHEMATIC DRAWINGS

Calgary 4-bits SSD1325T6 TAB Interface Schematic



Part Name	Recommended Components: Part Number	Description	Case	Qty
C1	EMK325F1062ZF-T	Chip Cap 10uF 16V	1210	1
C2	F921C475MBA	Chip Cap 4.7uF 16V	1210(B)	1
C3	JMK107BJ105KA-T	Chip Cap 1uF 6.3V	0603	1
C4	JMK212F475ZD-T	Chip Cap 4.7uF 6.3V	0805	1
R1	RMC1/16-824FTP	Chip Resistor 820K Ohm	0603	1

7. QUALIFICATION TESTS

7.1. QUALIFICATION TESTS

For reference, the main qualification tests and test criteria done on the OLED module are indicated as per below tables.

OLED Module Internal Qualification Tests

For Elegance Yellow Modules

Test	Condition	Duration	
		Guarenteed	Capability
High Temperature and Humidity Bias (THB) *	60°C / 90% RH	250 hrs	504 hrs
High Temperature Operating (ELT) *	70°C	336 hrs	1000 hrs
	85°C	-	250 hrs
Powered Temperature Cycle (PTC) *	-30°C / 70°C; 30 min. dwell time; 15 min. transition time	60 cycles	60 cycles
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles	100 cycles
Low Temperature Storage (LTS)	-40°C	336 hrs	> 1000 hrs
High Temperature Storage (HTS)	70°C	336 hrs	> 1000 hrs
	85°C	-	> 500 hrs

For Spring Green Modules

Test	Condition	Duration	
		Guarenteed	Capability
High Temperature and Humidity Bias (THB) *	60°C / 90% RH	250 hrs	-
High Temperature Operating (ELT) *	85°C	500 hrs	-
Powered Temperature Cycle (PTC) *	-30°C / 70°C; 30 min. dwell time; 15 min. transition time	60 cycles	-
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles	-
Low Temperature Storage (LTS)	-40°C	500 hrs	-
High Temperature Storage (HTS)	85°C	500 hrs	-
Low Temperature Operating (LTO) *	- -40°C	500 hrs	-

* Note: The modules are powered for these tests, with a standard OSRAM pattern (50% emission ratio)

Test	Condition	Duration
Low Air Pressure (LAT) **	15kPa 25°C (0.15bar)	16hrs
Mechanical Vibration **	10-58hz 0.75mm 58-150Hz 10g, 1oct/min	10 sweeps per X, Y, Z direction
Mechanical Shock **	11ms half sine 100g peak	6 shocks per X, Y, Z direction
Mechanical Bump **	6ms half sine 40g Peak	1000 bumps per X, Y, Z direction

** Note: These mechanical tests may not be performed on the specific part numbers in this specification.

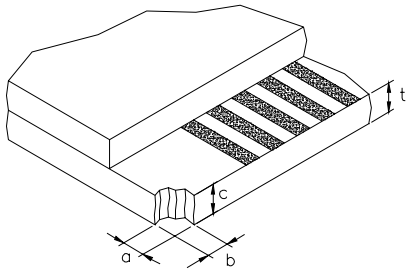
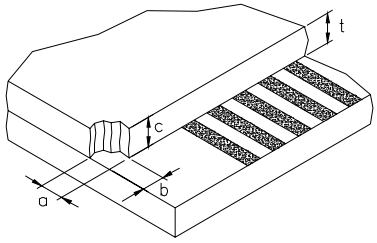
OLED Module Qualification Test Criteria

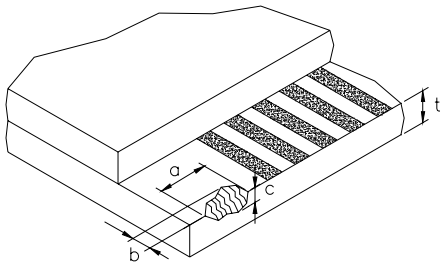
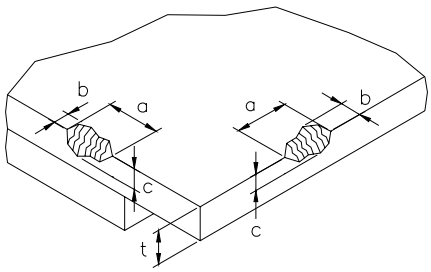
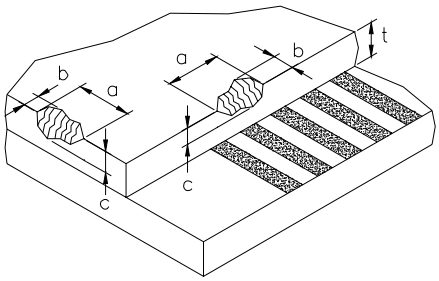
Acceptance Criteria (without polarizer):	**Test Patterns for Powered Tests:**
< 50% luminance loss after test 5 point luminance uniformity <20% No mechanical failure No electrical failure Pixel gap (initial + growth) ≤ 30%	Checkerboard pattern Inverse Checkerboard pattern All pixels On All pixels Off

8. COSMETIC CRITERIA

Inspection Criteria

<table>
<tr><th>Items</th><th>Criterion for Defects</th><th>Defect Type</th></tr>
<tr><td>Black / bright spot, particle, pin-hole (on the glass / polarizer), dent on polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.1</td><td>Not counted</td></tr><tr><td>0.1 ≤ Φ ≤ 0.2</td><td>3</td></tr><tr><td>Φ > 0.2</td><td>0</td></tr></table>* Φ = (Long diameter + Short diameter)/2</td><td>Minor</td></tr>
<tr><td>Scratches / lines on the polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>W≤ 0.1</td><td>Not counted</td></tr><tr><td>L ≤ 2, 0.1 < W ≤ 0.2</td><td>3</td></tr><tr><td>W > 0.2</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>Polarizer Bubble</td><td>Reject if bubble is observed with naked eyes at 30cm distance. with the following criteria

Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.2</td><td>Not counted</td></tr><tr><td>0.2≤Φ ≤ 0.3</td><td>3</td></tr><tr><td>0.3 < Φ</td><td>0</td></tr></table>Outside Viewing Area – IGNORE</td><td>Minor</td></tr>
<tr><td>Polarizer coverage</td><td>Reject if the polarizer does not cover the Viewing Area.</td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Criteria for Corner Chip
t = Glass thickness
Accept If
a ≤ 1.5 mm or
b ≤ 1.5 mm
c ≤ t
  </td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Accept If
a ≤ 3.0 mm
or
b ≤ 3.0 mm
  </td><td>Minor</td></tr>
</table>

Chip on contact pad	**Criteria for Chips on contact pad** t = Glass thickness Accept if b ≤ 1/3 width of contact ledge 	Minor
Chip on Face of Display	**Criteria for Chips on Face of Display** Accept if b ≤ 1.5mm 	Minor
Chip on Back of Display	**Criteria for Chips on Back of Display** Accept if b ≤ 3.0 mm 	Minor

Definition of W & L & ϕ (Unit: mm)

Note: Distance between any two defects should be over 5 mm

9. GENERAL OLED MODULE HANDLING & CARE

9.1. Mechanical Handling

9.1.1. Avoid mechanical stress, such as shock and pressure. For parts designed without bezel, exercise caution to avoid glass chipping. When handled with bare fingers, pay special attention to sharp glass edges to avoid potential injury.

9.1.2. Avoid touching Flex contact pad with bare fingers and avoid mechanical stress and pressure on the flex.

9.1.3. Handle the polarizer with care. Avoid hard or sharp objects in contact with the display surface.

9.1.4. Store and operate the OLED display within the specified ratings. It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

9.1.5. Avoid corner contact to display during assembly or installation to end products.

9.1.6. Installation Bending: The flex is generally designed to facilitate mounting to a PCB or connector. It is not a dynamic flex. Therefore, bending should be limited to less than 3 times.

9.1.7. Bending Radius: The minimum bending radius is as shown in the product drawing or equal to the thickness of the rear cap glass, whichever is smaller.

9.1.8. Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause damage of polarizer or color fading, while an active OLED display with water condensation on its surface will cause corrosion of metal traces.

9.1.9. Cleaning:

9.1.9.1. Particle/ Foreign materials: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) to gently wipe over the surface of the display in one direction.

9.1.9.2. Glue/ Adhesive Residue:

9.1.9.2.1. Method 1: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) and applicator (dipped in IPA or ethanol if necessary) to gently wipe over the surface of the display in one direction.

9.1.9.2.2. Method 2: Use the finger cot to gently clean the stain on by rubbing it on the polarizer in one direction.

9.2. ESD

9.2.1. Electrostatic discharge (ESD): OLED modules are semiconductor devices. Take ESD handling precautions by wearing a ground strap and avoid contacting electrical connections.

Condition	MM	HBM
Vdd mode	200v	2000v
Vss mode	200v	2000v
IO mode	200v	2000v