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PSPICE Model SFH6700/01/02/05/11/12/19/20/21

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High Speed Optocoupler, 5 MBd

DESCRIPTION

This 5 MBd family is an industry standard optocoupler with a high efficient LED as input and an integrated photo detector as output. The detector incorporates a Schmitt-Trigger stage to improve noise immunity. The detector output is 3-state, totem pole or open collector.

Their PSPICE models are written from device characterization data for simulation. All symbols are in the symbol library file VSH_OPTO_5M.olb. All model data are in the PSPICE model library file VSH_OPTO_5M.lib.

This document is intended as a guideline of simulating with provided models and does not constitute as commercial product, neither a substitute to datasheet.

PART	MODEL DESCRIPTION	SYMBOL FILE	MODEL FILE	
SFH6700, SFH6719	Three state V _O : pin 7 V _E : pin 6	U1 8 V _{CC} 7 V _O 6 V _E 5 GND VSH_OPTO_5M.olb (1)	VSH_OPTO_5M.lib	
SFH6701, SFH6711, SFH6720, SFH6721	Totem pole V _O : pin 7	U2 8 V _{CC} 7 V _O 5 GND VSH_OPTO_5M.olb (1)	VSH_OPTO_5M.lib	
SFH6702, SFH6712	Totem pole V _O : pin 6	U3 8 V _{CC} 6 V _O 5 GND VSH_OPTO_5M.olb (1)	VSH_OPTO_5M.lib	
SFH6705	Open collector V _O : pin 6 need pull-up resistor ⁽¹⁾	04 2 3 K 6 V _O 5 GND VSH_OPTO_5M.olb (1)	VSH_OPTO_5M.lib	

Note

RECOMMENDED USE OF THE MODEL

- This model is designed only for use at 25 °C and should be used as is.
- This model has been created and tested with OrCAD version 16.3.
- The olb file (symbol) is not down-compatible. Users of the earlier versions need to create the symbols on their platform and associate with relative PSPICE model data.

⁽¹⁾ Applicable only with OrCAD16.3 or higher versions.

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TRUTH TABLE (positive logic)					
PART	LED	ENABLE (V _E)	OUTPUT (V _O) ⁽¹⁾		
SFH6700, SFH6719	On	Н	Z		
	Off	Н	Z		
	On	L	Н		
	Off	L	L		
SFH6701, SFH6702, SFH6711,	On	-	Н		
SFH6720, SFH6721, SFH6712, SFH6705 ⁽¹⁾	Off	-	L		

Nota

⁽¹⁾ SFH6705 with external pull-up resistor

SIMULATED PARAMETERS (T _{amb} = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	DATA	UNIT		
COUPLER						
Input threshold current	V _{CC} = 5 V	I _{Fon}	1.6	mA		
Input current hysteresis	$V_{CC} = 5 \text{ V}, I_{HYS} = I_{Fon} - I_{Foff}$	l _{HYS}	0.1	mA		
SWITCHING						
Propagation delay time to high output level ⁽²⁾	I _{Fon} = 3 mA, C _L = 15 pF ⁽¹⁾	t _{pLH}	200	ns		
Propagation delay time to low output level (2)		t _{pHL}	200	ns		

Notes

- $^{(1)}\,$ SFH6705 with pull-up resistor R_L = 390 Ω
- (2) See fig. 1 and timing simulation setup on page 3.

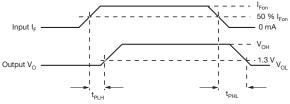


Fig. 1 - Switching Times

EXAMPLE SIMULATION PLOTS USING OrCAD

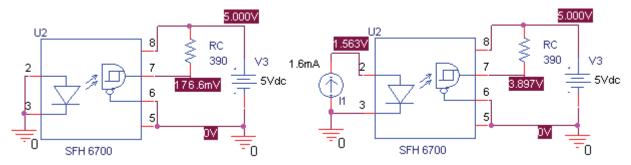


Fig. 2 - Simulation Setup for DC Characteristics of SFH6700

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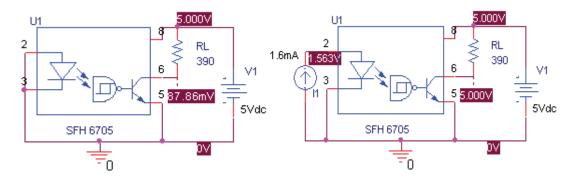


Fig. 3 - Simulation Setup for DC Characteristics of SFH6705

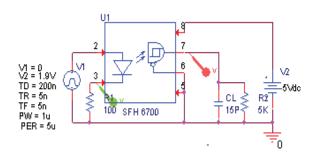


Fig. 4 - Timing Simulation Setup of SFH6700 ($V_{CC} = 5 \text{ V}, I_F = 3 \text{ mA}, C_L = 15 \text{ pF}$)

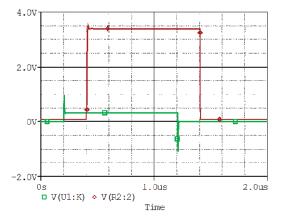


Fig. 5 - Timing Simulation Output of SFH6700

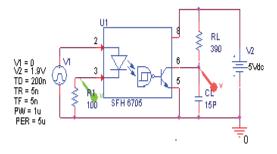


Fig. 6 - Timing Simulation Setup of SFH6705 (V_{CC} = 5 V, I_F = 3 mA, R_L = 390 Ω)

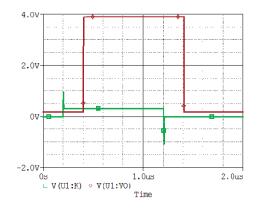


Fig. 7 - Timing Simulation Output of SFH6705